REPORT ON VLSI

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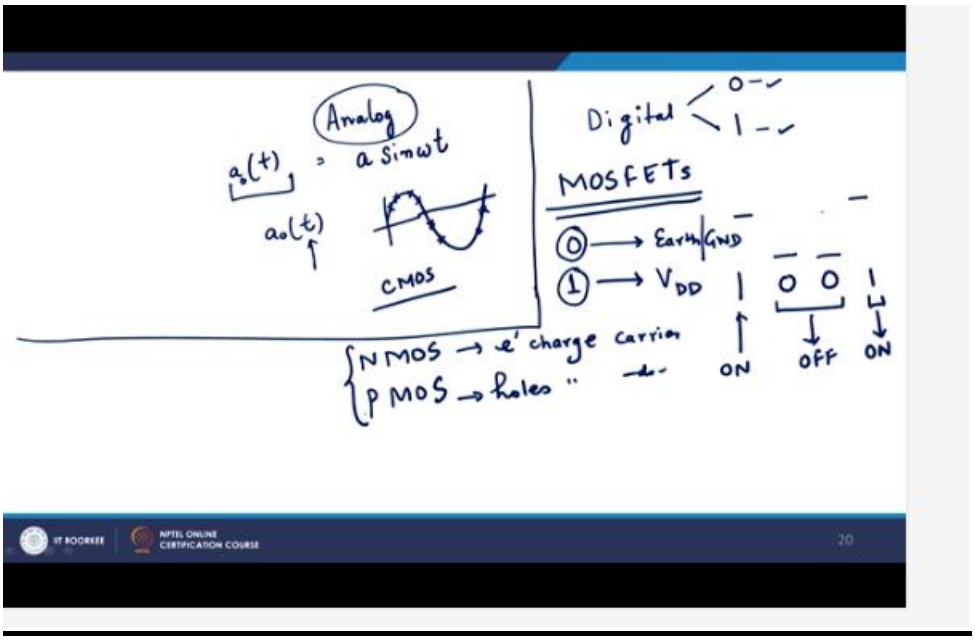
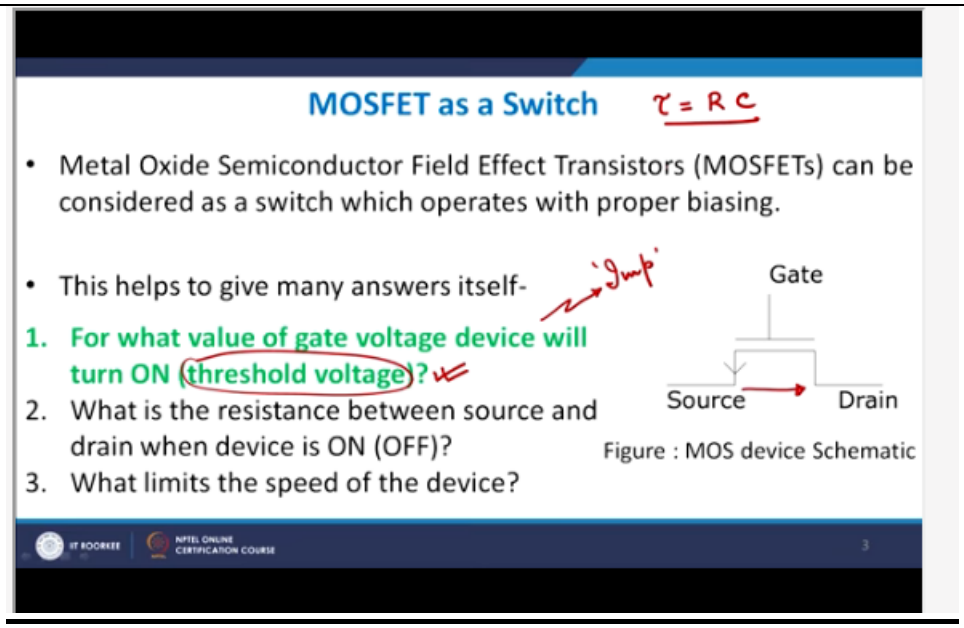
Course:	**VLSI**	**USN:**	**4AL16EC061**
Topic:	**CMOS INVERTER BASICS**	**Semester & Section:**	**8TH B**
Github Repository:	**Safiya-Courses**		





a CMOS circuit is composed of two MOSFETs. The top FET (MP) is a PMOS type device while the bottom FET (MN) is an NMOS type. The body effect is not present in either device since the body of each device is directly connected to the device's source. Both gates are connected to the input line. The output line connects to the drains of both FETs.

Take a look at the VTC in Figure 2. The curve represents the output voltage taken from node 3. You can easily see that the CMOS circuit functions as an inverter by noting that when VIN is five volts, VOUT is zero, and vice versa. Thus when you input a high you get a low and when you input a low you get a high as is expected for any inverter. You might be wondering what happens in the middle, transition area of the curve. You might also be curious as to what modes of operation the MOSFETs are in. We will look at these issues next.

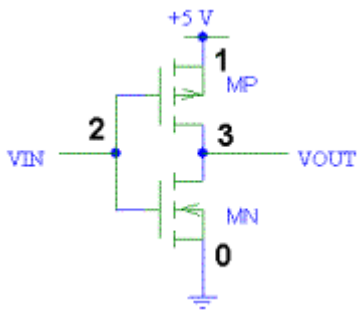


Figure 1: CMOS Inverter

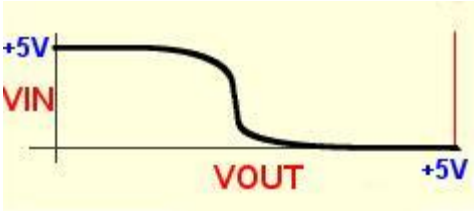


Figure 2: Basic Voltage Transfer Characteristic

DC Analysis

Figure 3 shows a more detailed VTC. Before we begin our analysis it is important to mention three items.

- The MOSFETS must be perfectly matched for optimum operation, that is, they must have the same threshold voltage magnitude and conduction parameter.
- The drain current (ID) through the NMOS device equals the drain current through the PMOS device at all times. MOSFET gates have a high input impedance and we assume the circuit's output sees no significant loading.
- VDD equals the voltage across the PMOS plus the voltage across the NMOS by KVL.

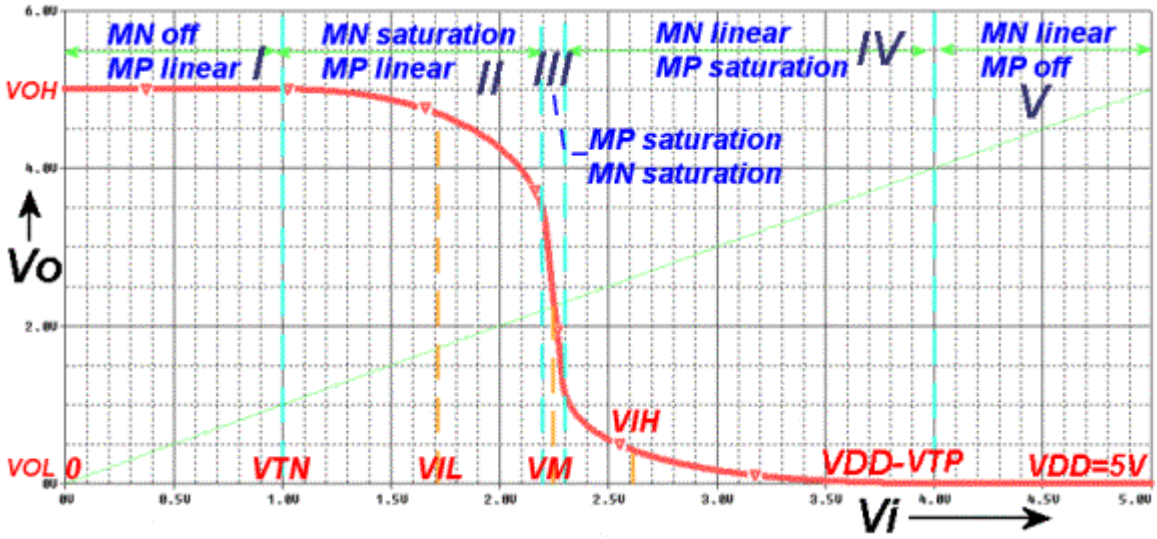


Figure 3: VTC with Input Signal

Region I

First we focus our attention on **region I**. In this case when we apply an input voltage between 0 and VTN. The PMOS device on since a low voltage is being applied to it. The NMOS is already negative enough and has no use for more free electrons so it refuses to conduct and turns into a large resistor. Since the NMOS device is on vacation, there is no current flow through either device. VDD is available at the Vo terminal since no current is going through the PMOS device and thus no voltage is being dropped across it.

- The PMOS device is forward biased (VSG > -VTP) and therefore on. This MOSFET is in the linear region (VSD<=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is cut off since the input voltage is below VTN (Vi=VGS<VTN).
- The power dissipation is zero.

Region II

Here we raise the input voltage above VTN. We find that the PMOS device remains in the linear region since it still has adequate forward bias. The NMOS turns on and jumps immediately into saturation since it still has a relatively large VDS across it.

- The PMOS device is in the linear region (VSD<=VSG+VTP).
- The NMOS device is in the saturation region (Vi=VDS>=VGS-VTN=Vo-VTN).
- Current now flows through both devices. Power dissipation is no longer zero.

The maximum allowable input voltage at the low logic state (**VIL**) occurs in this region. VIL is the value of Vi at the point where the slope of the VTC is -1. Put another way, VIL occurs at (dVo/dVi)=-1.

Region III

In the middle of this region there exists a point where Vi=Vo. We label this point VM and identify it as the gate threshold voltage. The voltage dropped across the NMOS device equals the voltage dropped across the PMOS device when the input voltage is VM. For a very short time, both devices see enough forward bias voltage to drive them to saturation.

- The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is in the saturation region (VDS>=VGS-VTN=Vo-VTN).
- Power dissipation reaches a peak in this region, namely at where VM=Vi=Vo.

Region IV

Region IV occurs between an input voltage slightly higher than VM but lower than VDD-VTP. Now the NMOS device is conducting in the linear region, dropping a low voltage across VDS. Since VDS is relatively low, the PMOS device must pick up the tab and drop the rest of the voltage (VDD-VDS) across its VSD junction. This, in turn, drives the PMOS into saturation. This region is effectively the reverse of region II.

- The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN=Vo-VTN).

The minimum allowable input voltage at the logic high state (**VIH**) occurs in this region. VIH occurs at the point where the slope of the VTC is –1 (dVo/dVi)=-1.

Region V

The NMOS wants to conduct but its drain current is severely limited due to the PMOS device only letting through a tiny leakage current. The PMOS is out to lunch since it is seeing a positive drive but it is already positive enough and has no use for more. This drain current let through by the PMOS is too small to matter in most practical cases so we let ID=0. With this information we can conclude that VDS=Vo=0 V for the NMOS since no current is going through the device. We have, in effect, sent in VDD and found the inverter's output to be zero volts. **For CMOS inverters,**

VOH=VDD. VOL is defined to be the output voltage of the inverter at an input voltage of VOH. We have just proven that **VOL=0**.

- The PMOS device is cut off when the input is at VDD (VSG=0 V).
- The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN).
- The total power dissipation is zero just as in region I.

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