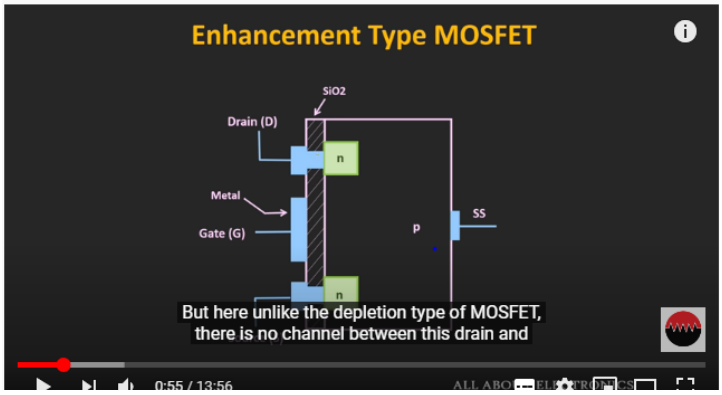
REPORT ON VLSI

Date:	**9/06/2020**	**Name:**	**SAFIYA BANU**
Course:	**VLSI**	**USN:**	**4AL16EC061**
Topic:	1. MOSFET - Enhancement Type MOSFET Explained (Construction, Working and Characteristics Explained) 2. GATE 2009 and 20121 ECE operating region and output voltage of CMOS inverter given 3. MOSFET vth based problems 4. MOSFET problems and solutions 5. TRICK to implement 4:1 mux using TRANSMISSION GATE & PASS TRANSISTOR LOGIC 6. MOSFET Drain current - graph , formulae & sums (cutoff,linear& saturation) 7. Realization of logic function using Multiplexer	**Semester & Section:**	**8TH B**
Github Repository:	**Safiya-Courses**		

FORENOON SESSION DETAILS
MOSFET - Enhancement Type MOSFET Explained (Construction, Working and Characteristics Explained)



MOSFET

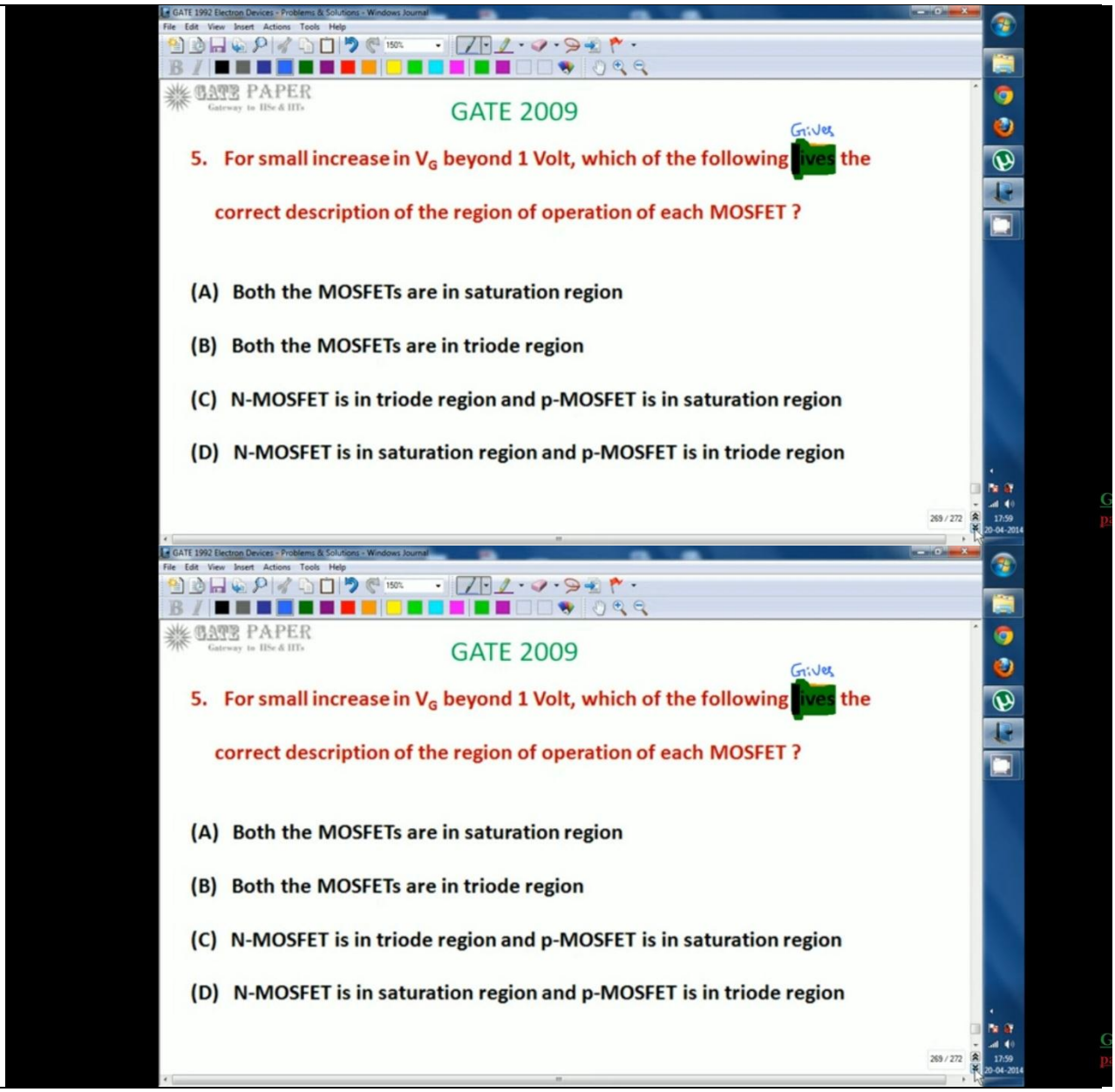
In case of JFET, the gate must be reverse biased for proper operation of the device i.e. it can only have negative gate operation for n-channel and positive gate operation for p-channel. That means we can only decrease the width of the channel from its zero-bias size.

TYPES

1. Depletion-type MOSFET or D-MOSFET: The D-MOSFET can be operated in both depletion mode and the enhancement mode. For this reason it is also called depletion/enhancement MOSFET.

2. Enhancement-type MOSFET or E-MOSFET: The E-MOSFET can be operated only in enhancement mode.

GATE 2009 and 20121 ECE operating region and output voltage of CMOS inverter given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5. For small increase in V_G beyond 1 Volt, which of the following gives the correct description of the region of operation of each MOSFET ?
(A) Both the MOSFETs are in saturation region
(B) Both the MOSFETs are in triode region
(C) N-MOSFET is in triode region and p-MOSFET is in saturation region
(D) N-MOSFET is in saturation region and p-MOSFET is in triode region
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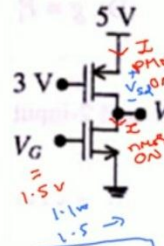
$V_{tn} = |V_{tp}| = 1$ volt, $\beta_n = \beta_p = 1 mA/V^2$



$I_{Dn} = I_{Dp}$

$\frac{\beta}{2}(V_{GSn} - V_{tn})^2 = \frac{\beta}{2}\left[(V_{SG} - V_{tp})(V_{SD}) - \frac{V_{SD}^2}{2}\right]$

$\frac{1}{2}(V_{Gn} - V_{Sn} - V_{tn})^2 = \left[(V_{Sp} - V_{Gp} - V_{tp})(V_{SD}) - \frac{V_{SD}^2}{2}\right]$

$\frac{1}{2}(1.5 - 0 - 1)^2 = \left[(5 - 3 - 1)(V_{SD}) - \frac{V_{SD}^2}{2}\right]$

$V_{SD} = 1 \pm \sqrt{3}/2$

$V_0 = 5 - V_{SD}$

$V_0 = 5 - (1 \pm \sqrt{3}/2)$ $\quad V_0 = 4 \mp \sqrt{3}/2 \Rightarrow$ $V_0 = 4 - \sqrt{3}/2 = 3.133$ volts ✓

$4 + \sqrt{3}/2 = 4.866$ volts

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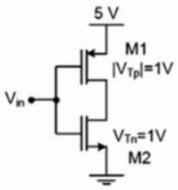
GATE 2012

1. In the CMOS circuit shown, electron and hole motilities are equal, and M1 and M2 are equally sized. The device M1 is in the linear region if



(A) $V_{in} < 1.875$ V

(B) $1.875 \text{ V} < V_{in} < 3.125$ V

(C) $V_{in} > 3.125$ V

(D) $0 < V_{in} < 5$ V

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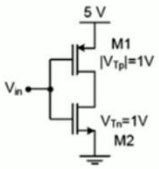

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(B) $1.875 \text{ V} < V_{in} < 3.125$ V

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(D) $0 < V_{in} < 5$ V

$V_0 > V_{in} - 1$

V_{in}	V_0
0 V	

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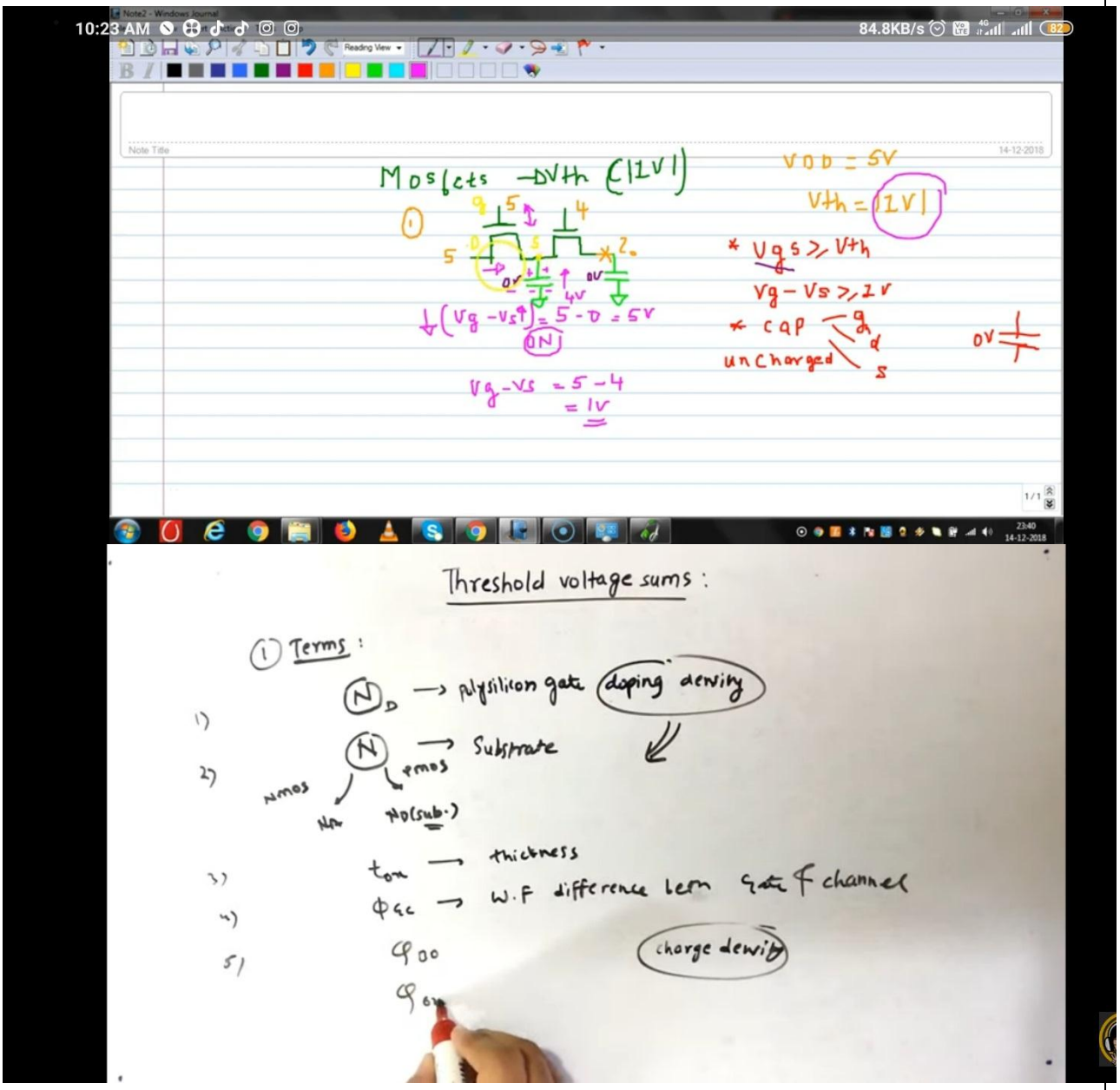
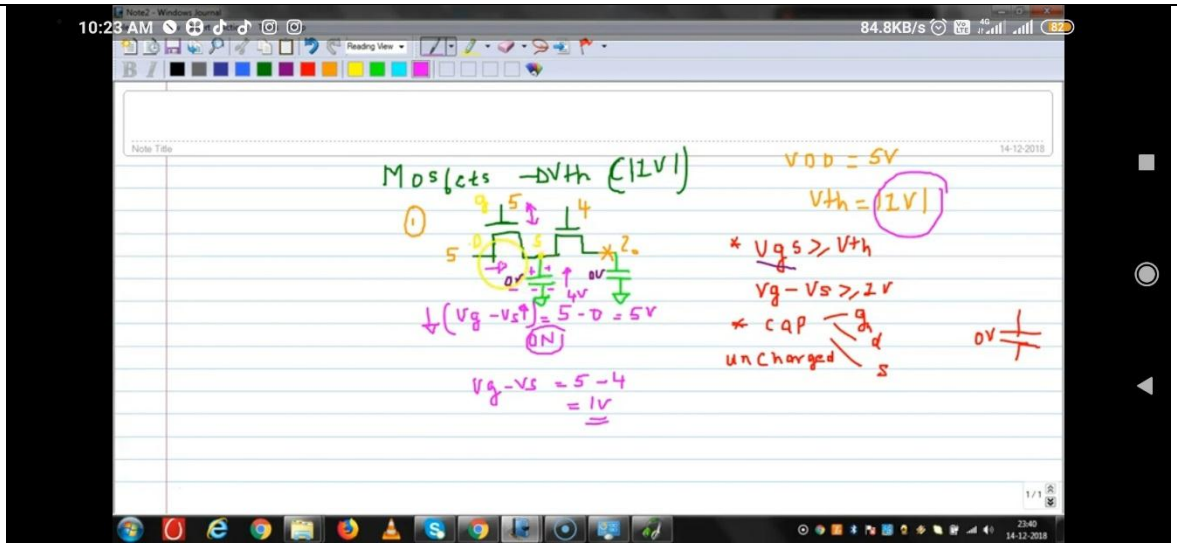
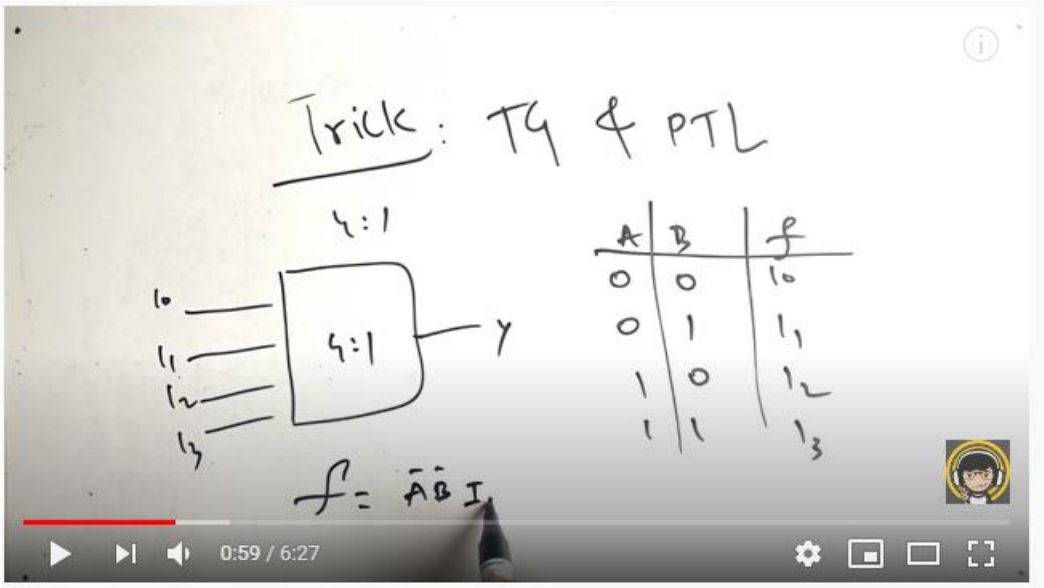
MOSFET vth based problems





TRICK to implement 4:1 mux using TRANSMISSION GATE & PASS TRANSISTOR LOGIC



TRICK to implement 4:1 mux using TRANSMISSION GATE & PASS TRANSISTOR LOGIC

4-1-multiplexer_using_CMOS_logic | Pass-Transistor-Logic

4:1 multiplexer using CMOS logic The path selector logic Boolean expression can be given as :

Out = AS + B––S

When the select line signal S is high A is passed to the output and when S is low B is passed to the output. The same logic is used for 4 : 1 MUX in which number of inputs are four (A, B, C, D) and the number of select lines are two (S1, S2). The Boolean expression for 4 : 1 MUX can be given as :

Out = A (S1 · S2) + B (S1 · ––S2) + C (––S1 · S2) + D (––S1 · ––S2)

The above Boolean expression can be used to implement 4 : 1 multiplexer or 1 : 4 demultiplexer. The above logic can be generalised as :

2m = n

Where n is the number of inputs in case of MUX (outputs in case of DEMUX) and m is the number of control lines.

4 : 1 MUX using CMOS logic

The implementation of 4 : 1 MUX using CMOS logic is shown in Figure below.

4 : 1 MUX using transmission gates

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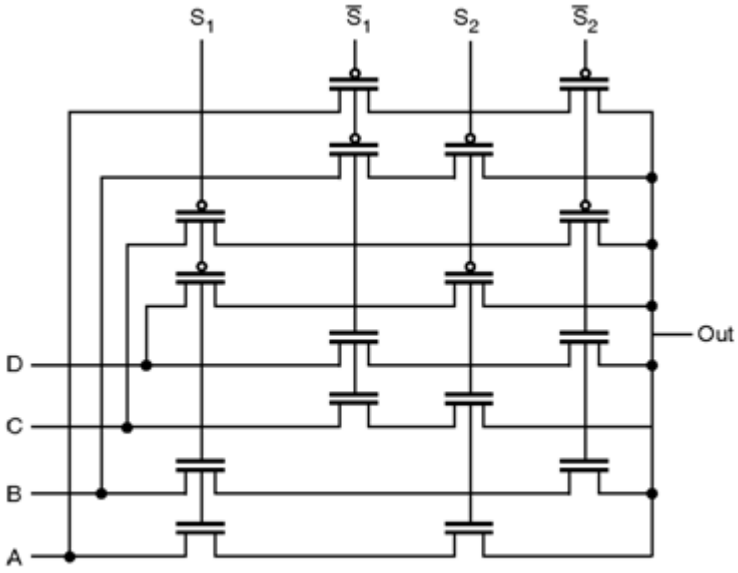
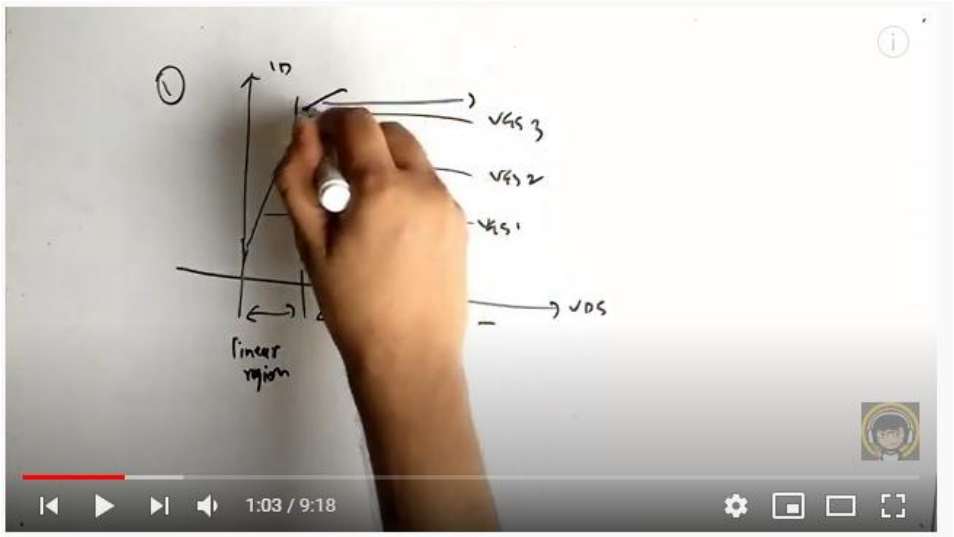
Figure below.



4 : 1 MUX using CMOS logic

4 : 1 MUX using pass transistor log

MOSFET Drain current - graph , formulae & sums (cutoff,linear& saturation)



MOSFET Drain current - graph , formulae & sums (cutoff,linear& saturation)

In general, any MOSFET is seen to exhibit three operating regions viz.,

1. Cut-Off Region
   Cut-off region is a region in which the MOSFET will be OFF as there will be no current flow through it. In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.
2. Ohmic or Linear Region
   Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.
3. Saturation Region
   In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

MOSFET DRAIN GRAPH

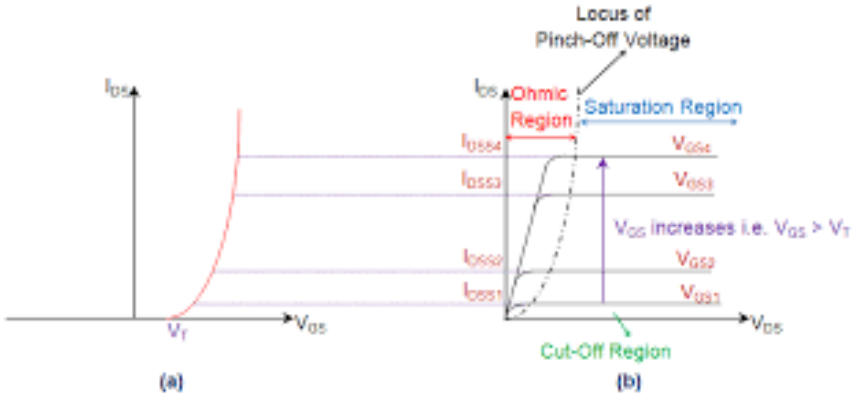
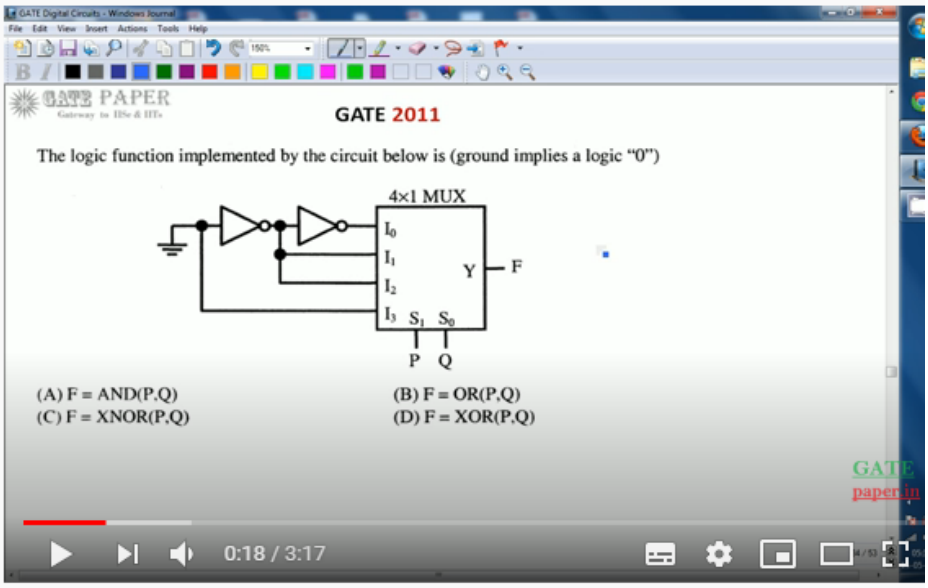


Figure 1 n-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Realization of logic function using Multiplexer



GATE 2011 ECE Realization of logic function using Multiplexer

It is a combinational circuit which have many data inputs and single output depending on control or select inputs. For N input lines, log n (base2) selection lines, or we can say that for 2^n input lines, n selection lines are required. Multiplexers are also known as "Data n selector, parallel to serial convertor, many to one circuit, universal logic circuit". Multiplexers are mainly used to increase amount of the data that can be sent over the network within certain amount of time and bandwidth.