

REPORT ON VLSI

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Topic:	Digital VLSI Design Virtual lab Experiments: 1. Logic gates 2. 4:1 Mux 3. MOSFET 4. CMOS Inverter	Semester & Section:	8TH B
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Digital VLSI Design Virtual lab



MOSFET

To plot the (i) output characteristics & (ii) transfer characteristics of an n-channel and p-channel MOSFET.



CMOS Inverter

To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.



Ring Oscillator

To design and plot the output characteristics of a 3-inverter ring oscillator.



Logic Gates

To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.



4x1 Multiplexer

To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.



Latches

To design and plot the characteristics of a positive and negative latch based on multiplexers.



Registers

To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.

MOSFET

The aim of this experiment is to plot (i) the output characteristics and, (ii) the transfer characteristics of an n-channel and p-channel MOSFET.

Introduction

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a transistor used for amplifying or switching electronic signals. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type, and is accordingly called an nMOSFET or a pMOSFET. Figure 1 shows the schematic diagram of the structure of an nMOS device before and after channel formation.

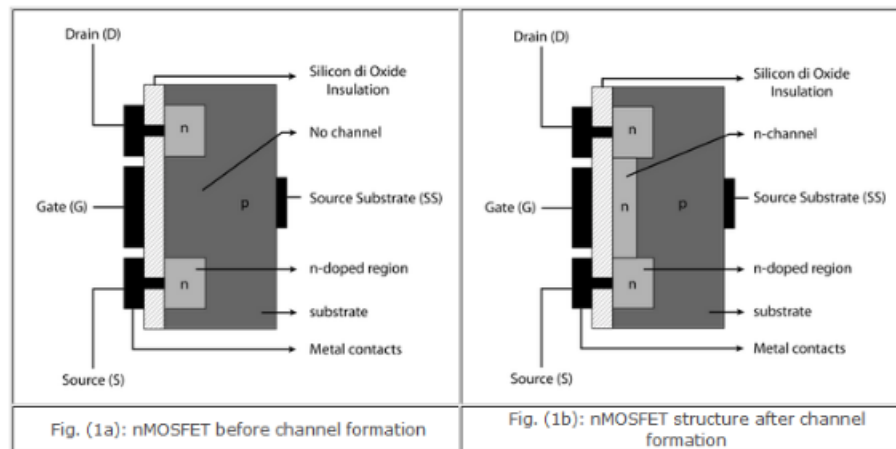
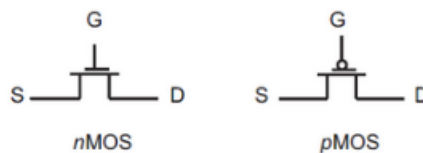


Figure 2 shows symbols commonly used for MOSFETs where the bulk terminal is either labeled (B) or implied (not drawn).



Output Characteristics

MOSFET output characteristics plot I_D versus V_{DS} for several values of V_{GS} .

The characteristics of an nMOS transistor can be explained as follows. As the voltage on the top electrode increases further, electrons are attracted to the surface. At a particular voltage level, which we will shortly define as the threshold voltage, the electron density at the surface exceeds the hole density. At this voltage, the surface has inverted from the p-type polarity of the original substrate to an n-type inversion layer, or inversion region, directly underneath the top plate as indicated in Fig. 1(b). This inversion region is an extremely shallow layer, existing as a charge sheet directly below the gate. In the MOS capacitor, the high density of electrons in the inversion layer is supplied by the electron–hole generation process within the depletion layer. The positive charge on the gate is balanced by the

combination of negative charge in the inversion layer plus negative ionic acceptor charge in the depletion layer. The voltage at which the surface inversion layer just forms plays an extremely important role in field-effect transistors and is called the threshold voltage V_{tn} . The region of output characteristics where $V_{GS} < V_{tn}$ and no current flows is called the cut-off region. When the channel forms in the nMOS (pMOS) transistor, a positive (negative) drain voltage with respect to the source creates a horizontal electric field moving the electrons (holes) toward the drain forming a positive (negative) drain current coming into the transistor. The positive current convention is used for electron and hole current, but in both cases electrons are the actual charge carriers. If the channel horizontal electric field is of the same order or smaller than the vertical thin oxide field, then the inversion channel remains almost uniform along the device length. This continuous carrier profile from drain to source puts the transistor in a bias state that is equivalently called either the non-saturated, linear, or ohmic bias state. The drain and source are effectively short-circuited. This happens when $V_{GS} > V_{DS} + V_{tn}$ for nMOS transistor and $V_{GS} < V_{DS} + V_{tp}$ for pMOS transistor. Drain current is linearly related to drain-source voltage over small intervals in the linear bias state.

But if the nMOS drain voltage increases beyond the limit, so that $V_{GS} < V_{DS} + V_{tn}$, then the horizontal electric field becomes stronger than the vertical field at the drain end, creating an asymmetry of the channel carrier inversion distribution shown in Figure 4.

Transfer Characteristics

The transfer characteristic relates drain current (I_D) response to the input gate-source driving voltage (V_{GS}). Since the gate terminal is electrically isolated from the remaining terminals (drain, source, and bulk), the gate current is essentially zero, so that gate current is not part of device characteristics. The transfer characteristic curve can locate the gate voltage at which the transistor passes current and leaves the OFF-state. This is the device threshold voltage (V_{tn}). Figure 5 shows measured input characteristics for an nMOS and pMOS transistor with a small 0.1V potential across their drain to source terminals.

The transistors are in their non-saturated bias states. As V_{GS} increases for the nMOS transistor in Figure 5a, the threshold voltage is reached where drain current elevates. For V_{GS} between 0V and 0.7V, I_D is nearly zero indicating that the equivalent resistance between the drain and source terminals is extremely high. Once V_{GS} reaches 0.7V, the current increases rapidly with V_{GS} indicating that the equivalent resistance at the drain decreases with increasing gate-source voltage. Therefore, the threshold voltage

of the given nMOS transistor is about $V_{th} \approx 0.7V$. The pMOS transistor input characteristic in Figure 5b is analogous to the nMOS transistor except the I_D and V_{GS} polarities are reversed.

CMOS INVERTER

The aim of this experiment is to design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.

Introduction

The inverter is universally accepted as the most basic logic gate doing a Boolean operation on a single input variable. Fig.1 depicts the symbol, truth table and a general structure of a CMOS inverter. As shown, the simple structure consists of a combination of an pMOS transistor at the top and a nMOS transistor at the bottom.

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor**. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices.

Inverter Static Characteristics (VTC)

Digital inverter quality is often measured using the Voltage Transfer Curve (VTC), which is a plot of input vs. output voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained.

Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between on and off - but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts. The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching. The tolerance to noise can be measured by comparing the minimum input to the maximum output for each region of operation (on / off).

Noise margin : is a parameter intimately related to the transfer characteristics. It allows one to estimate the allowable noise voltage on the input of a gate so that the output will not be affected. Noise margin (also called noise immunity) is specified in terms of two parameters - the low noise margin N_L , and the high noise margin N_H . Referring to above figure, N_L is defined as the difference in magnitude between the maximum LOW input voltage recognized by the driven gate and the maximum LOW output voltage of the driving gate. That is, $N_L = |V_{IL} - V_{OL}|$. Similarly, the value of N_H is the difference in magnitude between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognizable by the driven gate. That is, $N_H = |V_{OH} - V_{IH}|$. Where V_{IH} : minimum HIGH input voltage, V_{IL} : maximum LOW input voltage, V_{OH} : minimum HIGH output voltage, V_{OL} : maximum LOW output voltage.

Inverter Dynamic Characteristics

Rise Time (t_r) : Time taken to rise from 10% to 90%.

Fall Time (t_f): Time taken to fall from 90% to 10%

Edge Rate (t_{rf}): $(t_r + t_f)/2$.

High-to-Low propagation delay (t_{pHL}): Time taken to fall from V_{OH} to 50%.

Low-to-High propagation delay (t_{pLH}): Time taken to rise from 50% to V_{OL} .

Propagation Delay (t_p): $(t_{pHL} + t_{pLH})/2$.

Contamination Delay (t_{cd}): Minimum time from the input crossing 50% to the output crossing 50%

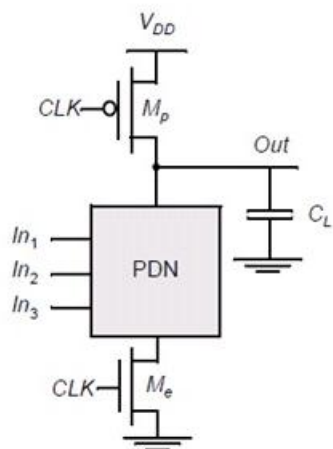
LOGIC GATES

The aim of this experiment is to design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR gates based on CMOS static logic.

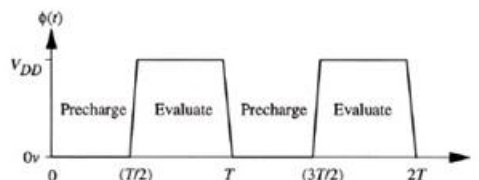
Introduction

Static logic is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low-impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that, one and only one of these networks is conducting in the steady state.

Dynamic logic is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. The basic construction of a dynamic logic gate is shown in fig.2. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.



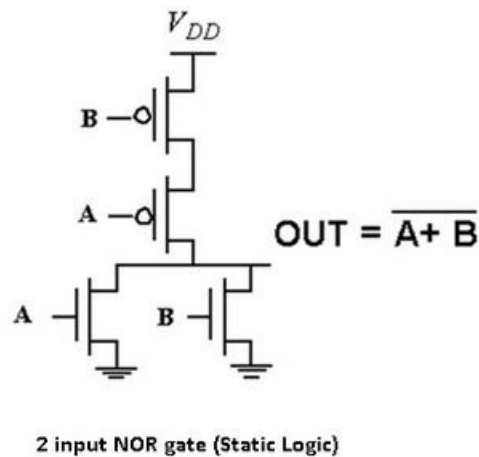
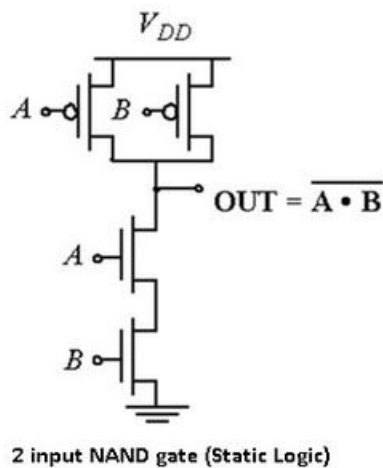
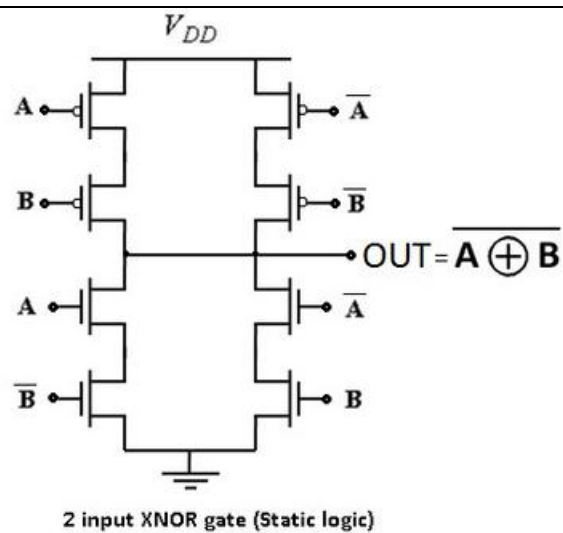
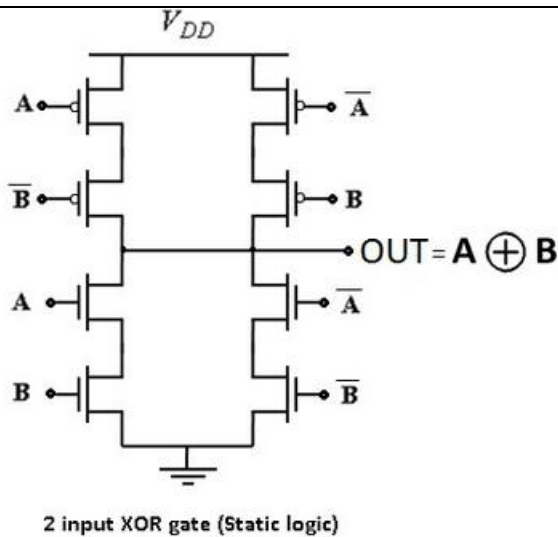
Phase	Clk	Inputs	Outputs
Precharge	Low	Don't care	High
Evaluation	High	Valid	Valid



Precharge: When $CLK = 0$, the output node Out is precharged to V_{DD} by the PMOS transistor M_p . During that time, the evaluate NMOS transistor M_e is off, so that the pull-down path is disabled. The evaluation FET eliminates any static power that would be consumed during the precharge period (this is, static current would flow between the supplies if both the pulldown and the precharge device were turned on simultaneously).

Evaluation: For $CLK = 1$, the precharge transistor M_p is off, and the evaluation transistor M_e is turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between Out and GND and the output is discharged to GND. If the PDN is turned off, the precharged value remains stored on the output capacitance C_L , which is a combination of junction capacitances, the wiring capacitance, and the input capacitance of the fan-out gates. During the evaluation phase, the only possible path between the output node and a supply rail is to GND. Consequently, once Out is discharged, it cannot be charged again till then next precharge operation. The inputs to the gate can therefore make at most one transition during evaluation.

Static Logic Design of NAND, NOR, XOR and XNOR Gates



In order to design 2-input NAND, NOR, XOR and XNOR gates for equal rise and fall time, it is necessary to first design an inverter with equal rise and fall time. This involves compensating for the difference in electron and hole mobilities. For silicon material, the electron mobility is about 2.5 to 3 times greater than the hole mobility. Therefore, to have equal rise and fall time in an inverter, we must choose the W/L ratio of pMOS as 2.5 times greater than that of the nMOS transistor. After performing this task, we need to size the transistors of each gate under worst case conditions (of input combination) for charging and discharging resistances R_c and R_d . (In every gate circuit, the PUN provides maximum ON resistance for rise time and the PDN provides maximum ON resistance for fall time.) For a NAND gate, the worst case charging corresponds to an input combination where only one of the pMOS is ON and discharging takes place only when both nMOS' are turned ON. i.e. in the worst case, $R_c/R_d=1/2$. Thus, in order to equalize both currents (considering also the mobility differences), we must have

$(W/L)_p = (2.5 \times 2)(W/L)_n$. This can be achieved in a 180nm technology by choosing $W_n = 0.18 \mu\text{m}$ and $W_p = 0.90 \mu\text{m}$. Similarly in case of a NOR gate, $(W/L)_p$ must be equal to $(2.5 \times 0.5)(W/L)_n$ which can be achieved by taking $W_n = 0.36 \mu\text{m}$ and $W_p = 0.45 \mu\text{m}$. For XOR and XNOR gates, worst case R_c/R_d ratio is equal to one. Therefore, $(W/L)_p$ must be equal to $(2.5 \times 1)(W/L)_n$ for both gates.

4:1 MUX

The aim of this experiment is to design and plot the characteristics of a 4x1 digital multiplexer using pass transistor and transmission gate logic.

Introduction

A multiplexer or mux is a combinational circuits that selects several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n selected lines, are used to select which input line to send to the output.

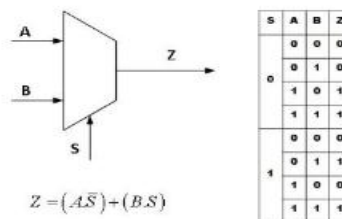


Fig.1: The schematic diagram, boolean equation and the truth table of a 2:1 multiplexer with inputs A and B, select input S and the output Z.

Figure 2 shows how a 4:1 MUX can be constructed out of two 2:1 MUXs.

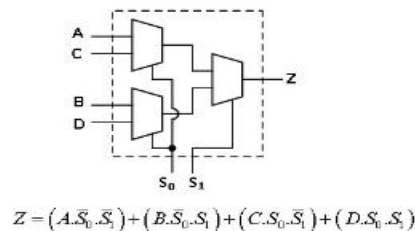


Figure 2 shows how a 4:1 MUX can be constructed out of two 2:1 MUXs.

Design using pass-transistor logic

A multiplexer can be designed using various logics. Fig.3 shows how a 2:1 MUX is implemented using a pass-transistor logic.

The pass-transistor logic attempts to reduce the number of transistors to implement a logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The implementation of a 2:1 MUX requires 4 transistors (including the inverter required to invert S), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

Design using transmission gate logic

A transmission gate is an electronic element and good non mechanical relay built with CMOS technology. It is made by parallel combination of nMOS and pMOS transistors with the input at the gate of one transistor (C) being complementary to the input at the gate () of the other.

The transmission gate acts as a bidirectional switch controlled by the gate signal C. When $C=1$, both MOSFETs are on, allowing the signal to pass through the gate. In short, $A=B$, if $C=1$. On the other hand, $C=0$, places both transistors in cut-off, creating an open circuit between nodes A and B. Fig.5 shows the implementation of a 2:1 MUX using transmission gate logic.

Here, the transmission gates selects input A or B on the basis of the value of the control signal S. When $S=0$, $Z=A$ and when $S=1$, $Z=B$.