

REPORT ON VLSI

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Course:	VLSI	USN:	4AL16EC061
Topic:	MOS transistor basics-II MOS transistor basics-III	Semester & Section:	8 TH B
Github Repository:	Safiya-Courses		

FORENOON SESSION DETAILS

- We assume the ONSET of inversion takes place at $V_{GS} = V_{TH}$. So, the inversion charge density is proportional to $V_{GS} - V_{TH}$, i.e.

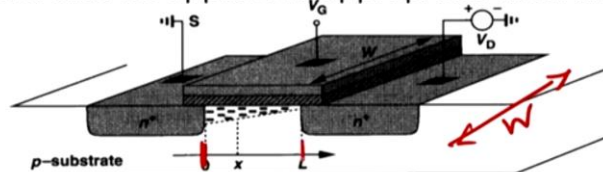
$$Q = WC_{OX}(V_{GS} - V_{TH})$$

$(V_{GS} - V_{TH})$ ← charge/length

nmos enhance
 $V_{th} = 0.5V$

with W be the width of the device and C_{OX} being the gate oxide (per unit area)

- Next, consider that we applied an appropriate drain bias.



Source: B. Razavi, "Design of Analog CMOS Integrated Circuit," McGraw-Hill Education Pvt. Ltd., 2002.

$V_{ds} > V_{th}$
 $1V$
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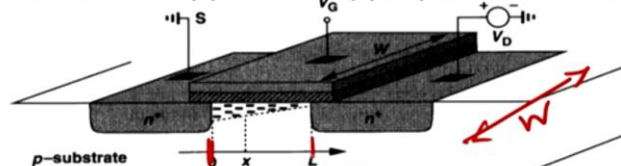
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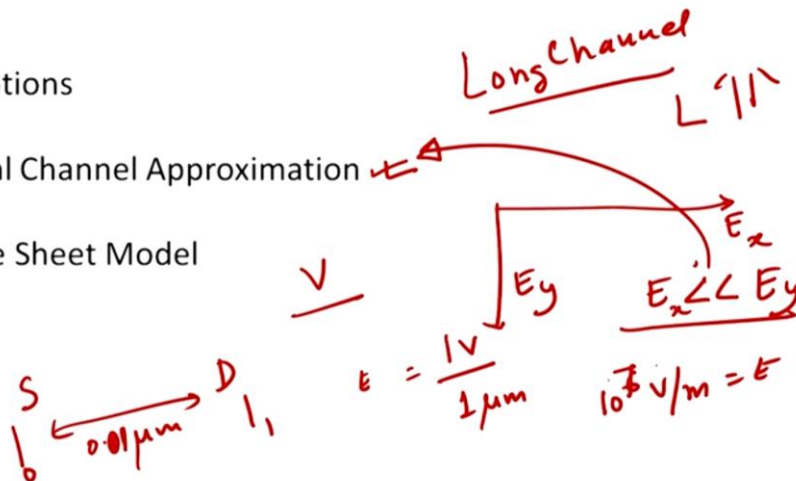
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Assumptions

- Gradual Channel Approximation

- Charge Sheet Model



- Outline
- Short Channel Effects ←
 - Second Order Effects ✓
 - Body Effect →
 - Channel Length Modulation →
 - Types of Device Scaling
 - Velocity Saturation ✓
 - Drain Induced Barrier Lowering (DIBL)
 - Punchthrough →
 - Model for manual analysis
 - Basic Equations to be remembered
 - Recapitulation



Short Channel Effects

- ☐ What if the device dimension is reduced?
- **Moore's Law**-In 1965, Gordon **Moore** postulated that the number of transistors per unit area on integrated circuits will double every 18 months. **Moore's law** predicts that this trend will continue into the foreseeable future.
- ☐ What beyond the Moore's law?



SHORT CHANNEL EFFECT

Short-channel effects occur when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. In MOSFETs, channel lengths must be greater than the sum of the drain and source depletion widths to avoid edge effects. Otherwise, a number of effects appear.

Among the reported effects cited by a number of researchers at universities around the globe are:

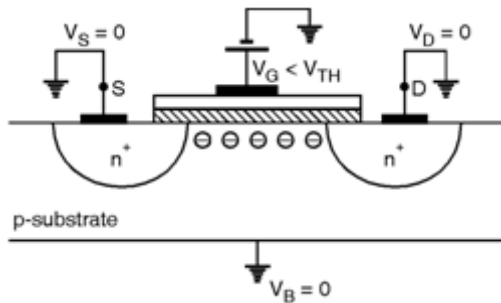
1. "Off-state" leakage current.

2. Impact ionization, in which a charge carrier can be affected by other charge carriers;
3. Velocity saturation/mobility degradation;

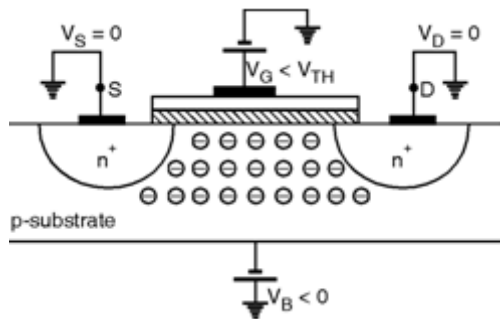
BODY EFFECT

In I-V analysis we assumed that the bulk and source of transistor were tied to ground, what happens if the bulk voltage of NMOS is drops below the source voltage ?

To understand this effect suppose $V_S = 0$ and $V_D = 0$ and V_G is somewhat less than V_{TH} so that depletion region is formed under the gate but inversion channel does not exist as shown in Figure below.



As V_B becomes more negative (i.e. $V_B < V_S$ where $V_S = 0$) more holes are attracted to the substrate connection leaving a larger negatively charged ions behind i.e. the depletion region becomes wider as shown in Figure below.



As we know that the threshold voltage is a function of the total charge in the depletion region (i.e. Q_{dep}). Thus as the body voltage V_B drops then depletion charge (Q_{dep}) increases which increases the threshold voltage (V_{TH}). This effect is called as the body effect or back gate effect.

When the body bias voltage V_{SB} is applied between source and body the surface potential required for strong inversion is increased and becomes $|2\phi_F + V_{SB}|$. The charge stored in the depletion region can now be expressed as :

$$Q_{dep} =$$

From the preceeding discussions it is clear that V_{SB} has an impact on the threshold voltage.

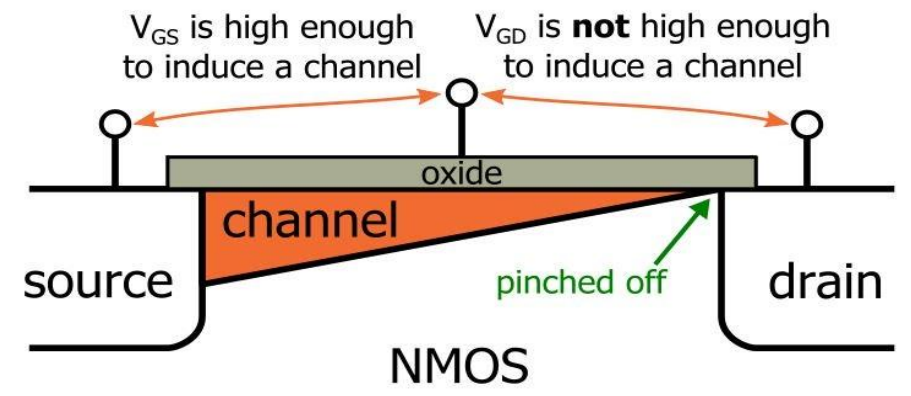
Thus the threshold voltage with body bias can be expressed as :

$$V_{TH} = V_{TH0} + g (-$$

Where V_{TH0} is given by Equation discussed in above Section

g = is the body effect coefficient.

CHANNEL LENGTH MODULATION



Analysis of MOSFET circuits is based on three possible operating modes: cutoff, triode (aka linear), and saturation. (The subthreshold region is a fourth mode, but we don't need to worry about that for this article.)

In cutoff, the gate-to-source voltage is not greater than the threshold voltage, and the MOSFET is inactive.

In triode, the gate-to-source voltage is high enough to allow current flow from drain to source, and the nature of the induced channel is such that the magnitude of the drain current is influenced by the gate-to-source voltage and the drain-to-source voltage. As the drain-to-source voltage increases, the triode region transitions to the saturation region, in which drain current is (ideally) independent of drain-to-source voltage and thus influenced only by the physical characteristics of the FET and the gate-to-source voltage.

The saturation-region relationship between gate-to-source voltage (V_{GS}) and drain current (I_D) is expressed as follows:

$$I_D = \frac{1}{2} \mu_n C_{ox} W L (V_{GS} - V_{TH})^2 \quad I_D = \frac{1}{2} \mu_n C_{ox} W L (V_{GS} - V_{TH})^2$$

The transition to saturation mode occurs because the channel gets “pinched off” at the drain end:

VELOCITY SATURATION

Saturation velocity is the maximum velocity a charge carrier in a semiconductor, generally an electron, attains in the presence of very high electric fields. When this happens, the semiconductor is said to be in a state of velocity saturation. Charge carriers normally move at an average drift speed proportional to the electric field strength they experience temporally. The proportionality constant is known as mobility of the carrier, which is a material property. A good conductor would have a high mobility value for its charge carrier, which means higher velocity, and consequently higher current values for a given electric field strength. There is a limit though to this process and at some high field value, a charge carrier can not move any faster, having reached its saturation velocity, due to mechanisms that eventually limit the movement of the carriers in the material.