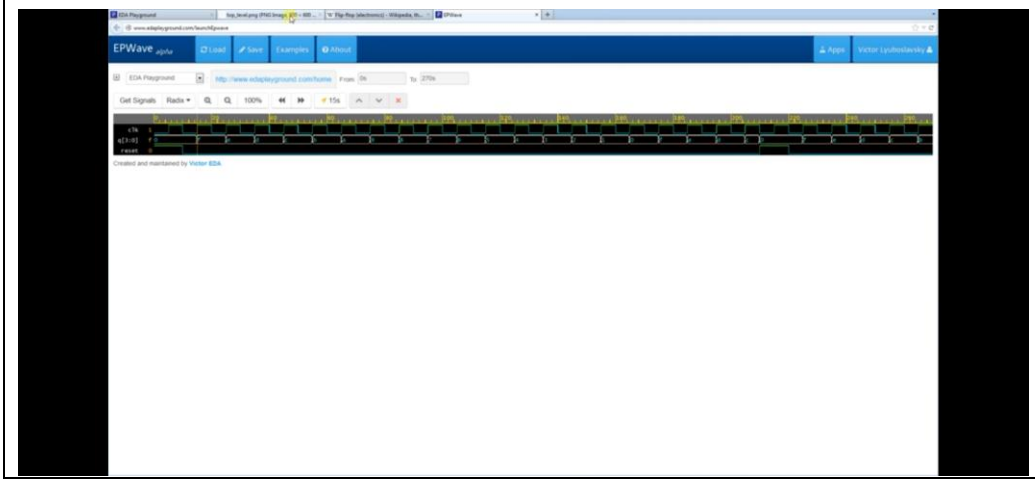
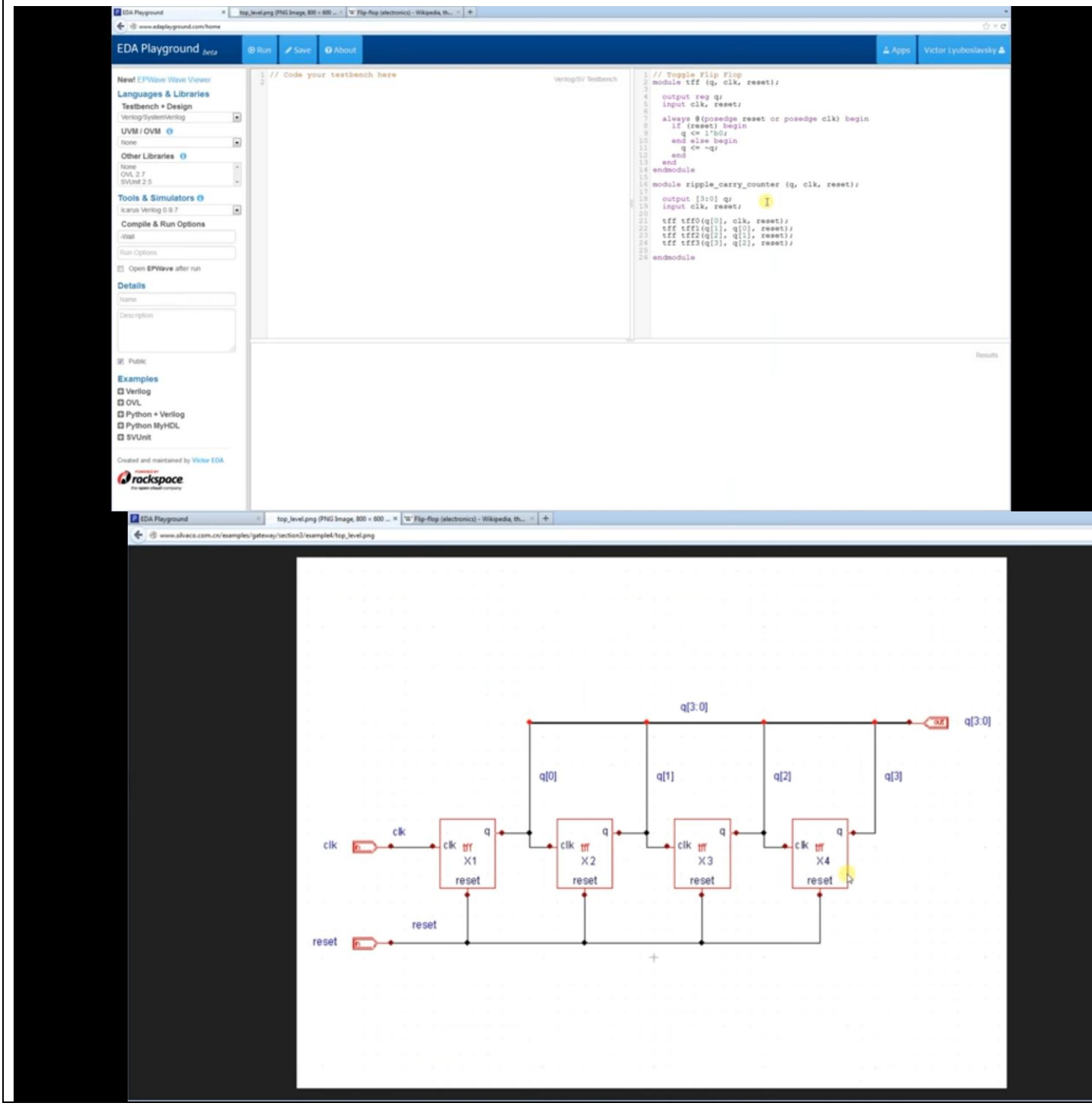
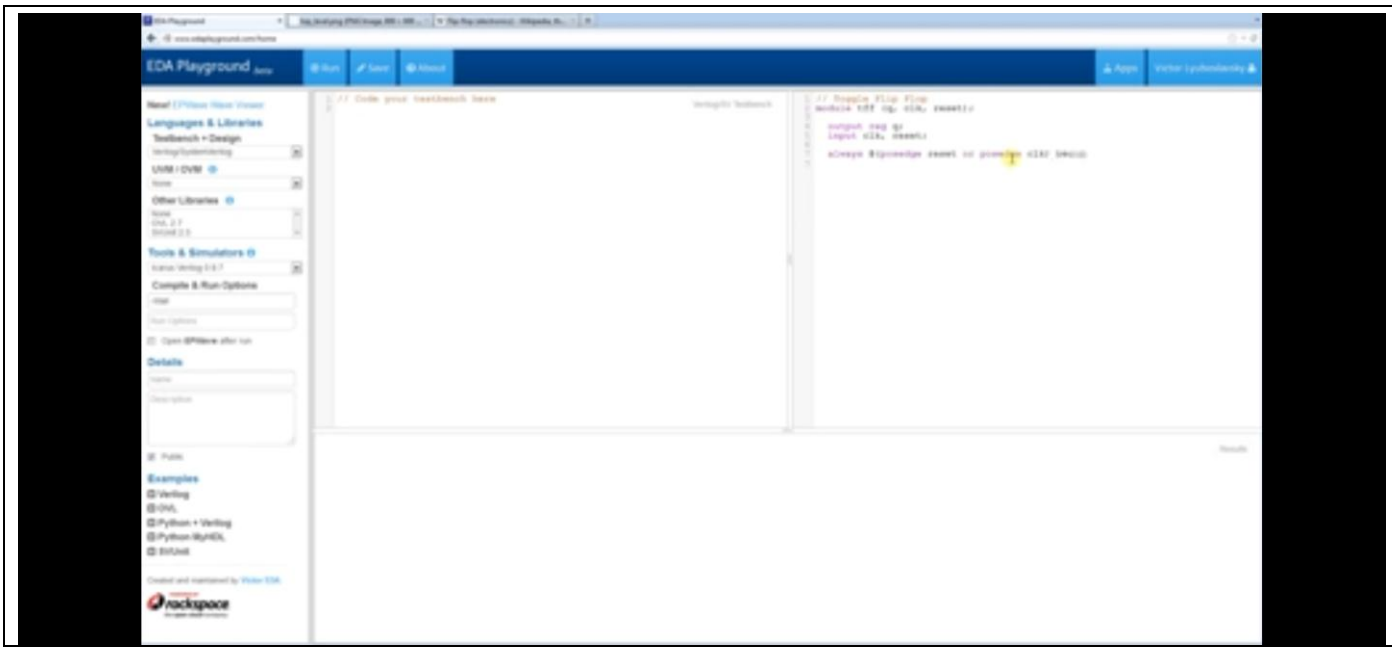
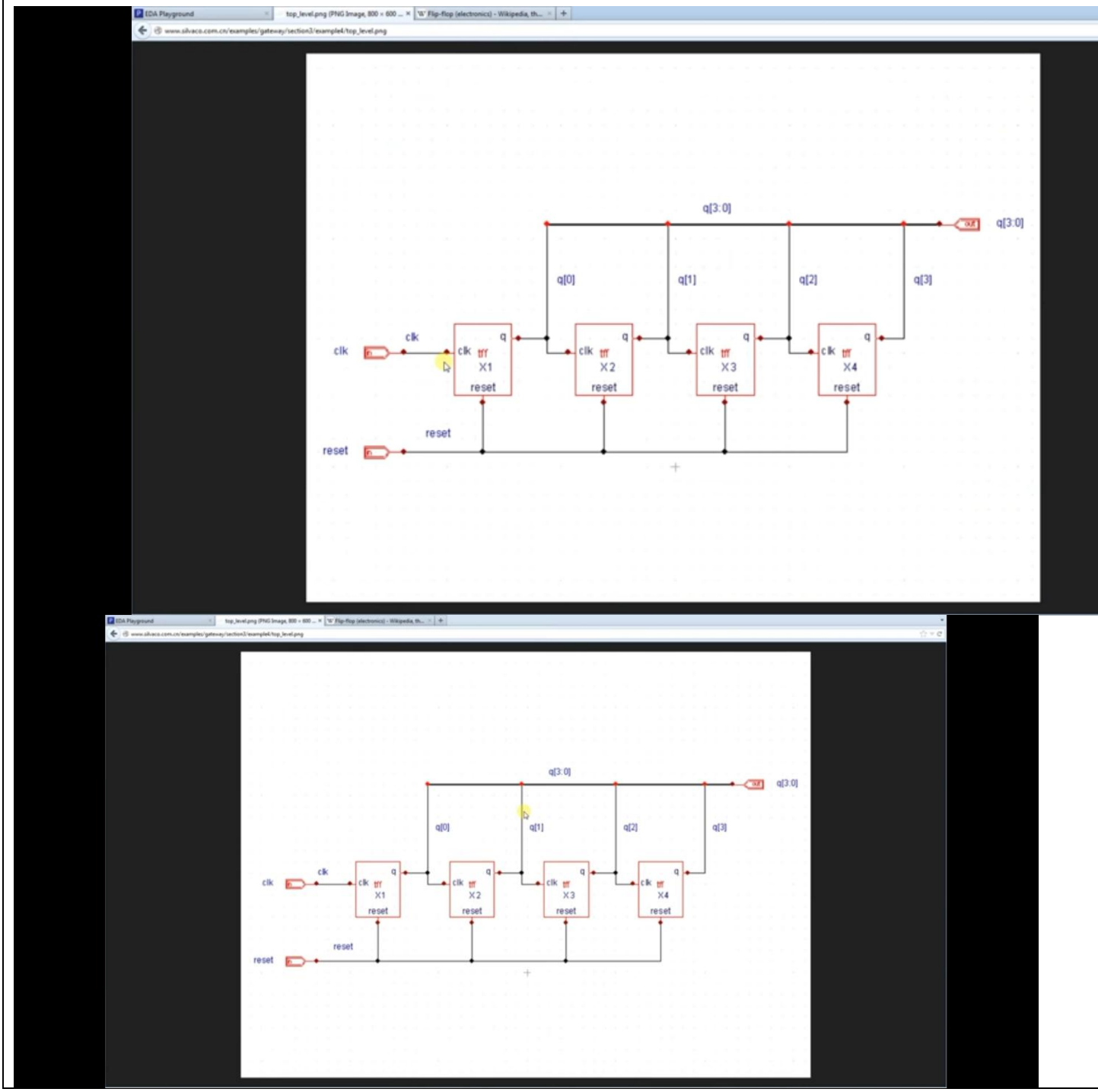
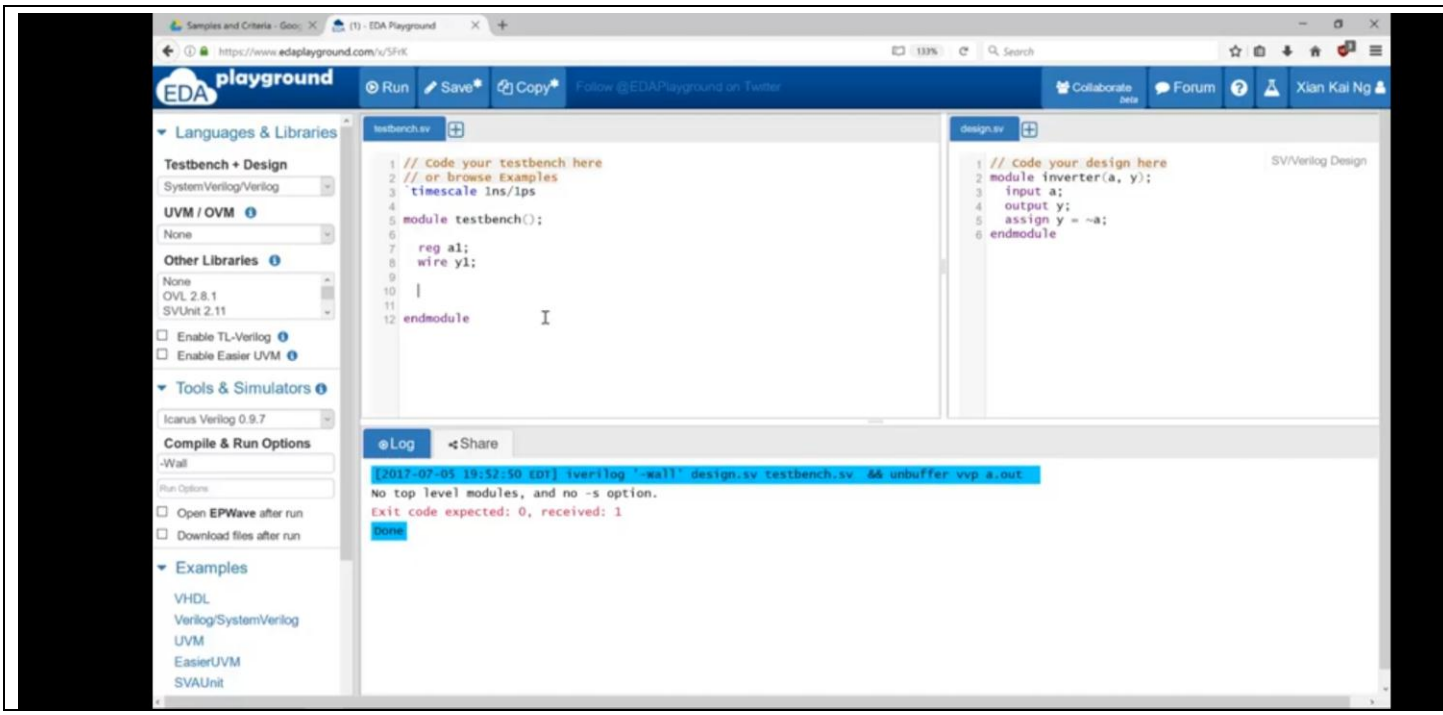
Date:	**03/6/2020**	**Name:**	**SAFIYA BANU**
Course:	**DIGITAL DESIGN USING HDL**	**USN:**	**4AL16EC061**
Topic:	**EDA Playground Online complier** **EDA Playground Tutorial Demo Video** **How to Download And Install Xilinx Vivado Design Suite**	**Semester & Section:**	**8th , B**
Github Repository:	**Safiya-Courses**		

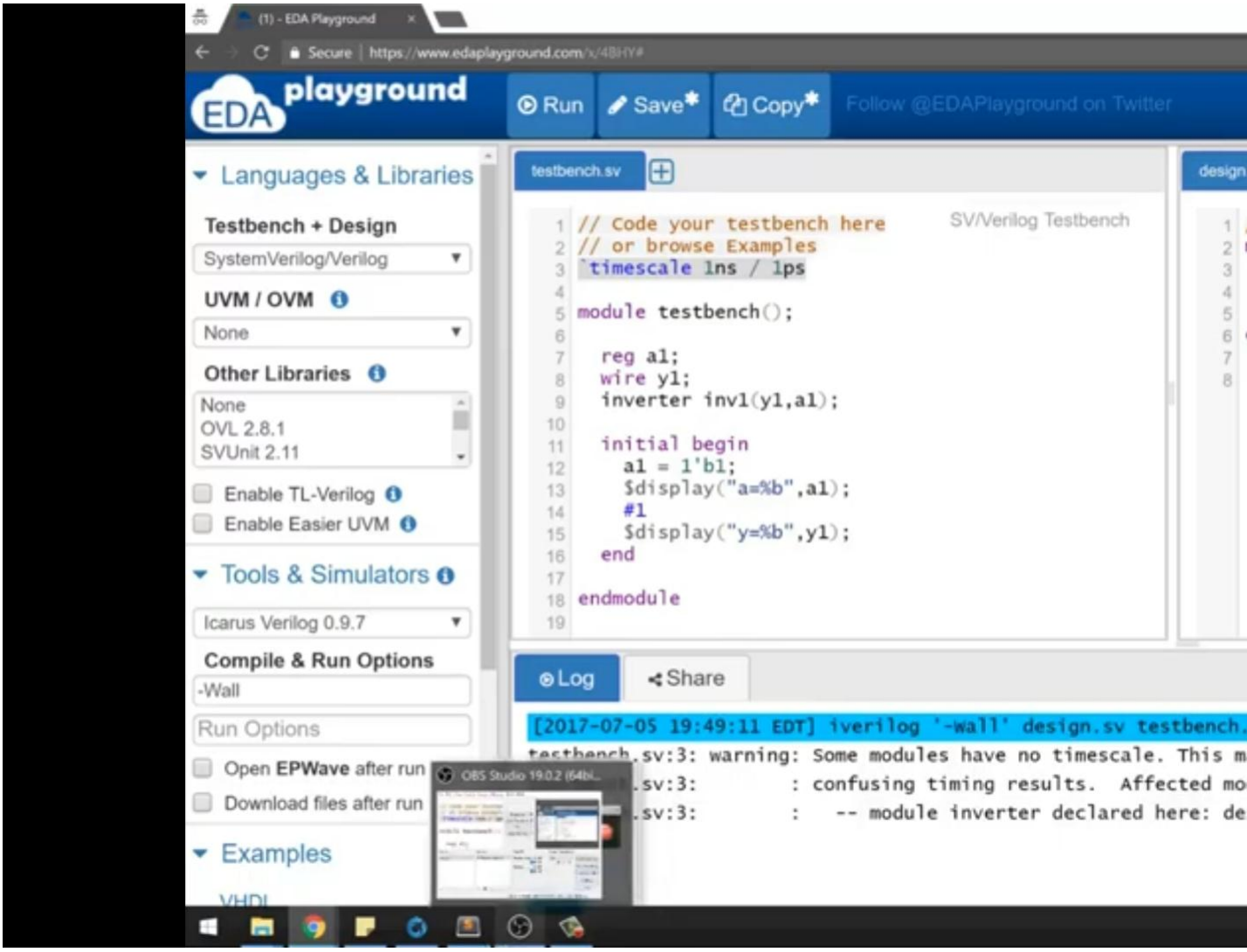



EDA Playground beta
Run
Save
About
Apps
Victor Lyuboslavsky
// Code your testbench here
// Toggle Flip Flop
module tff (q, clk, reset);
output reg q;
input clk, reset;
always @(posedge reset or posedge clk) begin
if (reset) begin
q <= 1'b0;
end else begin
q <= ~q;
end
end
endmodule
module ripple_carry_counter (q, clk, reset);
output [3:0] q;
input clk, reset;
tff tff0(q[0], clk, reset);
tff tff1(q[1], q[0], reset);
tff tff2(q[2], q[1], reset);
tff tff3(q[3], q[2], reset);
endmodule
Languages & Libraries
Tools & Simulators
Examples
Verilog
OVL
Python + Verilog
Python MyHDL
SVUnit
q[3:0]
q[0]
q[1]
q[2]
q[3]
clk
reset
X1
X2
X3
X4


EDA Playground
Run
Save
About
Apps
// Code your testbench here
// Toggle Flip Flop
Languages & Libraries
Testbench + Design
UVM / OVM
Other Libraries
Tools & Simulators
Compile & Run Options
Details
Examples
Verilog
OVL
Python + Verilog
Python MyHDL
SVUnit
rackspace


EDA Playground
top_level.png (PNG Image, 800 × 600 ...
Flip-flop (electronics) - Wikipedia, th...
www.silvaco.com.cn/examples/gateway/section3/example4/top_level.png
q[3:0]
q[3:0]
q[0]
q[1]
q[2]
q[3]
clk
clk
clk
q
clk
X1
reset
X2
X3
X4
reset
reset
reset


EDA playground
Run
Save
Copy
Follow @EDAPlayground on Twitter
Collaborate
Forum
Xian Kai Ng
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
Enable TL-Verilog
Enable Easier UVM
Tools & Simulators
Icarus Verilog 0.9.7
Compile & Run Options
-Wall
Open EPWave after run
Download files after run
Examples
VHDL
Verilog/SystemVerilog
UVM
EasierUVM
SVAUnit
testbench.sv
1 // Code your testbench here
2 // or browse Examples
3 `timescale 1ns/1ps
4
5 module testbench();
6
7 reg a1;
8 wire y1;
9
10
11
12 endmodule
design.sv
SV/Verilog Design
1 // Code your design here
2 module inverter(a, y);
3 input a;
4 output y;
5 assign y = ~a;
6 endmodule
Log
Share
[2017-07-05 19:52:50 EDT] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
No top level modules, and no -s option.
Exit code expected: 0, received: 1
Done


(1) - EDA Playground
Secure | https://www.edaplayground.com/x/4BHY#
EDA playground
Run
Save*
Copy*
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-Wall
Run Options
Open EPWave after run
Download files after run
Examples
testbench.sv
SV/Verilog Testbench
1 // Code your testbench here
2 // or browse Examples
3 `timescale 1ns / 1ps
4
5 module testbench();
6
7 reg a1;
8 wire y1;
9 inverter inv1(y1,a1);
10
11 initial begin
12 a1 = 1'b1;
13 $display("a=%b",a1);
14 #1
15 $display("y=%b",y1);
16 end
17
18 endmodule
19
Log
Share
[2017-07-05 19:49:11 EDT] iverilog '-Wall' design.sv testbench.
testbench.sv:3: warning: Some modules have no timescale. This m
.sv:3: : confusing timing results. Affected mo
.sv:3: : -- module inverter declared here: de
OBS Studio 19.0.2 (64bi...