Josepoon Bession Dote Page Date: 28 5 2020 Name: Sneha. G Cousse: Logic Design US N: 4ALISECOSC Topic: - Analysis of CSC Digital clock design Pepositiony: Gneha-Gla Reposit: Analyses of clocked sequented rescults: Some flip-flop have asynchronous anpute that are used to josco flip-flop The App that sets flep-flop to 1 is called present
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· The 91p that sets flep-flop to 188 called present
00 direct set. The Enput that clears the flepflop.
· When power is turned on in a degétal system
the state of Ff's is unknown. The direct
Elp's are useful for brenging all FF's
one gris avallable in a state dable can be
sepresented graphically en the form of a state
dlagram.
-> Analyses with D. Trep flops:
The input equation of a DIF is given by DA: ADD,
of account are the 1/p to the clocust.
The state of the s
The expension course are Obtained from the state eggs
The next state values are obtained from the state equal to 1

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