Forenoon Session

Date: 28/5/2020

Name: Sneha.G

Course: Logic Design

USN: 4AL18EC05

Topic: • Analysis of CSC

Sem & Sec: IV, 'A'

• Digital clock design

GitHub Repository: Sneha-GIa

Report:

⇒ Analysis of clocked sequential circuits:

- Some flip-flop have asynchronous inputs that are used to force flip-flop
- The i/p that sets flip-flop to 1 is called present or direct set. The input that clears the flipflop
- When power is turned on in a digital system the state of FF's is unknown. The direct i/p's are useful for bringing all FF's
- The info available in a state table can be represented graphically in the form of a state diagram.

⇒ Analyses with D-Flip flops:

- The input equation of a DFF is given by $D_A = A \oplus x$
- The x & y variables are the i/p to the circuit.
- The state table has one column for the present state
- The next state values are obtained from the state eqn
- The expression specifies an odd function & equal to 1

Afternoon Session

Date: 28/5/2020 Name: Sneha G

Course: Python USN: 4AL19EC050

Topic: Object oriented programming Sem, Sec: IV ; A

GitHub Repository: Sneha-G19

Report

⇒ Object oriented programming

- Object oriented programming Explained
- Turning this application into OOP style
- Creating a Bank Account Object
- Inheritance
- OOP Glossary
- GUI in OOP Design [Practice]
- Solution