**DAILY ASSESSMENT FORMAT**

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| **Date:** | **4/06/2020** | **Name:** | **Yalpi Nandika** |
| **Course:** | **Digital Design Using HDL** | **USN:** | **4AL17EC096** |
| **Topic:** | **1.Hardware Modelling using verilog**  **2.FPGA and ASIC interview questions** | **Semester & Section:** | **6th Sem,B** |
| **GitHub Repository** | **Yalpi-Online-Courses** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
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| **Date:** | **4/06/2020** | **Name:** | **Yalpi Nandika** |
| **Course:** | **Python** | **USN:** | **4AL17EC096** |
| **Topic:** | **1.Advanced string**  **2.Advanced sets** | **Semester & Section:** | **6th sem,Bsection** |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |