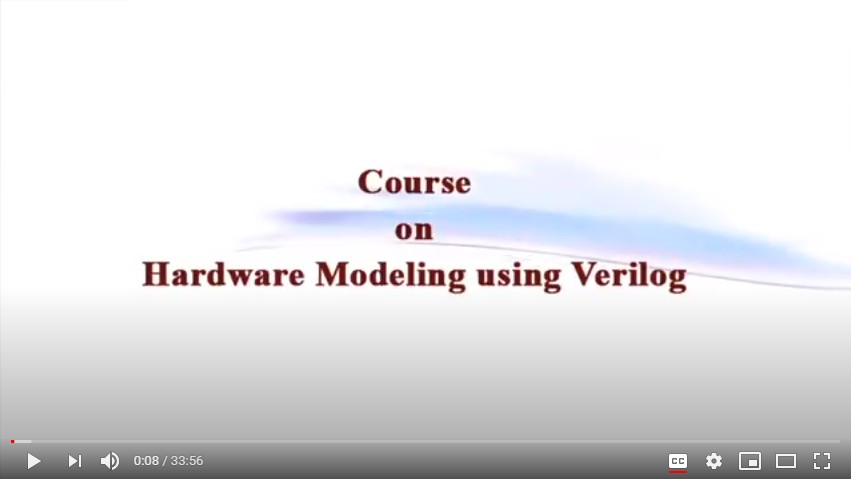
***DAILY ASSESSMENT FORMAT***

|  |  |  |  |
| --- | --- | --- | --- |
| ***Date:*** | ***2/06/2020*** | ***Name:*** | ***Yashaswini.R*** |
| ***Course:*** | ***DIGITAL DESIGN USING HDL*** | ***USN:*** | ***4AL17EC098*** |
| ***Topic:*** | ***FPGA Basics: Architecture, Applications and Uses,Verilog HDL Basics by Intel,Verilog Testbench code to verify the design under test (DUT)*** | ***Semester & Section:*** | ***6th Sem A sec*** |
| ***Github***  ***Repository:*** | ***Yashaswini*** |  |  |

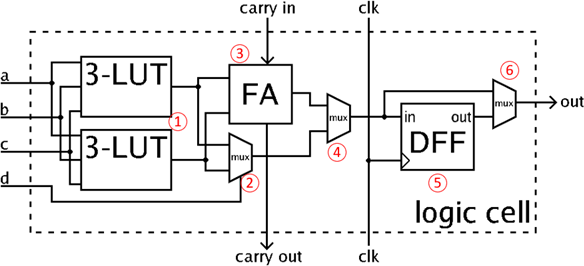


***Report – Report can be typed or hand written for up to two pages.***

# FPGA Architecture:

*A basic FPGA architecture (Figure 1) consists of thousands of fundamental elements called configurable logic blocks (CLBs) surrounded by a system of programmable interconnects, called a fabric, that routes signals between CLBs. Input/output (I/O) blocks interface between the FPGA and external devices.*

*Depending on the manufacturer, the CLB may also be referred to as a logic block (LB), a logic element (LE) or a logic cell (LC).*



# FPGA Application:

Many applications rely on the parallel execution of

identical operations; the ability to configure the FPGA’s CLBs into hundreds or thousands of identical processing blocks has applications in image processing, artificial intelligence (AI), data center hardware accelerators, enterprise networking and automotive advanced driver assistance systems (ADAS).

Many of these application areas are changing very quickly as requirements evolve and new protocols and standards are adopted. FPGAs enable manufacturers to implement systems that can be updated when necessary.

# FPGA Uses:

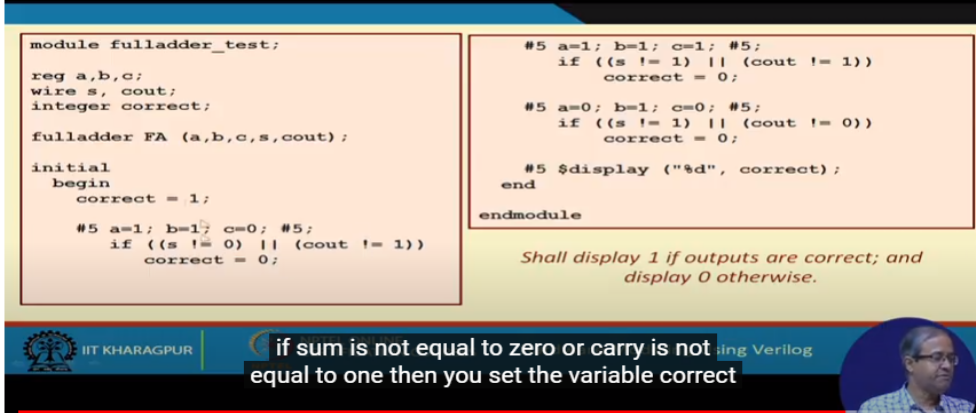
* *FPGAs are often used to provide a custom solution in situations in*

which developing an ASIC would be too expensive or time-consuming.

* *An FPGA application can be configured in hours or days instead of months. Of course, the flexibility of the FPGA comes at a price.*
* *An FPGA is likely to be slower, require more PCB area and consume more power than an equivalent ASIC.*

# Verilog HDL basics by Intel:

* *What is verilog?*
* *Verilog History*
* *Verilog terminology*
* *RTL synthesis*
* *Data types,Net data types,Variable data types*
* *Module instantiation*
* *Port declaration,Port connection rules*
* *Parameters,assigning values*
* *Operators ,Assignment statements*
* *Loops ,case statements*
* *Clock enable*
* *Functional counter*



***Write a verilog code to implement NAND gate in all different styles:***

# IMPLEMENTATION :

module m41 ( input a, input b,

input c, input d, input s0, s1, output out);

assign out = s1 ? (s0 ? d : c) : (s0 ? b : a); endmodule

# TEST BENCH :

*module top;* ***wire out; reg a;***

# reg b; reg c; reg d;

***reg s0, s1;***

***m41 name(.out(out), .a(a), .b(b), .c(c), .d(d), .s0(s0), .s1(s1)); initial***

***begin***

***a=1'b0; b=1'b0; c=1'b0; d=1'b0; s0=1'b0; s1=1'b0;***

***#500 $finish; end***

***always #40 a=~a;***

***always #20 b=~b;***

***always #10 c=~c;***

***always #5 d=~d;***

***always #80 s0=~s0;***

***always #160 s1=~s1;***

***always@(a or b or c or d or s0 or s1)***

***$monitor("At time = %t, Output = %d", $time, out); endmodule***

***Date: 2/06/2020 Name: Yashaswini.R***

***Course: Python USN: 4AL17EC030***

***Topic: Python for Image and Video processing***

***Semester & Section:***

***6th Sem A sec***

***AFTERNOON SESSION DETAILS***



***Image of session***

***Report – Report can be typed or hand written for up to two pages.***

*Matchmaker Game:*

1. A Matchmaker game is programmed using TKintermodule package of python library.
2. Tkinter is the standard GUI library for Python.
3. Python when combined with Tkinter provides a fast and easy way to create GUI applications.
4. Tkinter provides a powerful object-oriented interface to theTkGUI toolkit. 5.Creating a GUI application using Tkinter is an easy task.
5. Steps involved in creating the Matchmakergame are:
   1. ImporttheTkintermodule.
   2. Create the GUI application main window.
   3. Add the required widgets to the GUI application.
   4. Enter the main event loop to take action against each event triggered by the user.