**DAILY ASSESSMENT FORMAT**

|  |  |  |  |
| --- | --- | --- | --- |
| **Date:** | **01-06-2020** | **Name:** | **Yashwitha C N** |
| **Course:** | **Digital design using HDL** | **USN:** | **4al17ec099** |
| **Topic:** | **•Industry Application of FPGA**  **•FPGA Business Fundamental**  **•FPGA vs FPGA design flow**  **•FPGA basics A look under the hood** | **Semester & Section:** | **6th sem**  **B sec** |
| **Github Repository:** | **Yashwitha-coures** |  |  |

|  |
| --- |
| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.** |