**DAILY ASSESSMENT FORMAT**

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| **Date:** | **02-06-2020** | **Name:** | **Yashwitha C N** |
| **Course:** | **Digital design using HDL** | **USN:** | **4al17ec099** |
| **Topic:** | **•FPGA Basics Architecture Application and Uses**  **•Verilog HDL Basics by intel**  **•Verilog testbench code to verify the design under test (DUT)** | **Semester & Section:** | **6th sem**  **B sec** |
| **Github Repository:** | **Yashwitha-coures** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.** |