

June3 ASSESSMENT

Date:	03/06/20	Name:	Ankitha c c
Course:	Digital designing using hdl	USN:	4al16ec004
Topic:	About EDA	Semester & Section:	8th & a
Github Repository:	ankitha-course		

FORENOON SESSION DETAILS

Image of session

```

// Code your testbench here
`timescale 1ns / 1ps
`include "design.sv"
module testbench;
    reg a;
    reg b;
    invt inverter inv(a, b);
    initial begin
        $readmemh("abc", a);
        $readmemh("xyz", b);
        $display("%b", a);
        $display("%b", b);
    end
endmodule

```

```

// Code your design here
module inverter(a, b);
    input a;
    output b;
    assign b = ~a;
endmodule

```

```

testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:       confusing timing results. Affected modules are:
testbench.sv:3:           inverter declared here: design.sv
a=1
b=0

```

Report - Report can be typed or hand written for up to two pages.

EDA Playground Help

Quick Start

Log in. Click the Log in button (top right) Then either

click on Google or Facebook or

register by clicking on 'Register for a full account' (which enables all the simulators on EDA Playground)

Select your language from the Testbench + Design menu.

Select your simulator from the Tools & Simulators menu. Using certain simulators will require you to supply additional identification information.

Type in your code in the testbench and design windows.

Click Run.

Tutorial <<http://eda-playground.readthedocs.io/en/latest/tutorial.html>>

EDA Playground on YouTube - Tutorials for Verilog, SystemVerilog, UVM, and VHDL, interview questions, news and features, etc.

What is EDA Playground?

EDA Playground gives engineers immediate hands-on exposure to simulating SystemVerilog, Verilog, VHDL, C++/SystemC, and other HDLs. All you need is a web browser. The goal is to accelerate learning of design/testbench development with easier code sharing and simpler access to EDA tools and libraries.

With a simple click, run your code and see console output in real time.

View waves for your simulation using EPWave browser-based wave viewer.

Save your code snippets ("Playgrounds").

Share your code and simulation results with a web link. Perfect for web forum discussions or emails. Great for asking questions or sharing your knowledge.

Quickly try something out

Try out a language feature with a small example.

Try out a library that you're thinking of using.

```

class my_driver extends uvm_driver #(uvm_transaction);
  ...
endclass

function void build_phase(uvm_component parent);
  ...
endfunction

task run_phase(uvm_phase phase);
  ...
endtask

task run_phase(uvm_phase phase);
  ...
endtask

```

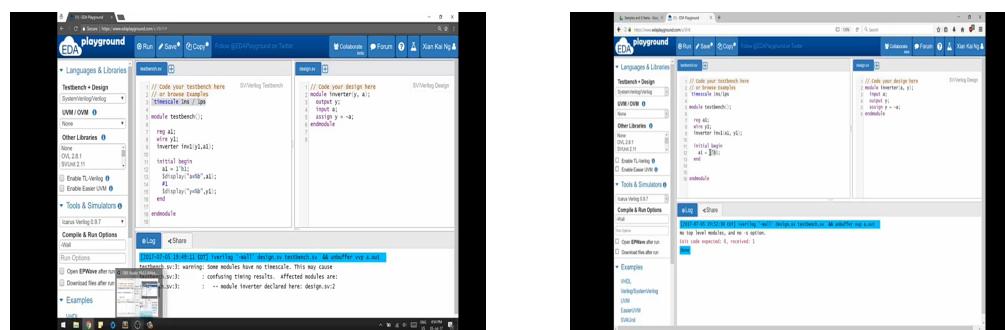
Results:

```

[1] // This is the SystemVerilog interface that we will use for our UVM testbench.
[2] interface dut_if;
[3]   logic [32] data;
[4]   logic [32] address;
[5]   logic [32] offset;
[6]   logic [32] size;
[7]   logic [32] response;
[8]   logic ready;
[9]   logic [32] data;
[10]  endinterface
[11] 
[12] // This is our design module.
[13] class my_design extends uvm_design;
[14]   ...
[15]   logic [32] data;
[16]   logic [32] address;
[17]   logic [32] offset;
[18]   logic [32] size;
[19]   logic [32] response;
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```

EDA Playground Tutorial Demo Video



How to Download And Install Xilinx Virarado Design Suite

Vivado Design Suite - HLx Editions Update 1 - 2019.2

Important Information

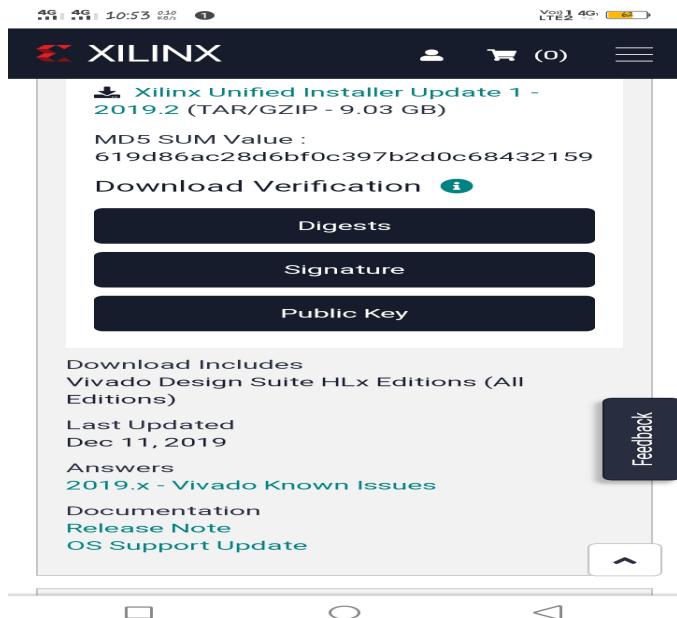
This is a common update. You do not need to re-run it for Vitis if you have already run it for Vivado and vice versa.

Vivado Design Suite 2019.2.1 is now available with support for:

Additional Zynq UltraScale+ RFSOCs devices enabled:- (XCZU46DR, XCZU47DR, XCZU48DR, XCZU49DR)

For customers using these devices, Xilinx recommends installing Vivado 2019.2.1. For other devices, please continue to use Vivado 2019.2.

Note: Download verification is only supported with Google Chrome and Microsoft Internet Explorer web browsers.



Vivado Design Suite for implementation of HDL code

Introduction

Synthesis is the process of transforming an RTL-specified design into a gate-level representation. Vivado® synthesis is timing-driven and optimized for memory usage and performance. Vivado synthesis supports a synthesizable subset of:

- SystemVerilog: IEEE Standard for SystemVerilog—Unified Hardware Design,

Specification, and Verification Language (IEEE Std 1800-2012)

- Verilog: IEEE Standard for Verilog Hardware Description Language (IEEE Std 1364-2005)
- VHDL: IEEE Standard for VHDL Language (IEEE Std 1076-2002)

- VHDL 2008

- Mixed languages: Vivado supports a mix of VHDL, Verilog, and SystemVerilog.

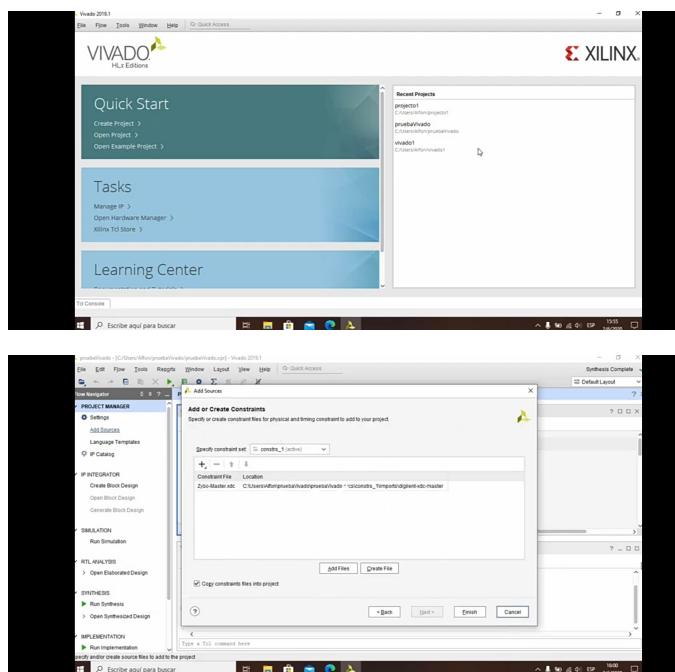
In most instances, the Vivado tools also support Xilinx design constraints (XDC), which is based on the industry-standard Synopsys design constraints (SDC).

Synthesis Methodology

The Vivado IDE includes a synthesis and implementation environment that facilitates a push button flow with synthesis and implementation runs. The tool manages the run data automatically, allowing repeated run attempts with varying Register Transfer Level (RTL) source versions, target devices, synthesis or implementation options, and physical or timing constraints.

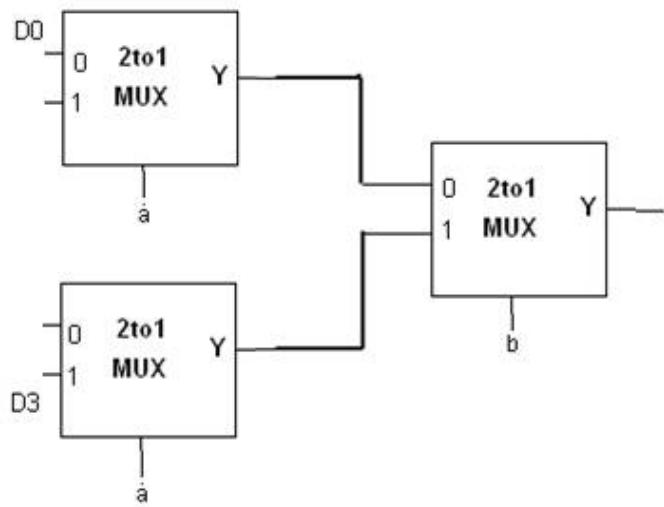
Within the Vivado IDE, you can do the following:

- Create and save a strategy. A strategy is a configuration of command options that you can apply to design runs for synthesis or implementation. See [Creating Run Strategies](#).
- Queue the synthesis and implementation runs to launch sequentially or simultaneously with multi-processor machines. See [Running Synthesis](#).
- Monitor synthesis or implementation progress, view log reports, and cancel runs. See [Monitoring the Synthesis Run](#).



Task 3

Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.



```
module mux4to1(a,sel,out);
    input [3:0] a;
    input [1:0] sel;
    output out;
    wire mux[2:0];
    mux2to1 m1 (a[3],a[2],sel[0],mux_1),
    m2 (a[1],a[0],sel[0],mux_2),
    m3 (mux_1,mux_2,sel[1],out);
endmodule.
```

Date: 03/06/20 Name: Ankitha c c
Course: Python USN: 4al16ec004
Topic: Semester & 8th & a
Section:

AFTERNOON SESSION DETAILS

Image of session



The screenshot shows a Jupyter Notebook interface with a table titled "Scraped Website Data - How The Output Will Look Like". The table contains data from a real estate website, listing various addresses, their details, and prices. The columns include Address, Bedrooms, Bathrooms, Half Bathrooms, Locality, Lot Size, and Price.

Index [i]	Address	Bedrooms	Bathrooms	Half Bathrooms	Locality	Lot Size	Price
0	200 Calleloma	None	None	None	Rock Springs, WY 82261	Half	\$725,000
1	1023 Winchester Blvd	None	4	None	Rock Springs, WY 82261	Under 1/2 Acre	\$325,000
2	12729 Speedwell Way	3	2	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
3	11461 1st	3	2	1	Rock Springs, WY 82261	Half	\$375,000
4	3407 Broad Avenue	3.25	1	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
5	238 Via Spindrift	2.88	4	2	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
6	2420 Crooked Creek	3.5	2	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
7	1172 1st	1.5	2	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
8	1302 Melody Drive	1.52	1	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
9	1421 Via Rustica	None	1	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000
10	1101 Mission Dr	1.04	1	1	Rock Springs, WY 82261	Under 1/2 Acre	\$375,000

Report - Report can be typed or hand written for up to two pages.

Request Headers

Note

Whenever I use this code in the next videos:

```
r = requests.get("http://www.pythonhow.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/")
```

please use this instead:

```
r = requests.get("http://www.pyclass.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/", headers={'User-agent': 'Mozilla/5.0 (X11; Ubuntu; Linux x86_64; rv:61.0) Gecko/20100101 Firefox/61.0'})
```

The rest of the code stays the same.

So, we're just changing the domain name from pythonhow to pyclass and we're adding a header argument. Some webpages don't like scripts sometimes, so adding a header allows the script to impersonate a web browser.

