Date:- 4/6/20

Course:- Digital design using HDL

Topic:- Hardware modeling using verilog & fpga & asic.

Name:- Harshitha.T

USN:- 4AL17EC106

Sem:- 6th & B.

* Hardware modeling using verilog it uses various digital circuit modeling issues using verilog, writing test benches and some case studies.
* Here the paper provides an overview of some of the key elements of FPGAs for engineers interested in utilizing FPGA-based technologies.
* This paper still give you a lot of help information if youre new to the world of FPGA.
* Here we are not designing the FPGA. We are using code to tell the chip how to configure itself.
* Lot of planning bugs happens more the we expected. If we are a newbie developer
* Application-speific realites you to concern with resolving around cyber security and saftey.
* For example, some have A/D converters and PLLs
* ASIC is the core of it, youre desinging a digital logic circuit, as in AND, OR etc.
* There are four algorithm/processing attributes defined below that FPGAs are generally well-suited for.
* High data-to-clock rate ratio - if we calculate the need to be executed over & over continuously.

* The amount of determinism that you can achieve with an FPGA will usually far surpass that of a typical sequential processor.
* If there are too many operations to executed, we may not have enough time to close the loop to update all the I/O within the alloted time.
* It has more advanced components Hard cores. — These are functional blocks that have their own dedicated logical resources.

Date:- Mon 4/6/20

Course:- Python

Topic:- Build a web based financial graph

Name: Harshitha.T

USN:- 4AL17EC106

Sem & :- 6th B.

Sec

* The aims to inspect the stableness of interactive affinity blw search interest of prices of the stock & evidence stock market outcomes on world wide equity market indices.
* This study represents and develop former exploration into financial graph by registering the attributes and magnitudes of graph use and embarkement from representational impartially.
* Parador could also be derived through investoors behaviour and degree of disclousre inclusion.
* Downloading Dataset with python

```
from pandas - data reder import data
import data time
Statt = datatime. datatime (2016, 3, 1)
end = data time - data time (2016, 3, 1).
data. Data Reader (name = " AAPL". data. reader
                    "Yahoo", start. end. end)
```

* @ app - routes (/.)

def home():

```
    return render_template("home.html")
* @ app.route('/about/')
  def about():
  if __name__ == "__main__":
  app.run(debug = time).
```