Date:- 5/6/20
Course:- Digital design using HDL
Topic:- Verilog tutorials & practise program

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* FPGA projects → The first FPGA project helps students to understand the basics of FPGAs and how Verilog/VHDL works on FPGA

* D flip flop code

```
module d_ff (clk, d, q, q_bar);
input d, clk;
output q, q_bar;
wire d, clk;
reg q, q_bar;
always @ (posedge clk)
begin
q <= d;
q_bar <= !d;
end
endmodule.
```

* Bottom up design

Each design is performed at the gate level using the standard gates with increasing complexity of new designs this approach is nearly ~~impossible~~ impossible to maintain.

* Top-Down Design.

A real top-down design allows early testing easy change of different technologies a structured system design and offers many other advantages.

* Abstraction levels of Verilog

→ Behavioral Level

→ Register - Transfer level

→ Gate level.

* Data types

There are two primary data types

→ Nets → Registers.

* All the data types were explained with example program and codes.

Date:- 5/6/20
Course:- Python
Topic:- Applications

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* Flask startup and configuration like most widely used Python libraries, the flask package is installable from the python package index (PPI).
* Firstly we should create a directory to work in i.e (flask_to do) ~~ss~~a then install the flask package.
* we have install flask-sqlacherry so our flask application has a simple way to talk to a SQL database.
* We should create setup.py which should look like this:

```
requires = [
        'flask',
        'flask-sqlalchemy',
        'psycopg2',
    ]

setup (
    name = 'flask_todo',
    version = '0.0',
    description = 'A To-Do List built with Flask',
    author = <' Your actual name here'>,
    author_email = <' Your actual email address here'>,
```

```
    keywords = 'web flask',
    packages = find_packages(),
    includes_package_data=True,
    install_requires = requires
)
```

This is the way whenever we want to install & deploy our project.