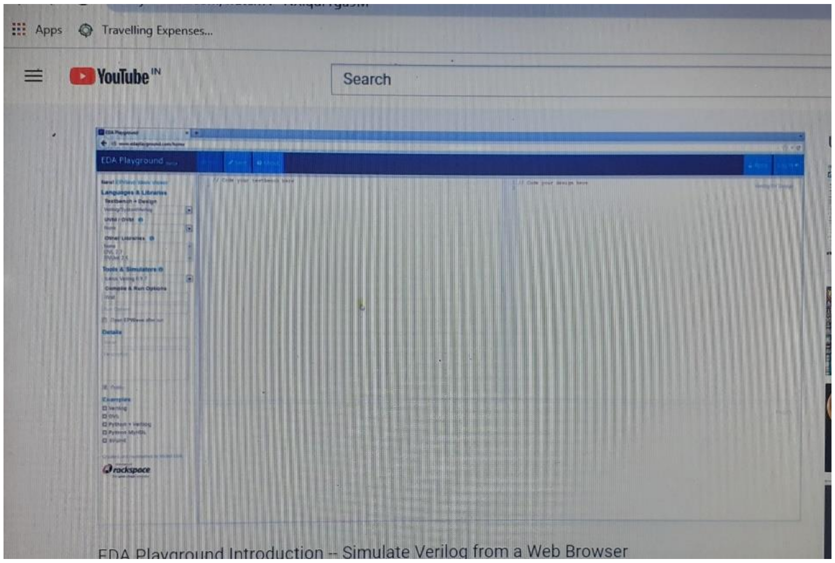
DAILY ASSESSMENT

Date:	3-6-2020	Name:	Kavyashree m
Course:	Digital design using HDL	USN:	4al15ec036
Topic:	EDA Playground Tutorial Demo Video, How to Download And Install Xilinx Vivado Design Suite, Vivado Design Suite for implementation of HDL code	Semester & Section:	8th A
Github Repository:	kavya		

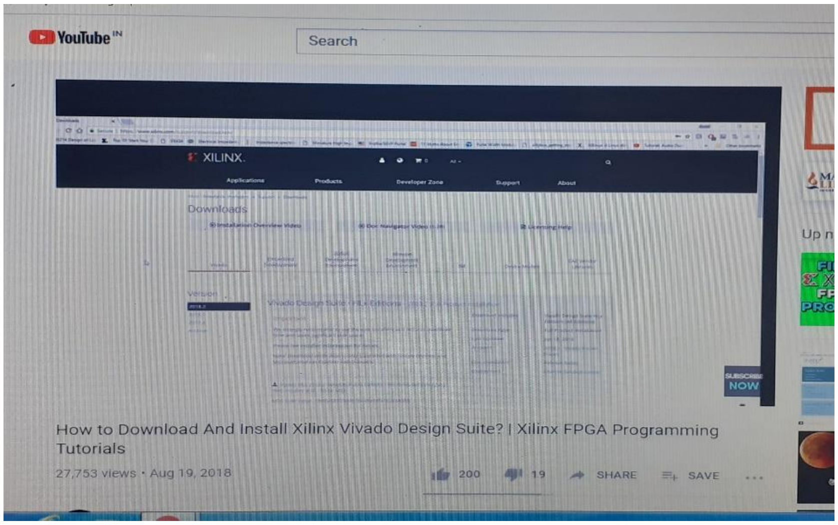
FORENOON SESSION DETAILS

Image of session



EDA Playground Introduction -- Simulate Verilog from a Web Browser

Fig 1: EDA Playground Tutorial Demo Video



How to Download And Install Xilinx Vivado Design Suite? | Xilinx FPGA Programming Tutorials

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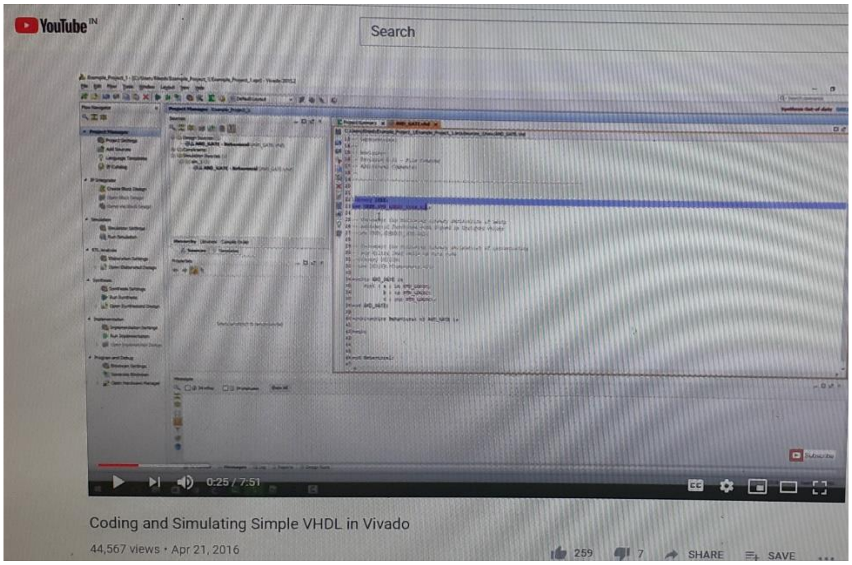
Fig 2 : How to Download And Install Xilinx Vivado Design Suite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7
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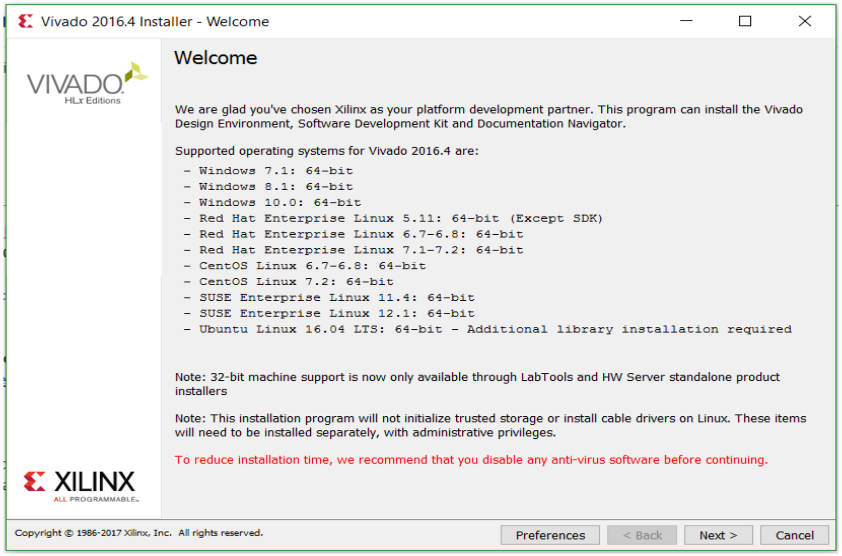
Fig 3 : Vivado Design Suite for implementation of HDL code

Download And Install Xilinx Vivado Design Suite

Vivado is the software that Xilinx has available for all of its current FPGAs, so we'll go through how to download the free WebPACK version of Vivado.

First, we have to download Vivado. Once you get to the download page, choose the appropriate installer for your system.



Welcome

We are glad you've chosen Xilinx as your platform development partner. This program can install the Vivado Design Environment, Software Development Kit and Documentation Navigator.

Supported operating systems for Vivado 2016.4 are:

```
 - Windows 7.1: 64-bit
 - Windows 8.1: 64-bit
 - Windows 10.0: 64-bit
 - Red Hat Enterprise Linux 5.11: 64-bit (Except SDK)
 - Red Hat Enterprise Linux 6.7-6.8: 64-bit
 - Red Hat Enterprise Linux 7.1-7.2: 64-bit
 - CentOS Linux 6.7-6.8: 64-bit
 - CentOS Linux 7.2: 64-bit
 - SUSE Enterprise Linux 11.4: 64-bit
 - SUSE Enterprise Linux 12.1: 64-bit
 - Ubuntu Linux 16.04 LTS: 64-bit - Additional library installation required
```

Note: 32-bit machine support is now only available through LabTools and HW Server standalone product installers

Note: This installation program will not initialize trusted storage or install cable drivers on Linux. These items will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.

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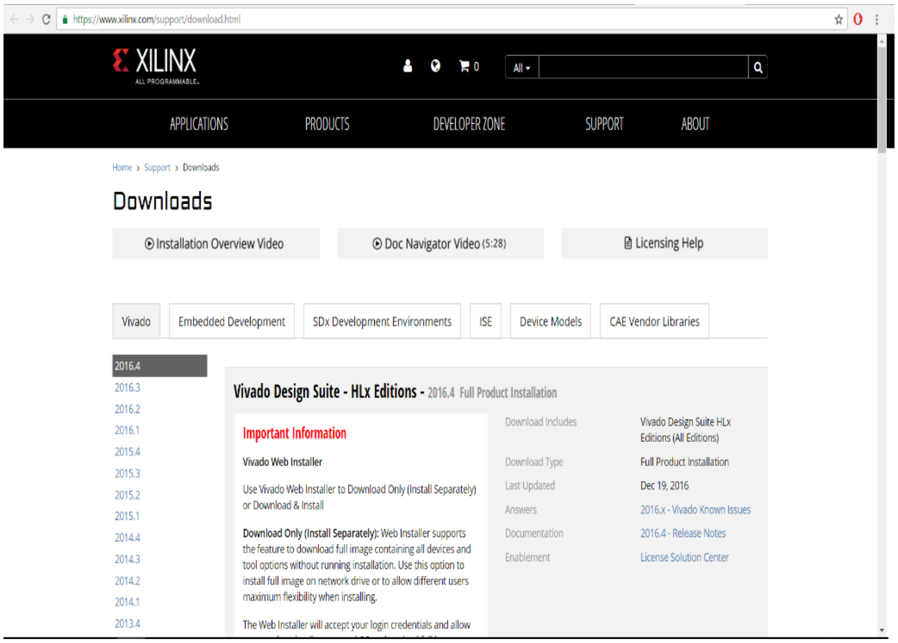
If you're familiar with Digilent, you'll know that we have a wide variety of Field Programmable Gate Arrays that can do many strange, complex, and wonderful things if you program them to do so. The big catch with this is that you have to download the software in order to program them. Simple right? Maybe not for everybody- otherwise we wouldn't see questions on how to get FPGAs up and running for the first time. Vivado is the software that Xilinx has available for all of its current FPGAs, so we'll go through how to download the free WebPACK version of Vivado.



Vivado Design Suite - HLx Editions - 2016.4 Full Product Installation

Important Information

Vivado Web Installer

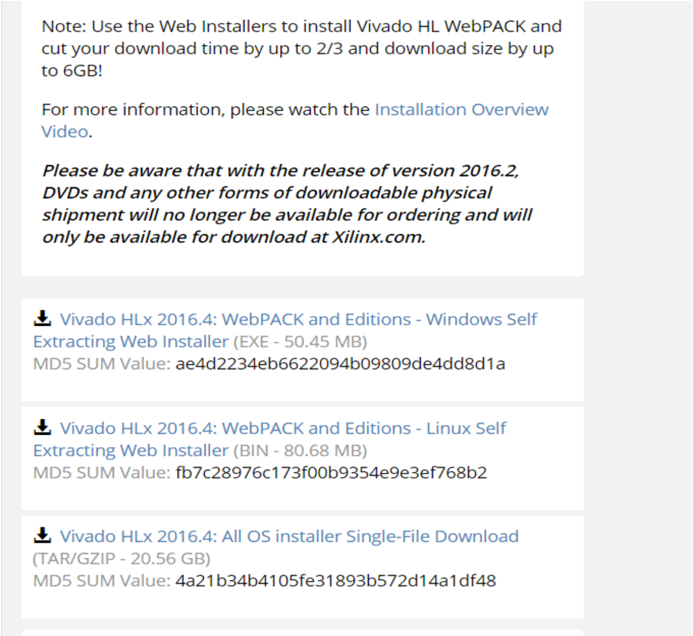
Use Vivado Web Installer to Download Only (Install Separately) or Download & Install

Download Only (Install Separately): Web Installer supports the feature to download full image containing all devices and tool options without running installation. Use this option to install full image on network drive or to allow different users maximum flexibility when installing.

The Web Installer will accept your login credentials and allow

Download Includes	Vivado Design Suite HLx Editions (All Editions)
Download Type	Full Product Installation
Last Updated	Dec 19, 2016
Answers	2016.x - Vivado Known Issues
Documentation	2016.4 - Release Notes
Enablement	License Solution Center

Once you get to the download page, choose the appropriate installer for your system; I'm on a Windows 10 machine and don't feel the need to get a universal, all OS installer, so I'll choose the Windows Self Extracting Web Installer.



Note: Use the Web Installers to install Vivado HL WebPACK and cut your download time by up to 2/3 and download size by up to 6GB!

For more information, please watch the Installation Overview Video.

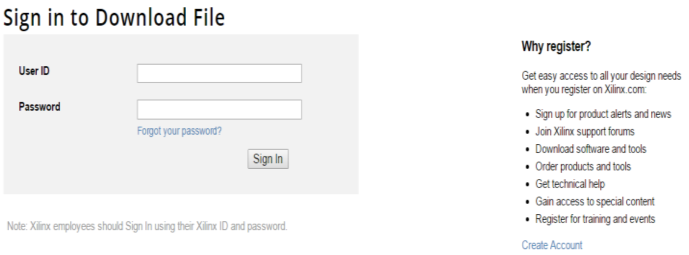
Please be aware that with the release of version 2016.2, DVDs and any other forms of downloadable physical shipment will no longer be available for ordering and will only be available for download at Xilinx.com.

Vivado HLx 2016.4: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 50.45 MB)
MD5 SUM Value: ae4d2234eb6622094b09809de4dd8d1a

Vivado HLx 2016.4: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 80.68 MB)
MD5 SUM Value: fb7c28976c173f00b9354e9e3ef768b2

Vivado HLx 2016.4: All OS installer Single-File Download (TAR/GZIP - 20.56 GB)
MD5 SUM Value: 4a21b34b4105fe31893b572d14a1df48

Which Vivado WebPACK installer do I choose?
Xilinx likes to know what demographic of people use their software so you’ll need to either sign in to your pre-existing account or create one with Xilinx.



Sign in to Download File

User ID

Password

Forgot your password?

Sign In

Note: Xilinx employees should Sign In using their Xilinx ID and password.

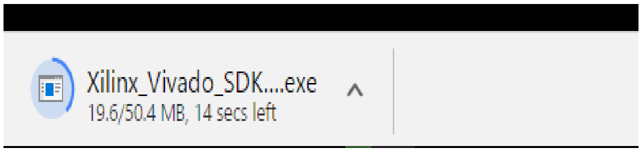
Why register?

Get easy access to all your design needs when you register on Xilinx.com:

- Sign up for product alerts and news
- Join Xilinx support forums
- Download software and tools
- Order products and tools
- Get technical help
- Gain access to special content
- Register for training and events

Create Account

Sign into your Xilinx account or create a Xilinx account to download the web installer. Once you sign in, go ahead and let your chosen installer download and then let it run.

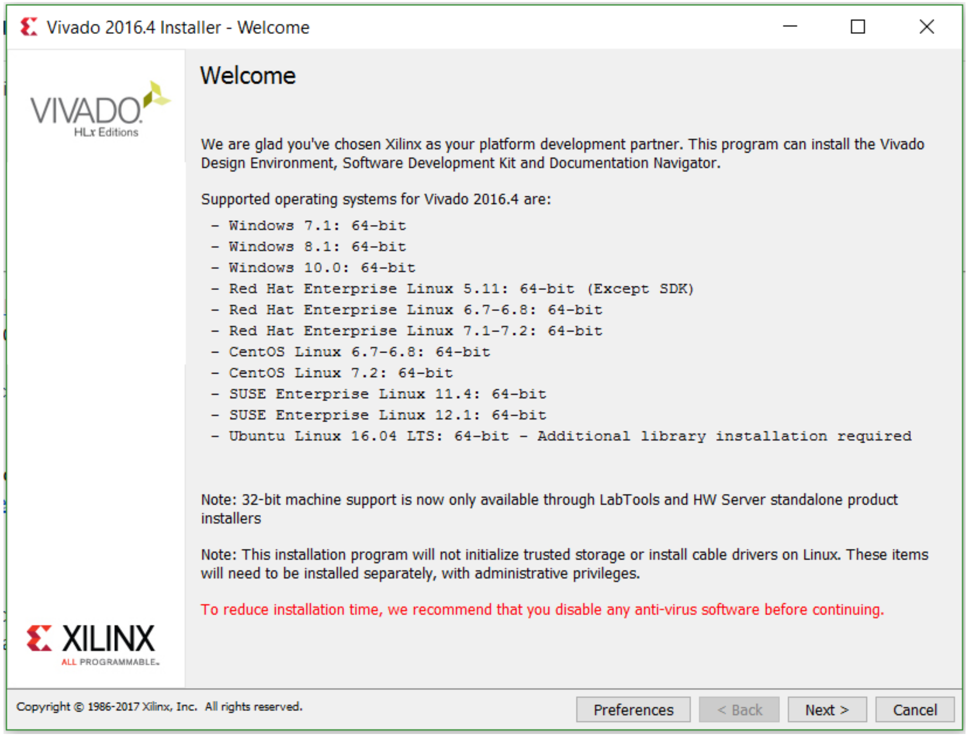


Xilinx_Vivado_SDK....exe
19.6/50.4 MB, 14 secs left

Downloading the Vivado web installer

You’ll first be brought to a friendly opening screen where it asks you to confirm that you have a compatible OS so you don’t download a large file only to have it not work.

You can also choose some installation preferences such as how many cores your computer utilizes to download Vivado, but I went with all of the default preferences.



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 - CentOS Linux 6.7-6.8: 64-bit
 - CentOS Linux 7.2: 64-bit
 - SUSE Enterprise Linux 11.4: 64-bit
 - SUSE Enterprise Linux 12.1: 64-bit
 - Ubuntu Linux 16.04 LTS: 64-bit - Additional library installation required
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Note: 32-bit machine support is now only available through LabTools and HW Server standalone product installers

Note: This installation program will not initialize trusted storage or install cable drivers on Linux. These items will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.

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Make sure you have a compatible OS before downloading Vivado.Xilinx will ask you to sign in again and choose how you want to download/install.choose the “Download and Install Now” to make I only download what I need to help conserve space on my laptop.

Vivado Design Suite for implementation of HDL code

1. In a separate web browser window, log in to EDA Playground.
2. Log in. Click the Log in button (top right) Then either

- click on Google or Facebook or
- register by clicking on ‘Register for a full account’ (which enables all the simulators on EDA Playground)

1. Select ‘Aldec Riviera Pro’ from the Tools & Simulators menu. This selects the Aldec Riviera Pro simulator, which can be used however you logged in. Using certain other simulators will require you to have registered for a full account.

2. In either the *Design* or *Testbench* window pane, type in the following code:
3. module test;
4.   initial
5. $display("Hello World!");
6. endmodule
7. Click Run (top left)

Yes, running a simulation is as simple as that!

8. In the bottom pane, you should see real-time results as your code is being compiled and then run. A run typically takes 1-5 seconds, depending on network traffic and simulator. Near the bottom of result output, you should see:
9. Hello World!
10. Now, let’s save our good work. Click the Share tab near in the bottom pane and then type in a name and description. Then click Save.
11. The browser page will reload and the browser address bar will change. This is a persistent link to your saved code. You can send the link by email, post it on a web page, post it on Stack Overflow forums, etc.
12. Now, let’s try modifying existing code. Load the following example: RAM
13. On the left editor pane, before the end of initial block, add the following:
14. write_enable = 1;
15. data_write = 8'h2C;
16. toggle_clk_write;
17. toggle_clk_read;
18. $display("data[%0h]: %0h",
19.   address_read, data_read);
20. Run the sim. In the results you should see this new message:
21. data[1b]: 2c

22. Optional. Click *Copy* to save a personal version of the modified *RAM* code, including the simulation results.

Loading Waves from EDA Playground

You can run a simulation on EDA Playground and load the resulting waves in EPWave.

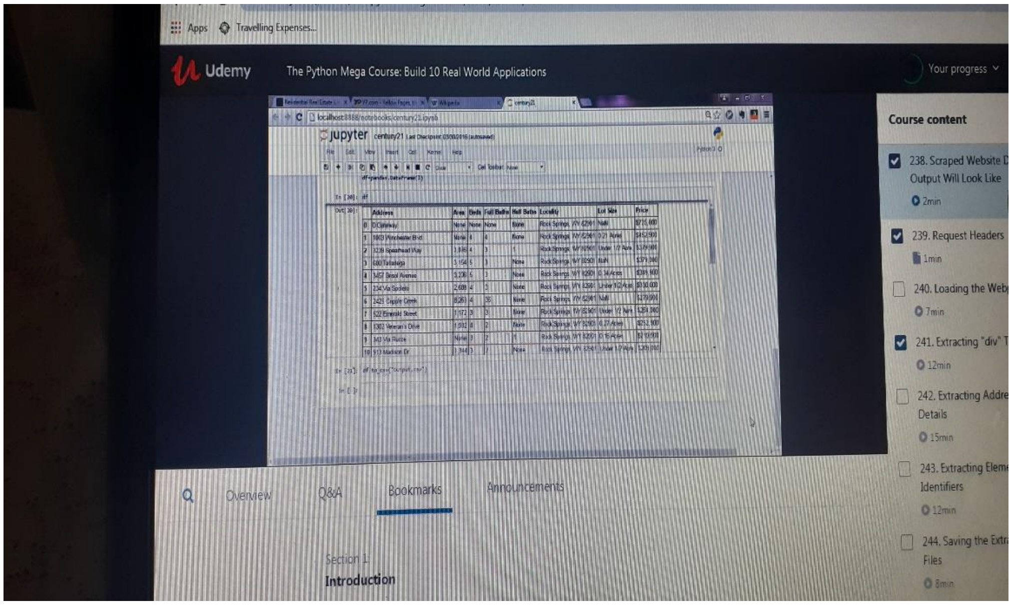
Loading Waves for SystemVerilog and Verilog Simulations

- Go to your code on EDA Playground. For example: RAM Design and Test
- Make sure your code contains appropriate function calls to create a *.vcd file. For example:
- initial begin
-   $dumpfile("dump.vcd");
-   $dumpvars(1);
- end
- Select a simulator and check the Open EPWave after run checkbox. Click Run. After the run completes, the resulting waves will load in a new EPWave window.
- Loading Waves for VHDL Simulations
- Check the Open EPWave after run checkbox.
- Specify the Top entity to simulate.
- Click Run. After the run completes, the resulting waves will load in a new EPWave window. (Pop-ups must be enabled.)
  - The waves for all signals in the specified Top entity and any of its components will be dumped.
  - In EPWave window, click Get Signals to select the signals to view.

AFTERNOON SESSION DETAILS

Date:	**3-6-2020**	**Name:**	**Kavyashree m**
Course:	**Python programming**	**USN:**	**4al15ec036**
Topic:	**Scrape Real Estate Property Data from the Web**	**Semester & Section:**	**8th A**
Github Repository:	**Kavya**		

Image of session


Apps
Travelling Expenses...
Udemy
The Python Mega Course: Build 10 Real World Applications
Your progress
localhost:8888/notebooks/century21.ipynb
jupyter century21 Last Checkpoint 03/30/2016 (autosaved)
File Edit View Insert Cell Kernel Help
Overview
Q&A
Bookmarks
Announcements
Section 1:
Introduction

```
df=pandas.DataFrame(l)

In [20]: df
Out[20]:
```

	Address	Area	Beds	Full Baths	Half Baths	Locality	Lot Size	Price
0	0 Gateway	None	None	None	None	Rock Springs, WY 82901	NaN	$725,000
1	1003 Winchester Blvd	None	4	4	None	Rock Springs, WY 82901	0.21 Acres	$452,900
2	3239 Spearhead Way	3,046	4	3	1	Rock Springs, WY 82901	Under 1/2 Acre	$396,900
3	600 Talladega	3,154	5	3	None	Rock Springs, WY 82901	NaN	$379,000
4	3457 Bristol Avenue	3,106	5	3	None	Rock Springs, WY 82901	0.34 Acres	$385,900
5	234 Via Spoleto	2,688	4	3	None	Rock Springs, WY 82901	Under 1/2 Acre	$330,000
6	2425 Cripple Creek	8,261	4	3.5	None	Rock Springs, WY 82901	NaN	$279,900
7	522 Emerald Street	1,172	3	3	None	Rock Springs, WY 82901	Under 1/2 Acre	$254,000
8	1302 Veteran's Drive	1,932	4	2	None	Rock Springs, WY 82901	0.27 Acres	$252,900
9	343 Via Rocce	None	3	2	1	Rock Springs, WY 82901	0.16 Acres	$210,900
10	913 Madison Dr	1,344	3	2	None	Rock Springs, WY 82901	Under 1/2 Acre	$209,000

```
In [21]: df.to_csv("output.csv")

In [ ]:
```

Course content

☑ 238. Scraped Website D Output Will Look Like 2min

☑ 239. Request Headers 1min

□ 240. Loading the Web 7min

☑ 241. Extracting "div" T 12min

□ 242. Extracting Addre Details 15min

□ 243. Extracting Eleme Identifiers 12min

□ 244. Saving the Extr Files 8min

Fig 1: Scrape Real Estate Property Data from the Web

Web Scraping in real estate to the rescue

Web scraping is the process of sorting through overwhelming amounts of data, refine the user’s searches and provide a list of relevant information. In a realtor’s case, it is the go-to tool for organized property listings. Scraping the web provides parameters which the realtor can further study to determine sales and prospective buyers. Parameters extracted by web scraping are:

- Size

- Property type
- Location
- Sale price
- Size
- Amenities
- Monthly rental price
- Parking spaces
- Agent contact

This information is displayed in form of a spreadsheet, allowing the realtor to make comparisons of relevant parameters.

Property value tracking

Let’s assume you decide to sell your property. Scraping the web for the value of similar properties can aid you in setting a good value on your own. This allows users searching for such properties to get fair deals, and on the other, you getting a profitable one.

Making the right investment

Obtaining real estate data is hard, as result of which most investors make financial investments blindly. ith web scraping, an investor can make decisions based on qualitative and relevant empirical data, rather than outdated or incomplete information. Aggregating property data from real estate listing websites is essential for investment analysis.

Rental Yield

Rental yield is the most important factor to be considered before investing in property. By scraping data from real estate websites, you can determine which properties have the best rental yield for any suburb. Moreover, scraping answers which property types (house, apartment, 1 bedroom, 2 bedrooms) are more preferred in a particular area and yield the best return on investment.

Track vacancy rates

A vacant investment property is risky. To minimize this risk, it is imperative to analyze property data and suburbs which have higher rental listings.The above parameters are the most relevant decoded by web scraping through numerous websites online. Having the above details at your fingertips improves a realtor’s efficacy at decision making, better communication and faster and profitable sales. The role of web scraping in retail is just getting started, its potential is however limitless.

Loading the Webpage in Python

They are highly specialized programming language embedded in Python. We can use it through re module of Python. It is also called RE or regexes or regex patterns. With the help of regular expressions, we can specify some rules for the possible set of strings we want to match from the data.

If you want to learn more about regular expression in general, go to the link https://www.tutorialspoint.com/automata_theory/regular_expressions.htm and if you want to know more about re module or regular expression in Python, you can followthe link https://www.tutorialspoint.com/python/python_reg_expressions.htm.

Example

In the following example, we are going to scrape data about India from http://example.webscraping.com after matching the contents of <td> with the help of regular expression.

```
import re

import urllib.request

response =

urllib.request.urlopen('http://example.webscraping.com/places/default/view/India-102')

html = response.read()

text = html.decode()

re.findall('<td class="w2p_fw">(.*?)</td>',text)
```

Output

The corresponding output will be as shown here −

```
[

   '<img src="/places/static/images/flags/in.png" />',

   '3,287,590 square kilometres',

   '1,173,108,018',

   'IN',

   'India',

   'New Delhi',

   '<a href="/places/default/continent/AS">AS</a>',

   '.in',

   'INR',

   'Rupee',

   '91',
  '######',
  '^(\\d{6})$',

'enIN,hi,bn,te,mr,ta,ur,gu,kn,ml,or,pa,as,bh,sat,ks,ne,sd,kok,doi,mni,sit,sa,fr,lus,inc',
  '<div>
    <a href="/places/default/iso/CN">CN </a>
    <a href="/places/default/iso/NP">NP </a>
    <a href="/places/default/iso/MM">MM </a>
    <a href="/places/default/iso/BT">BT </a>
    <a href="/places/default/iso/PK">PK </a>
    <a href="/places/default/iso/BD">BD </a>
  </div>'
]
```

Extracting "div" Tags

Extracting a div tag and its contents by id parses a block of HTML code and returns a string containing the value held within the div tag.

Call urllib.request.urlopen(url) to open a request of url. Use http.client.HTTPResponse.read() to return the HTML content of the request. Use bs4.BeautifulSoup(content, format) with format as "html" to parse this content. Call BeautifulSoup.find(tag_type, id_value) with tag_type as "div" and id_value as a dictionary with the syntax {"id": value} to extract a div tag by its id value. Use str() to convert the resultant content to a string.

```
url = "http://kite.com"
url_contents=urllib.request.urlopen(url).read()
soup = bs4.BeautifulSoup(url_contents, "html")
```

```
div = soup.find("div", {"id": "home-template"})
content = str(div)
print(content[:50])
print start of string
```

OUTPUT

```
<div id="home-template"><div class="homepage-banne
```

Extracting Elements without Unique Identifiers

We can use the class attribute of certain elements to filter down results. For example, looking at the list of blockquote elements returned by the previous query, and by looking at this page’s source, we can see that the blockquote elements on this page have different classes .

To refine the above query to get all the blockquote elements of the challenge class, we can type

```
document.querySelectorAll('blockquote.challenge')
```

which returns

```
<-Array[<blockquote.challenge>,<blockquote.challenge>,
<blockquote.challenge>, <blockquote.challenge> ]
```

Writing the Extracted Data in CSV Files

CSV (Comma Separated Values) is a simple file format used to store tabular data, such as a spreadsheet or database. CSV file stores tabular data (numbers and text) in plain text. Each line of the file is a data record. Each record consists of one or more fields, separated by commas. The use of the comma as a field separator is the source of the name for this file format.

Python provides an in-built module called csv to work with CSV files. There are various classes provided by this module for writing to CSV:

- Using csv.writer class
- Using csv.DictWriter class

Using csv.writer class

csv.writer class is used to insert data to the CSV file. This class returns a writer object which is responsible for converting the user's data into a delimited string. A csvfile object should be opened with newline='' otherwise newline characters inside the quoted fields will not be interpreted correctly.

csv.writer class provides two methods for writing to CSV. They are writerow() and writerows().

- **writerow():** This method writes a single row at a time. Field row can be written using this method.

Syntax:

writerow(fields)

- **writerows():** This method is used to write multiple rows at a time. This can be used to write rows list.

Syntax:

Writing CSV files in Python

writerows(rows)

Task 3

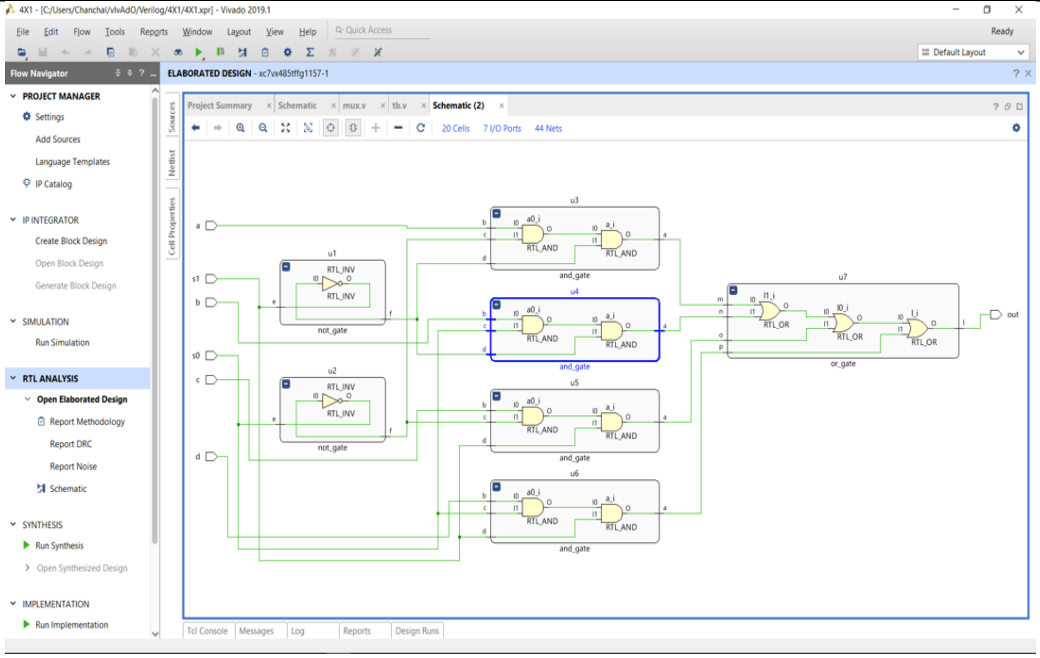
Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.

```
module and_gate(output a, input b, c, d);
assign a = b & c & d;
endmodule

module not_gate(output f, input e);
assign e = ~ f;
endmodule

module or_gate(output l, input m, n, o, p);
assign l = m | n | o | p;
endmodule

module m41(out, a, b, c, d, s0, s1);
output out;
input a, b, c, d, s0, s1;
wire s0bar, s1bar, T1, T2, T3;
not_gate u1(s1bar, s1);
not_gate u2(s0bar, s0);
and_gate u3(T1, a, s0bar, s1bar);
and_gate u4(T2, b, s0, s1bar);
and_gate u5(T3, c, s0bar, s1);
and_gate u6(T4, d, s0, s1);
or_gate u7(out, T1, T2, T3, T4);
endmodule
```


4X1 - [C:/Users/Chanchal/vlvAdO/Verilog/4X1/4X1.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7vx485tffg1157-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Sources
Netlist
Cell Properties
Project Summary
Schematic
mux.v
tb.v
Schematic (2)
20 Cells
7 I/O Ports
44 Nets
a
s1
b
s0
c
d
out
u1
RTL_INV
not_gate
u2
not_gate
u3
u4
u5
u6
a0_i
a_i
RTL_AND
and_gate
u7
I1_i
I0_i
I_i
RTL_OR
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Tcl Console
Messages
Log
Reports
Design Runs