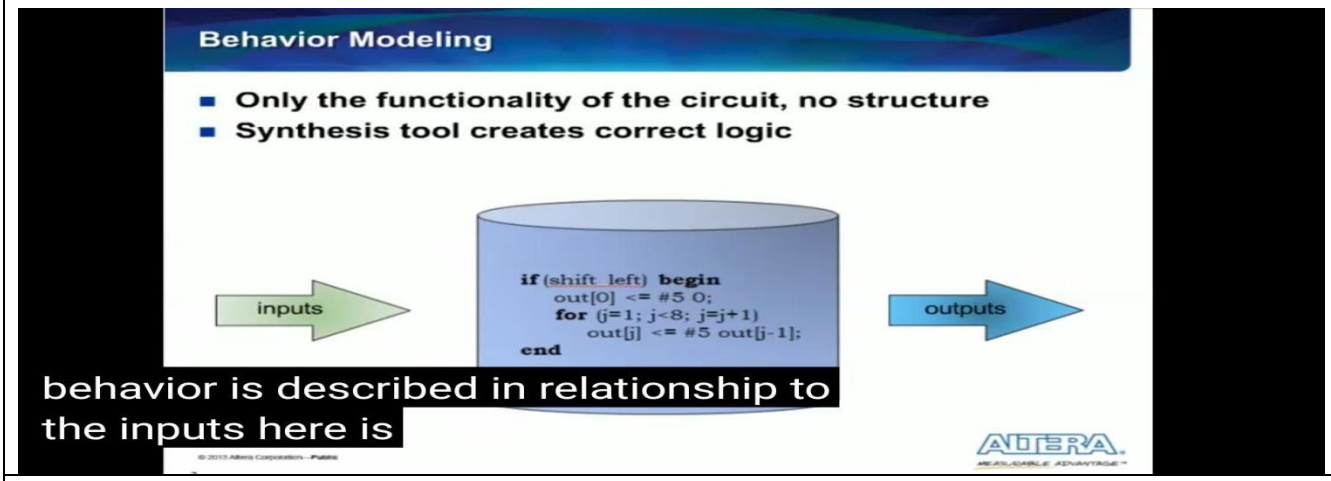
DAILY ASSESSMENT FORMAT

Date:	**2/06/2020**	**Name:**	**Kishan shetty**
Course:	**Digital Design Using HDL**	**USN:**	**4AL17EC041**
Topic:	**FPGA Basics: Architecture, Applications and Uses** **Verilog HDL Basics by intel** **Verilog Test bench code to verify the design under test (DUT).**	**Semester & Section:**	**6th sem A section**
GitHub Repository	**Kishanshetty-041**		

FORENOON SESSION DETAILS

Image of session



Report – Report can be typed or hand written for up to two pages.

- **Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL).**

It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using HDL we can describe any digital hardware at any level.

- Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.
- Verilog supports a design at many levels of abstraction. The major three are:
- **Behavioral level:**This level describes a system by concurrent algorithms (Behavioral). Every algorithm is sequential, which means it consists of a set of instructions that are executed one by one. Functions, tasks and blocks are the main elements. There is no regard to the structural realization of the design.
- **Register−Transfer Level:** Designs using the Register−Transfer Level specify the characteristics of a circuit using operations and the transfer of data between the registers. Modern definition of an RTL code is "Any code that is synthesizable is called RTL code".

• **Gate Level:** Within the logical level, the characteristics of a system are described by logical links and their timing properties. All signals are discrete signals. They can only have definite logical values (`0', `1', `X', `Z`). The usable operations are predefined logic primitives (basic gates). Gate level modelling may not be a right idea for logic design. Gate level code is generated using tools like synthesis tools and his netlist is used for gate level simulation and for backend.

• Some of the operators used in Verilog HDL

- **Arithmetic Operators** - These operators perform arithmetic operations (+, -, /, *, %).
- **Relational Operators -** These operators compare two operands and return the result in a single bit, 1 or 0 (==, !=, >, =, <=).
- **Bit-wise Operators -** Bit-wise operators which are doing a bit-by-bit comparison between two operands (&, |, ^, ~, ^~).
- **Logical Operators -** Logical operators are bit-wise operators and are used only for single-bit operands. They return a single bit value, 0 or 1 (!, &&, ||).
- **Reduction Operators-** Reduction operators are the unary form of the bitwise operators and operate on all the bits of an operand vector (&, |, ~&, ~|, ^, ~^).
- **Shift Operators -** Shift operators, which are shifting the first operand by the number of bits specified by second operand in the syntax (>>, <<).

Task :

Implement a 4:1 MUX and write the test bench code to verify the module

```
module m41 (input a, input b, input c, input d, input s0, s1, output out);
 assign out = s1 ? (s0 ? d : c) : (s0 ? b : a);
 endmodule
```

Date:	**2/06/2020**	**Name:**	**Kishan shetty**
Course:	**Python**	**USN:**	**4AL17EC041**
Topic:	**Interactive Data Visualization with Bokeh**	**Semester & Section:**	**6th sem A section**

AFTERNOON SESSION DETAILS

Image of session

- Some of the functions used under bokeh library:
  - The **figure ()** function under bokeh.plotting is used to create a new Figure for plotting. A subclass of Plot that simplifies plot creation with default axes, grids, tools, etc.
  - The **output_file ()** function configures the default output state to generate output saved to a file when show () function is called.
  - The **Show ()** function will immediately display a Bokeh object or application. Show () may be called multiple times in a single Jupyter notebook cell to display multiple objects. The objects are displayed in order.
  - The **line ()** method generates a single line glyph from one dimensional sequence of x and y points.
  - To scatter circle, triangle and square markers on the plot **circle (), triangle ()** and **square ()** methods are used respectively.