DAILY ASSESSMENT FORMAT

Date:	01 June 2020	Name:	Kishan shetty
Course:	Digital design using hdl	USN:	4AL17EC041
Topic:	• Industry Applications of FPGA • FPGA Business Fundamentals • FPGA vs ASIC Design Flow • FPGABasics	Semester & Section:	6th sem & A sec
Github Repository:	Kishanshetty-041		

FORENOON SESSION DETAILS
Image of session

FPGA Business Fundamentals

Intel PSG, CEG

Report – Report can be typed or hand written for up to two pages.

Industry Applications of FPGA:

• The impact of new FPGA features in industrial applications is analyzed in detail in three main areas, namely digital real-time simulation, advanced control techniques, and electronic instrumentation, with focus on mechatronics, robotics, and power systems design.

Core components of a FPGA

• **LUT (Look-Up Table)**: LUT is a logic lookup table, generally with 4 to 6 inputs and 1 to 2 outputs to specify any logical operation that fits within those bounds. There are however two other common uses for a LUT. LUT as a shift register – shift registers are very useful for things like delaying the timing of an operation to align the outputs of one algorithm with another. Size varies based on FPGA. LUT as a small memory – you can configure the LUT logic as a VERY small volatile random-access memory block. Size varies based on FPGA.

• **Flip-flop:**Flip-flops store the output of a combinational logic calculation. This is a critical element in FPGA design because you can only allow so much asynchronous logic and routing to occur before it is registered by a synchronous resource , otherwise the FPGA won’t make timing. It’s the core of how an FPGA works. Flip-flops can be used to register data every clock cycle, latch data, gate off data, or enable signals.

• **Block Memory :** This memory block is generally on the order of thousands of bits of memory, is configurable in width and depth, and multiple blocks of memory can be chained together to create larger memory elements. ⎞They can generally be configured as either single-port or dual-port random access, or as a FIFO. There will generally be many block memory elements within an FPGA.

• **I/O (Input/Output) :** fpgas will include I/O blocks that allow for various voltage standards as well as timing delay elements to help align multiple signals with one another

• Verilog code for nand gate using gate-level modeling:

```
module nand_2_gate_level(outputy,inputa,b);
wire yd;
and (yd, a, b);
 not(y,yd);
 endmodule
```

• Verilog code for nand gate using data-flow modeling:

```
 modulenand_2_data_flow(outputy,inputa,b);
 assigny=~(a&b);
 endmodule
```

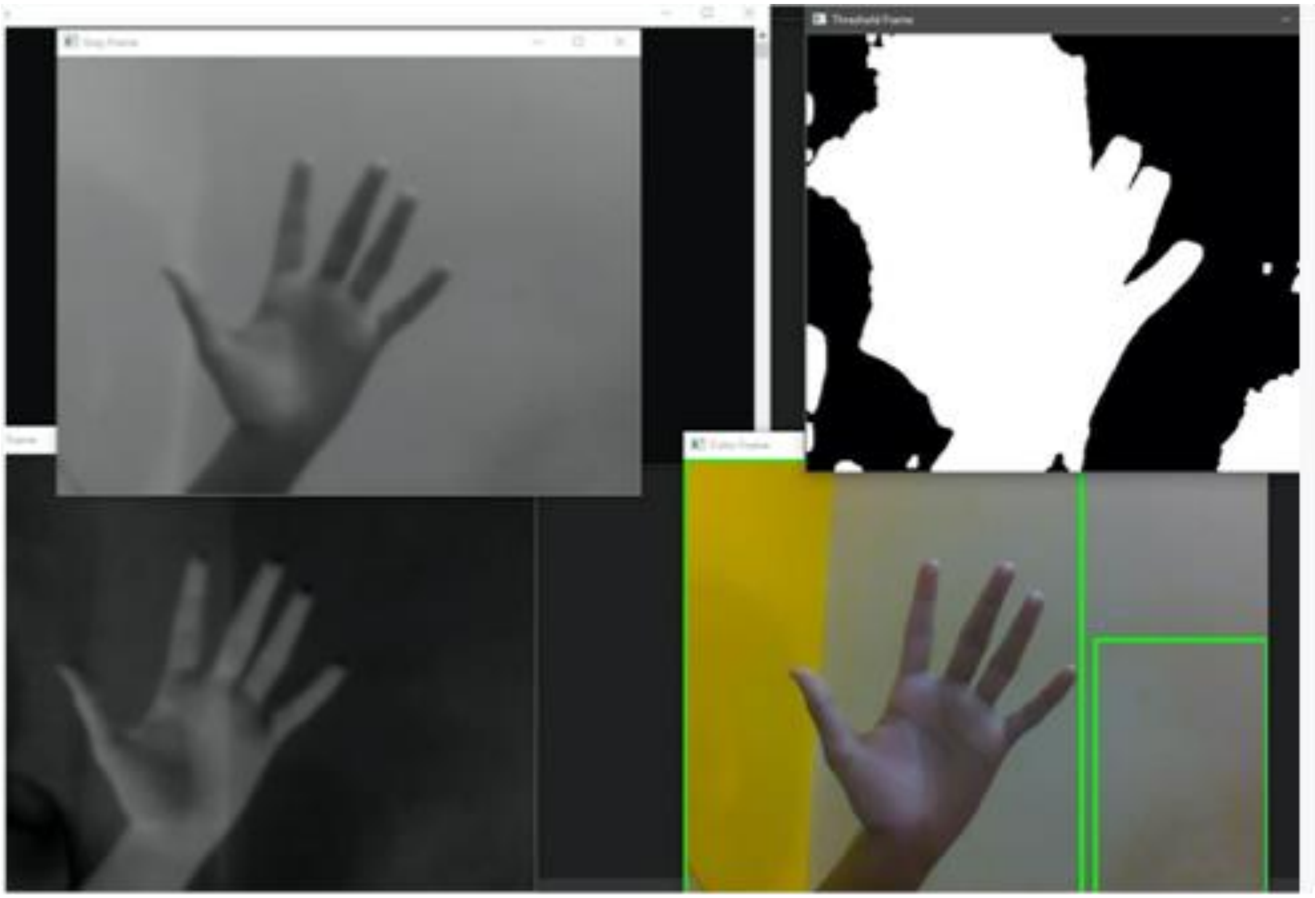
• Verilog code for nand gate using behavioral modeling:

```
 modulenand_2_behavioral(outputregy,inputa,b);
 always@(aorb)begin
 if(a==1'b1&b==1'b1)begin
 y=1'b0;
 end
 else
    y=1'b1;
end
 endmodule
```

Date:	**01 June 2020**	**Name:**	**Kishan shetty**
Course:	**Python**	**USN:**	**4AL17EC041**
Topic:	**Application 6: Build a Webcam Motion Detector**	**Semester & Section:**	**6th sem & A sec**

AFTERNOON SESSION DETAILS

Image of session



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Application 6: Build a Webcam Motion Detector

- **In this Application we learnt about building a Webcam Motion Detector.**
- **Creating Gray scale images and converting it into white and black.**
- **Also having raw colored images to detect motion.**
- **When motion is detected it starts noting the time at which the motion is detected.**
- **And that time and date is stored in excel file**.

• Build a webcam motion detector using OpenCV (cv2 module) library for video capturing, datetime module for noting down the time and pandas library for storing data in a csv file.

• Some of the functions used under cv2 module:

- Images also can contain different types of noise, especially because of the source (camera sensor). Image Smoothing techniques help in reducing the noise. OpenCV provides cv2.GaussianBlur () function to apply Gaussian Smoothing on the input source image.
- The function cv2.absdiff () calculates the per-element absolute difference between two arrays or between an array and a scalar.
- Thresholding is a technique in OpenCV, which is the assignment of pixel values in relation to the threshold value provided. In thresholding, each pixel value is compared with the threshold value. If the pixel value is smaller than the threshold, it is set to 0, otherwise, it is set to a maximum value (generally 255). For this technique cv2.threshold () function is used.
- The cv2.dilate () function dilates an image by using a specific structuring element.
- Contours are defined as the line joining all the points along the boundary of an image that are having the same intensity. Contours come handy in shape analysis, finding the size of the object of interest, and object detection. OpenCV has cv2.findContour () function that helps in extracting the contours from the image. It works best on binary images, so we should first apply thresholding techniques, Sobel edges, etc.
- The cv2.boundingRect () function of OpenCV is used to draw an approximate rectangle around the binary image. This function is used mainly to highlight the region of interest after obtaining contours from an image.

• Pandas pandas.DataFrame () function is a two-dimensional size-mutable, potentially heterogeneous tabular data structure with labeled axes (rows and columns). Pandas DataFrame consists of three principal components, the data, rows, and columns.

• To write DataFrame to a csv file pandas.to_csv () function is used.