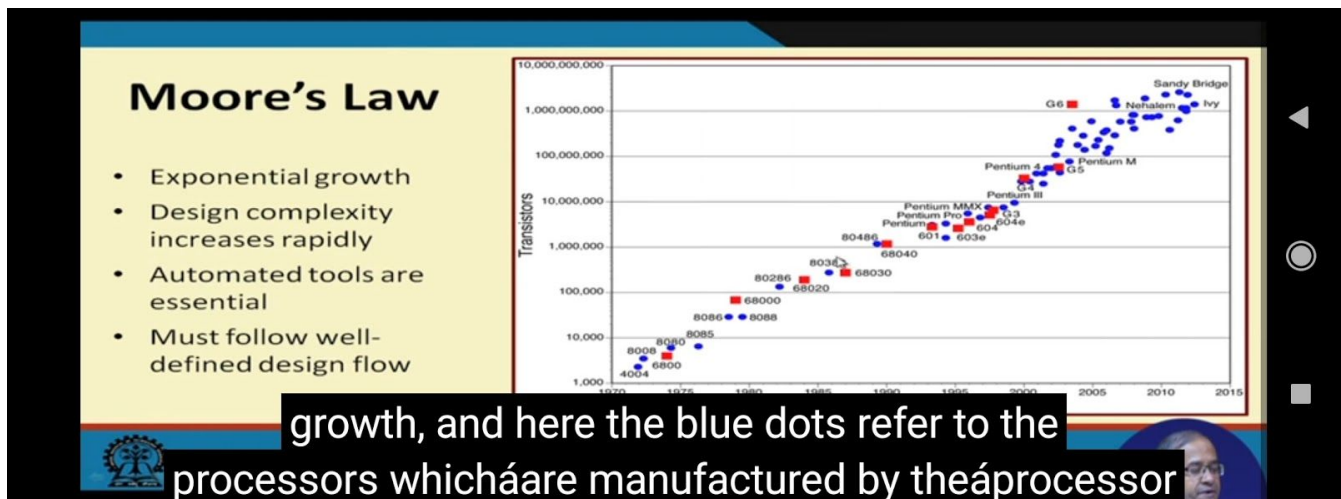
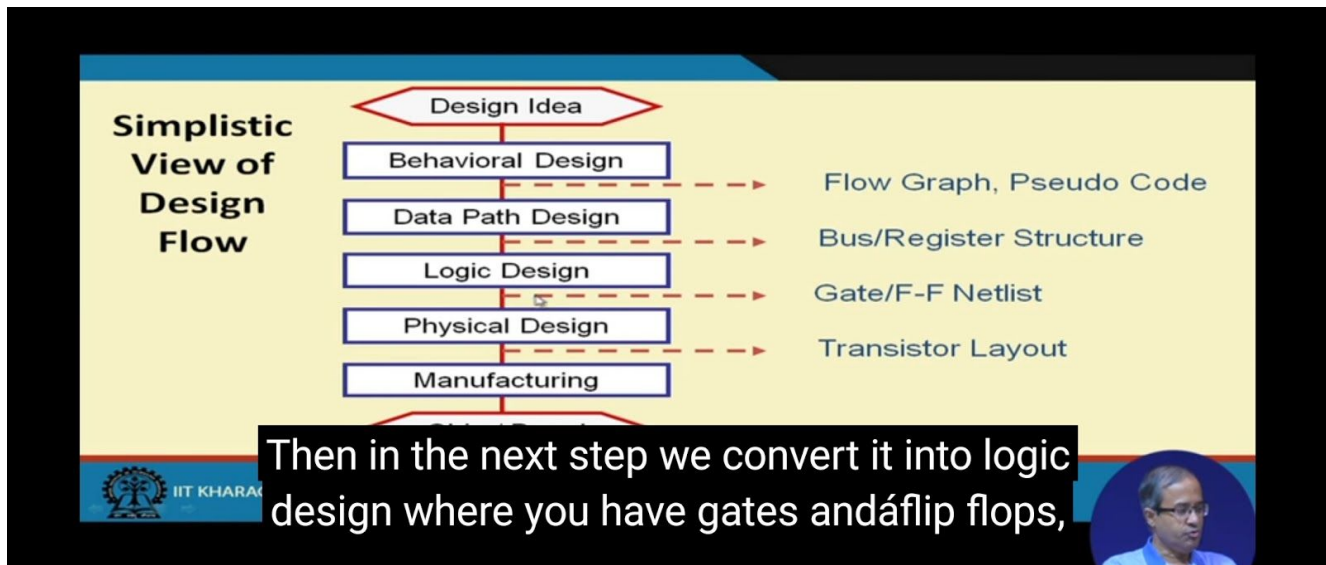


DAILY ASSESSMENT FORMAT

Date:	4-06-2020	Name:	MOUNITHA D M
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC055
Topic:	Hardware modelling using verilog FPGA AND ASIC Interview Question	Semester & Section:	6 TH SEM "A" SEC
Github Repository:	Mounitha_-ec055		

FORENOON SESSION DETAILS

Image of session



Verilog interview Questions & answers for FPGA & ASIC.

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Verilog interview Questions

[Verilog interview Questions page 1](#) [Verilog interview Questions Page 2](#)

[Verilog interview Questions page 3](#) [Verilog interview Questions page 4](#)

Ads by Google [Verilog Examples](#) [Verilog Simulator](#) [Verilog HDL](#)

1) Write a verilog code to swap contents of two registers with and without a temporary register?

With temp reg ;

```
always @ (posedge clock)
begin
temp=b;
b=a;
a=temp;
end
```

Without temp reg;

```
always @ (posedge clock)
begin
a <= b;
b <= a;
end
```

[Click to view more](#)



3) Difference between task and function?

Function:

A function is unable to enable a task however functions can enable other functions.

A function will carry out its required duty in zero simulation time. (The program time will not be incremented during the function routine)

Within a function, no event, delay or timing control statements are permitted

In the invocation of a function their must be at least one argument to be passed.

Functions will only return a single value and can not use either output or inout statement

Tasks:

Tasks are capable of enabling a function as well as enabling other versions of a Task

Tasks also run with a zero simulation however they can if required be executed in non zero simulation time.

Tasks are allowed to contain any of these statements.

A task is allowed to use zero or more arguments which are of type output, input or inout.

A Task is unable to return a value but has the facility to pass multiple values via the output and inout statements .

4) Difference between inter statement and

Report – Report can be typed or hand written for up to two pages.

Day 1 Digital Design using HDL

11/06/2020

Hardware modelling using verilog

- Learn about the verilog hardware description language
- understand the difference between behavioural and structural design
- learn to write test benches and analyze simulation results
- Distinguish between good and bad coding practices

VLSI Design process

- Design complexity increasing rapidly
- Increased size and complexity
- Fabrication technology improving
- CAD tools are essential
- The present trend
 - Standardize the design flow
 - Emphasis on low power design, and increased performance
- Need to use Computer Aided Design (CAD) tools
- Based on Hardware Description Language (HDL)
- HDLs provide formats for representing the outputs of various design steps
- A CAD tool transforms its HDL input into a HDL output that contains more detailed information about the hardware
 - Behavioural level to register transfer level
 - Register transfer level to gate level
 - Transistor level to the layout level.

Two competing HDLs

1 Verilog

2 VHDL

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Designers typically using HDLs, move from one level of abstraction to the next

Data path design

→ Generate a netlist of register transfer level components like registers, adders, multipliers, multiplexers, dividers etc.

A netlist is a directed graph, where the vertices indicate components and the edge indicate interconnection.

A netlist Specification is also referred to as Structural design

Netlist may be specified at various levels, where the components may be functional modules.

Physical design and Manufacturing
Generate final layout that can be sent for fabrication

The layout contains a large number of regular geometric shapes corresponding to the different fabrication layers.

Other steps in the Design Flow

• Simulation for verification

Formal verification

Testability analysis the manufactured device

Write a verilog code to swap contents of two registers with and without a temporary register?

With temp reg;

always @(posedge clock)

begin

temp = b;

b = a;

a = temp;

End

without temp reg;

always @(posedge clock)

begin

a <= b



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task: Implement a simple 1-to-1 multiplexer and test the module using a compiler

```
module tff (input clk, input rstn, input t, output reg q);  
    always @ (posedge clk)  
    begin  
        if (rstn)  
            q <= 0;  
        else  
            if (t)  
                q <= ~q;  
            else  
                q <= q;  
        end  
    end  
endmodule.
```

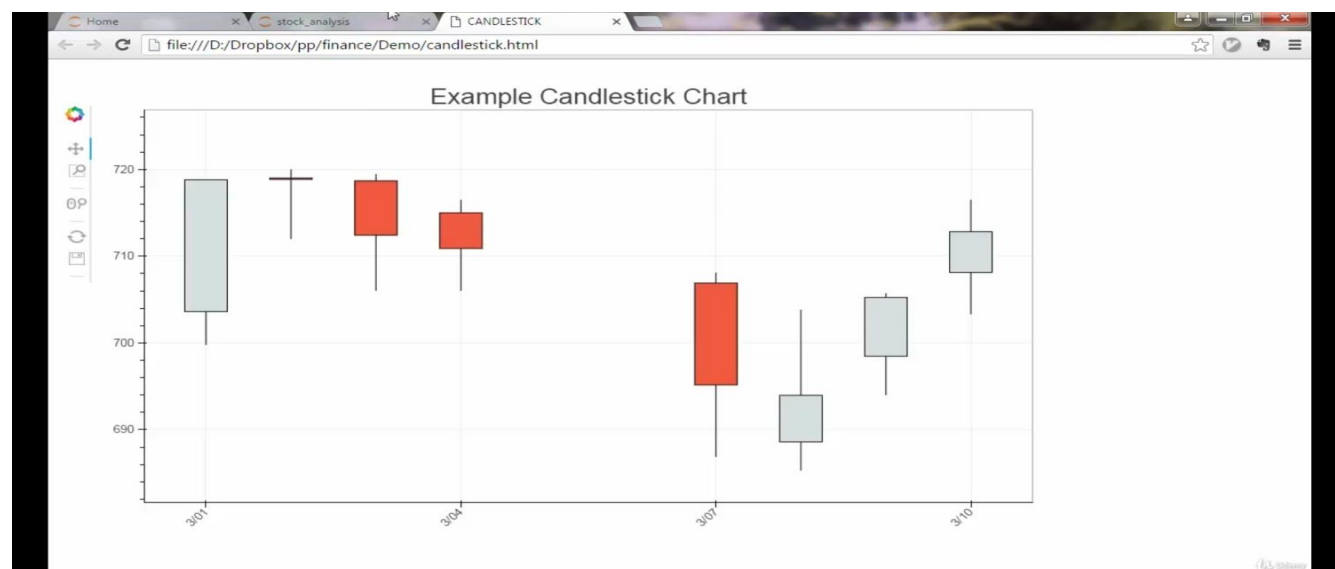
Test bench

```
module tb;  
    reg clk;  
    reg rstn;  
    reg t;  
    tff u0 (clk, rstn, t, q);  
    always #5 clk = ~clk;  
    initial  
        begin  
            rstn <= 0;  
            $monitor ("T = %0t rstn = %0b t = %0d", $time, rstn, t, q);  
            repeat (2) @ (posedge clk);  
            rstn <= 1;  
            for (integer i = 0; i < 20; i = i + 1) begin  
                dly[i] = $random;  
                #(dly) t <= $random;  
            end  
            #20 $finish  
        end  
end  
endmodule.
```

DATE	4-06-2020	Name:	MOUNITHA DM
Course:	PYTHON	USN:	4AL17EC055
Topic:	Application 8:Build a web-based Financial Graph	Semester & Section:	6 TH SEM "A" SEC

AFTERNOON SESSION DETAILS

Image of session



Remote Data Access — p X Home X stock_analysis X Symbol Lookup from Yali X

← → https://pandas-datareader.readthedocs.org/en/latest/remote_data.html#world-bank ☆ 🔍 ☰

pandas-datareader

latest

Search docs

What's New

Remote Data Access

⊞ Yahoo! Finance

Google Finance

FRED

Fama/French

⊞ World Bank

Indicators

Country Codes

Problematic Country Codes & Indicators

OECD

Eurostat

EDGAR Index

Caching queries

Read the Docs

v:latest ▼

Either from exploring the World Bank site, or using the search function included, every world bank indicator is accessible.

For example, if you wanted to compare the Gross Domestic Products per capita in constant dollars in North America, you would use the `search` function:

```
In [1]: from pandas_datareader import wb

In [2]: wb.search('gdp.*capita.*const').iloc[:, :2]
Out[2]:
```

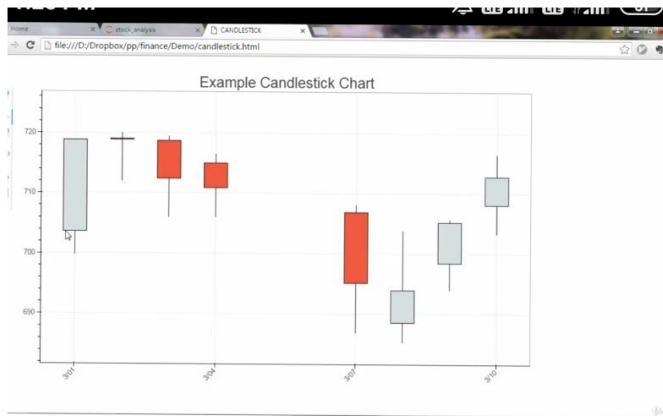
	id	name
3242	GDP.PCAP.KD	GDP per Capita, constant US\$, millions
5143	NY.GDP.PCAP.KD	GDP per capita (constant 2005 US\$)
5145	NY.GDP.PCAP.KN	GDP per capita (constant LCU)
5147	NY.GDP.PCAP.PP.KD	GDP per capita, PPP (constant 2005 internation...

Then you would use the `download` function to acquire the data from the World Bank's servers:

```
In [3]: dat = wb.download(indicator='NY.GDP.PCAP.KD', country=['US', 'CA', 'MX'], start=2005, end=2008)

In [4]: print(dat)
```

		NY.GDP.PCAP.KD
country	year	
Canada	2008	36005.5004978584
	2007	36182.9138439757
	2006	35785.9698172849
	2005	35087.8925933298
Mexico	2008	8113.10219480083
	2007	8119.21298908649
	2006	7961.96818458178
	2005	7666.60796097764



```

jupyter stock_analysis Last checkpoint Last Saturday at 5:22 PM (autosaved)
File Edit View Insert Cell Kernel Help Python 3
Code Cell Toolbar Home
p.segment(df.index, df.High, df.Low, df.Low, color="black")
p.rect(df.index[df.Status=="Increase"], df.High[df.Status=="Increase"],
      hours_12, df.High[df.Status=="Increase"], fill_color="W", line_color="black")
p.rect(df.index[df.Status=="Decrease"], df.Low[df.Status=="Decrease"],
      hours_12, df.Low[df.Status=="Decrease"], fill_color="W", line_color="black")

script1, div = components(p)
cdn_js_files
cdn_css_files
show()

In [18]: type(script1)
Out[18]: str
In [19]: cdn_js[0]
Out[19]: 'https://cdn.pydata.org/bokeh/release/bokeh-0.11.1.min.js'
In [20]: cdn_css[0]
Out[20]: 'https://cdn.pydata.org/bokeh/release/bokeh-0.11.1.min.css'

```

Lectures More

Section 31 - Application 9: Build a Web-based Financial ...

- 246 ☒ Web-based Financial Graph - How...
Video - 01:59 mins - Resources (1)
- 247 ☒ Downloading Datasets with Python
Video - 11:32 mins
- 248 ☒ Stock Market Data
Video - 03:25 mins
- 249 ☒ Stock Market Data Candlestick Ch...
Video - 05:39 mins
- 250 ☒ Candlestick Charts with Bokeh Quad...
Video - 10:17 mins
- 251 ☒ Candlestick Charts with Bokeh Rect...
Video - 22:28 mins
- 252 ☒ Candlestick Segments
Video - 05:02 mins

Lectures More

- 250 ☒ Candlestick Charts with Bokeh Qu...
Video - 10:17 mins
- 251 ☒ Candlestick Charts with Bokeh R...
Video - 22:28 mins
- 252 ☒ Candlestick Segments
Video - 05:02 mins
- 253 ☒ Stylizing the Chart
Video - 04:24 mins
- 254 The Concept Behind Embedding Bok...
Video - 11:04 mins
- 255 Note
Article
- 256 ☒ Embedding the Bokeh Chart in a ...
Video - 15:32 mins
- 257 Deploying the Chart Website to a Liv...
Video - 08:31 mins - Resources (1)

Report – Report can be typed or hand written for up to two pages.

Day 15 Python 11/06/2020

Application 8: Build a web based Financial Graph.

web based financial Graph

Downloading datasets with python

```
from pandas_datareader import data
import datetime
data = DataReader(name = "AAPL", data_source = "Yahoo",
```

Start - dutetime, dotetime

$df = \text{data_time, datetime} (2016, 3, 10)$

```
df = data.DataReader(name = "AAPL", data-source  
= "Yahoo", start, end = end)
```

Stock Market Data

```
Start = datetime.datetime(2016, 3, 1)
```

End = datetime.datetime(2016, 3, 10)

Stock Market Data Dashboard

candlestick charts with Boleh Quadrant

$$df_index \text{ cdf.close} > df_open$$

```
date_time_index(['2016-03-01', '2016-03-08', '2016-03-10'])
```

```
dtype 'datetime64[ns]', name 'Date', fuser = 10000
```

P = figure(x_axis_type = 'date time', width = 1000, height = 300)

P. quad

p. of word

candlestick chart with Bollinger Bands

Cardinality of Index [df.close ≥ df.open], $(df.open + df.close)/2$

chown -12, abs (df - open = df - close), fill - color = "green",
line - color = "black")

$$next[dt.index[dt.close < dt.open]](dt.open + dt.close)/2$$

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