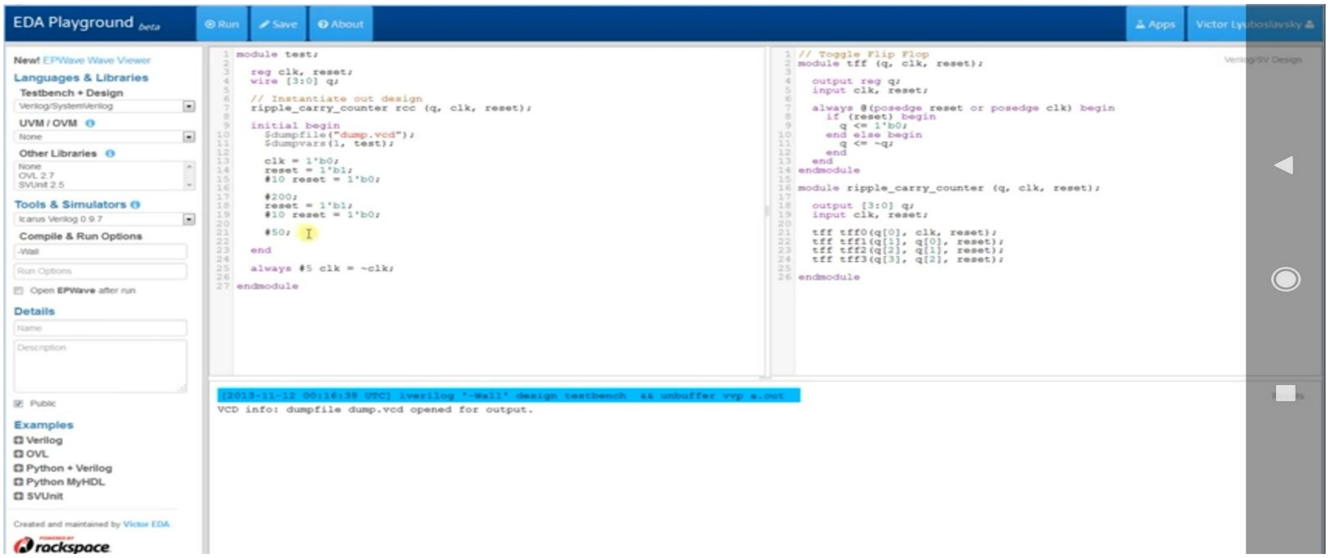
DAILY ASSESSMENT FORMAT

Date:	3-06-2020	Name:	MOUNITHA D M
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC055
Topic:	EDA Playground Tutorial Demo Video How to Download and Install Xilinx Vivado Design Suite Vivado Design for Implemenation HDL code	Semester & Section:	6TH SEM "A" SEC
Github Repository:	Mounitha_-ec055		

FORENOON SESSION DETAILS

Image of session



```
module test;

  reg clk, reset;
  wire [3:0] q;

  // Instantiate out design
  ripple_carry_counter rcc (q, clk, reset);

  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1, test);

    clk = 1'b0;
    reset = 1'b1;
    #10 reset = 1'b0;

    #200;
    reset = 1'b1;
    #10 reset = 1'b0;

    #50;

  end

  always #5 clk = ~clk;

endmodule
```

```
// Toggle Flip Flop
module tff (q, clk, reset);

  output reg q;
  input clk, reset;

  always @(posedge reset or posedge clk) begin
    if (reset) begin
      q <= 1'b0;
    end else begin
      q <= ~q;
    end
  end
endmodule

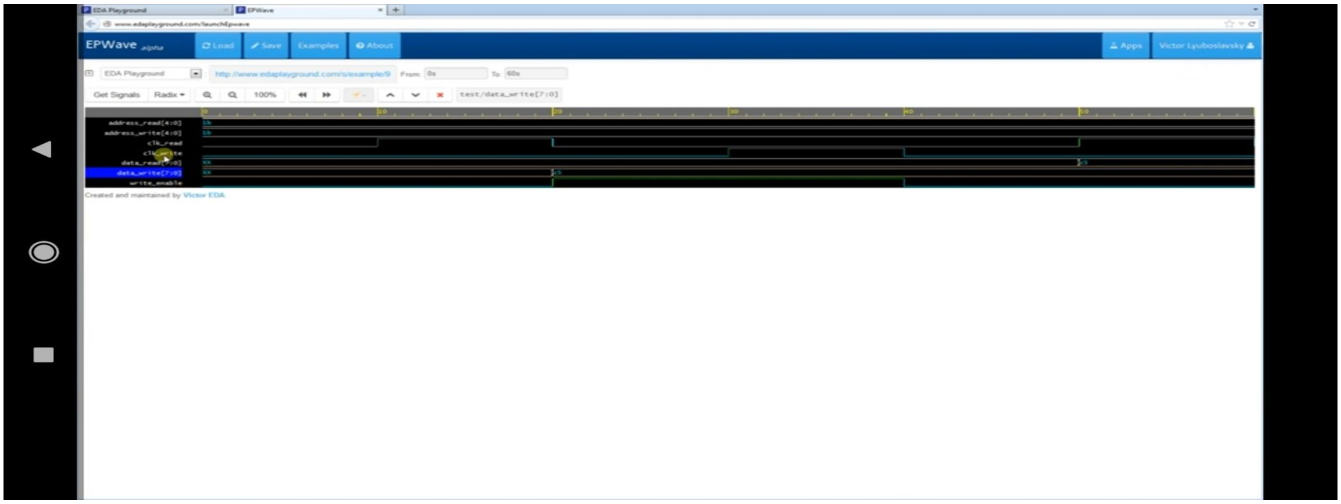
module ripple_carry_counter (q, clk, reset);

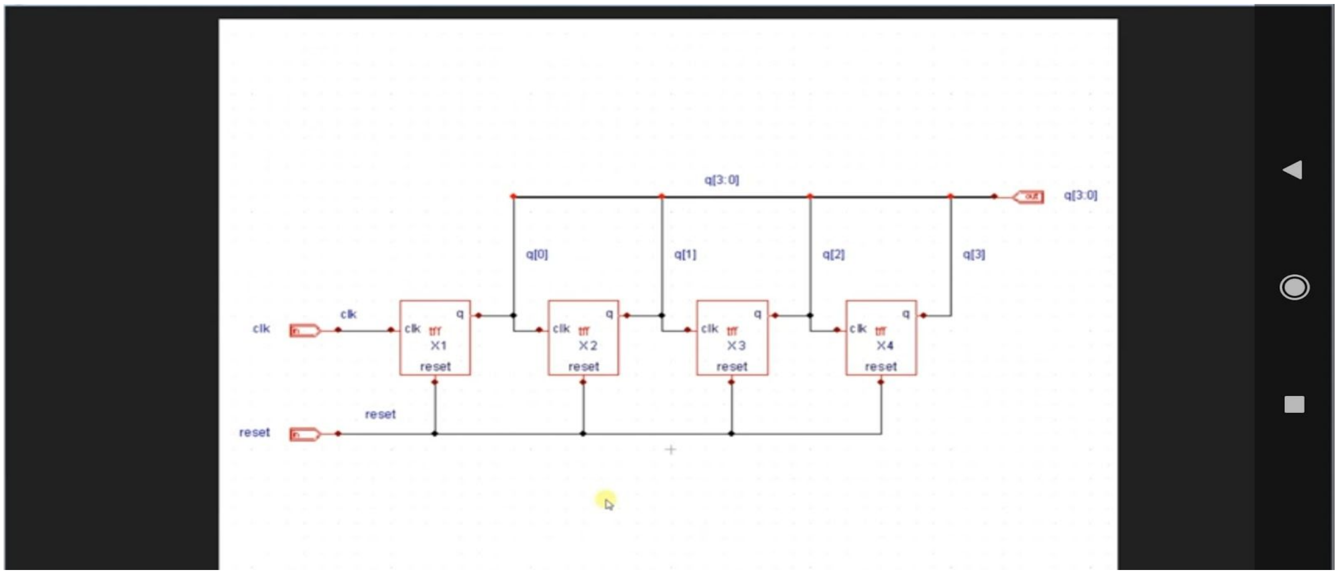
  output [3:0] q;
  input clk, reset;

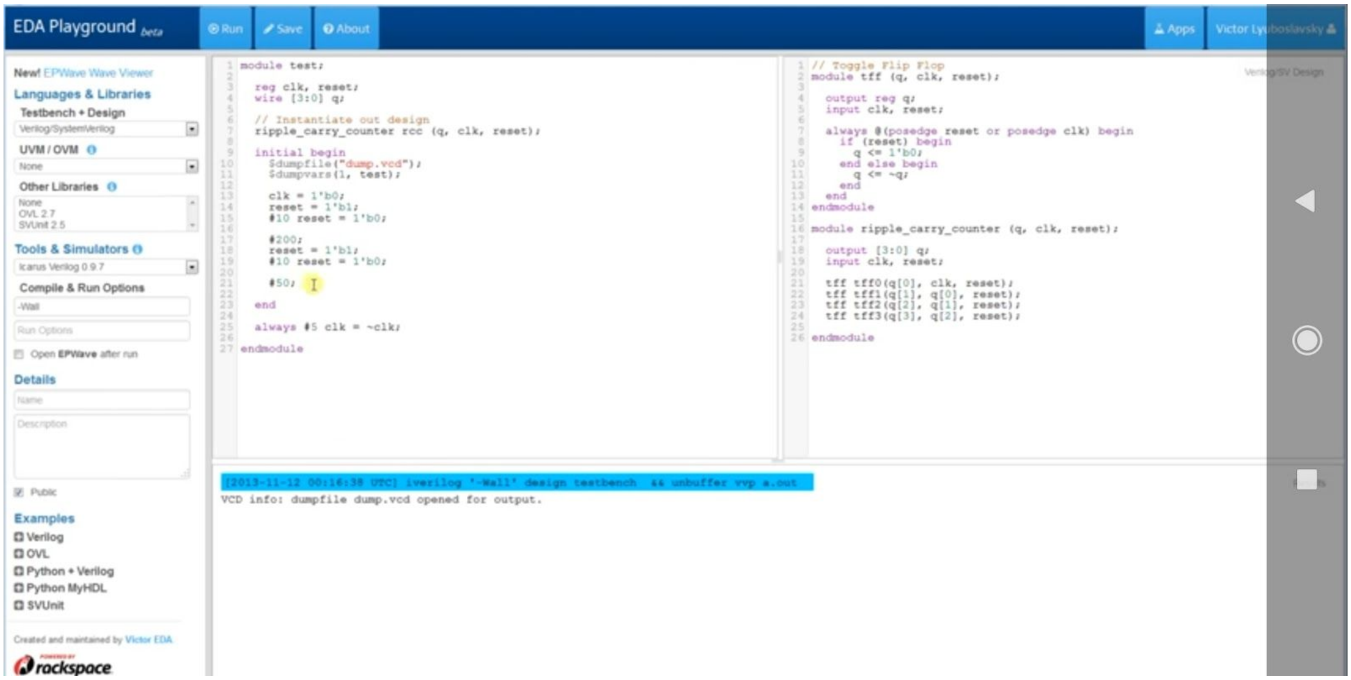
  tff tff0(q[0], clk, reset);
  tff tff1(q[1], q[0], reset);
  tff tff2(q[2], q[1], reset);
  tff tff3(q[3], q[2], reset);

endmodule
```

```
[2013-11-12 00:16:38 UTC] iverilog '-Wall' design testbench  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
```







Testbench + Design: Verilog/SystemVerilog

UVM / OVM: None

Other Libraries: None, OVL 2.7, SVUnit 2.5

Tools & Simulators: Icarus Verilog 0.9.7

Compile & Run Options: -Wall

Run Options

□ Open EPWave after run

Details

Name

Description

☑ Public

```
module test;

  reg clk, reset;
  wire [3:0] q;

  // Instantiate out design
  ripple_carry_counter rcc (q, clk, reset);

  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1, test);

    clk = 1'b0;
    reset = 1'b1;
    #10 reset = 1'b0;

    #200;
    reset = 1'b1;
    #10 reset = 1'b0;

    #50;

  end

  always #5 clk = ~clk;

endmodule
```

```
// Toggle Flip Flop
module tff (q, clk, reset);

  output reg q;
  input clk, reset;

  always @(posedge reset or posedge clk) begin
    if (reset) begin
      q <= 1'b0;
    end else begin
      q <= ~q;
    end
  end
endmodule

module ripple_carry_counter (q, clk, reset);

  output [3:0] q;
  input clk, reset;

  tff tff0(q[0], clk, reset);
  tff tff1(q[1], q[0], reset);
  tff tff2(q[2], q[1], reset);
  tff tff3(q[3], q[2], reset);

endmodule
```

```
[2013-11-12 00:16:38 UTC] iverilog '-Wall' design testbench  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
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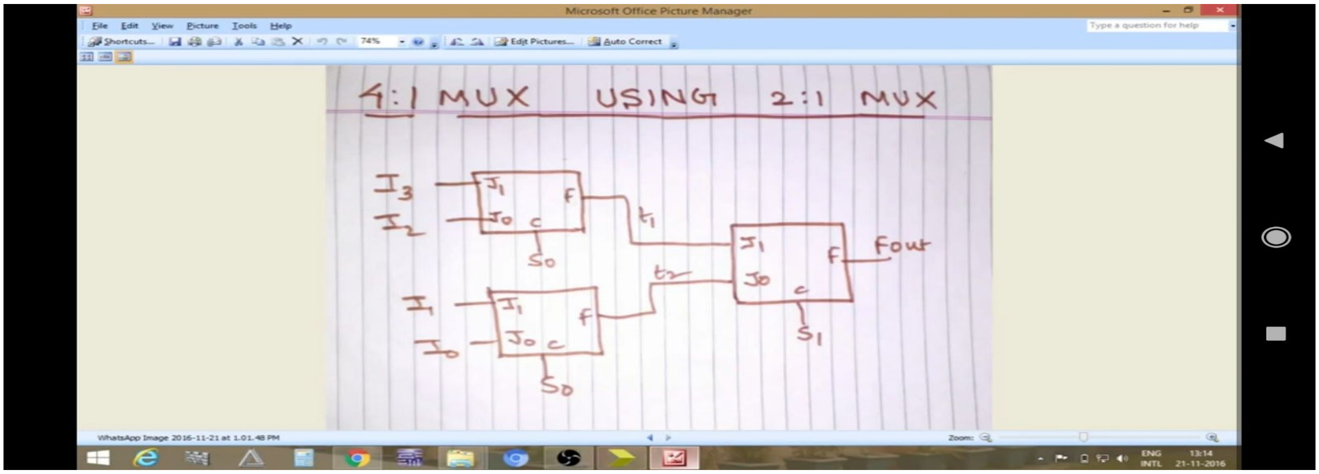
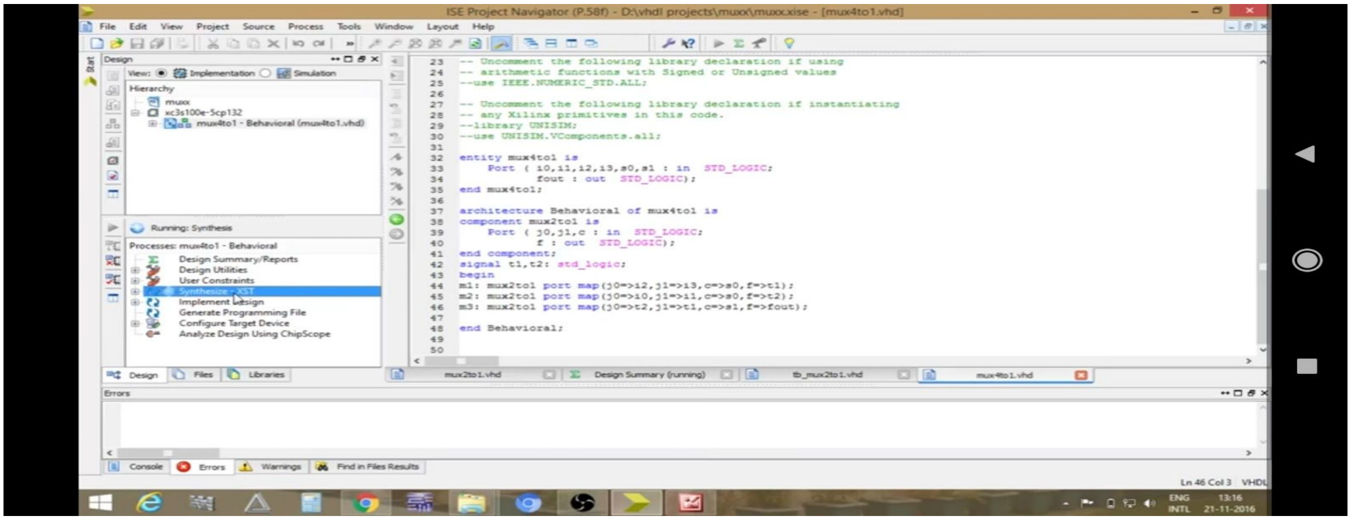


4:1 MUX USING 2:1 MUX



ISE Project Navigator (P.58f) - D:\vhdl projects\muxx\muxx.xise - [mux4to1.vhd]
mux4to1 - Behavioral (mux4to1.vhd)
Running: Synthesis
mux2to1.vhd
Design Summary (running)
tb_mux2to1.vhd
mux4to1.vhd

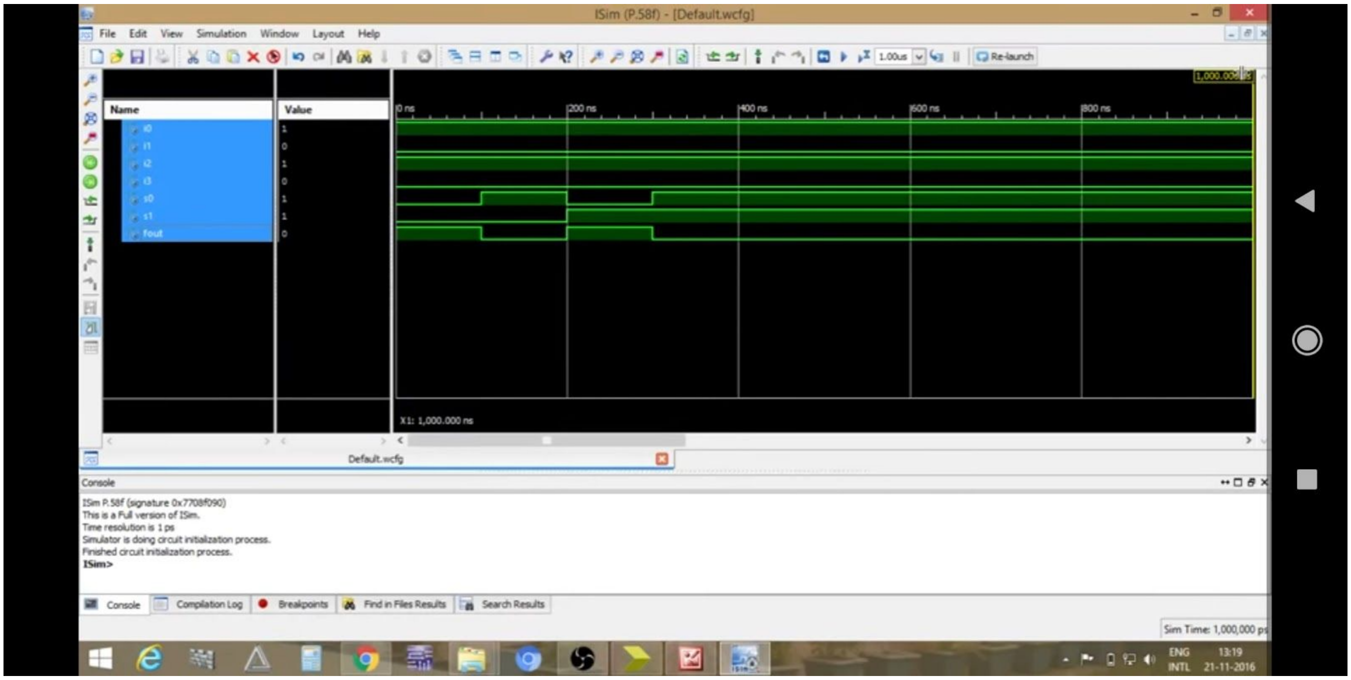
```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mux4to1 is
    Port ( i0,i1,i2,i3,s0,s1 : in  STD_LOGIC;
           fout : out  STD_LOGIC);
end mux4to1;

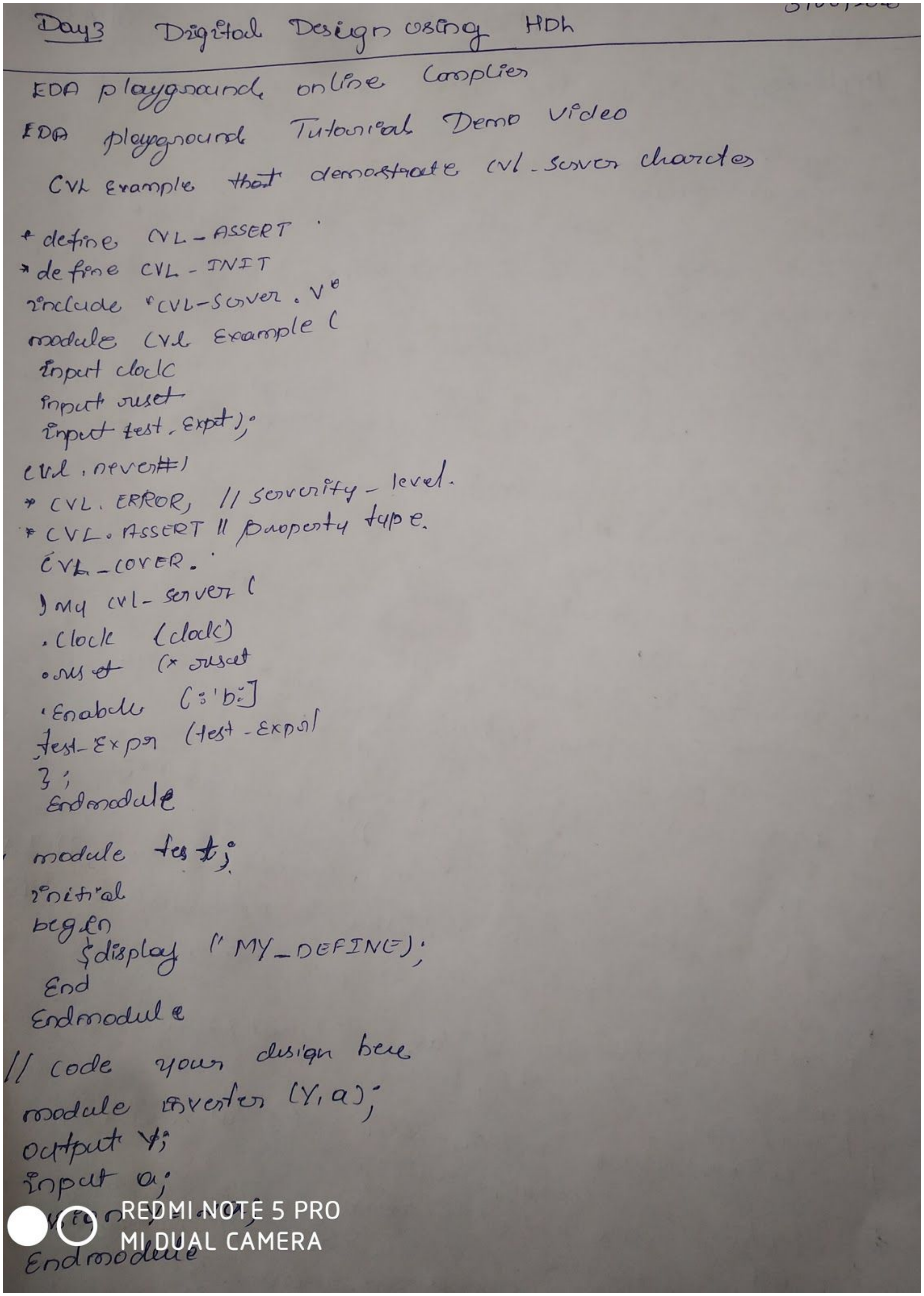
architecture Behavioral of mux4to1 is
component mux2to1 is
    Port ( j0,j1,c : in  STD_LOGIC;
           f : out  STD_LOGIC);
end component;
signal t1,t2: std_logic;
begin
m1: mux2to1 port map(j0=>i2,j1=>i3,c=>s0,f=>t1);
m2: mux2to1 port map(j0=>i0,j1=>i1,c=>s0,f=>t2);
m3: mux2to1 port map(j0=>t2,j1=>t1,c=>s1,f=>fout);

end Behavioral;
```



```
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Report – Report can be typed or hand written for up to two pages.



Day3 Digital Design using HDL

EDA playground online Compiler

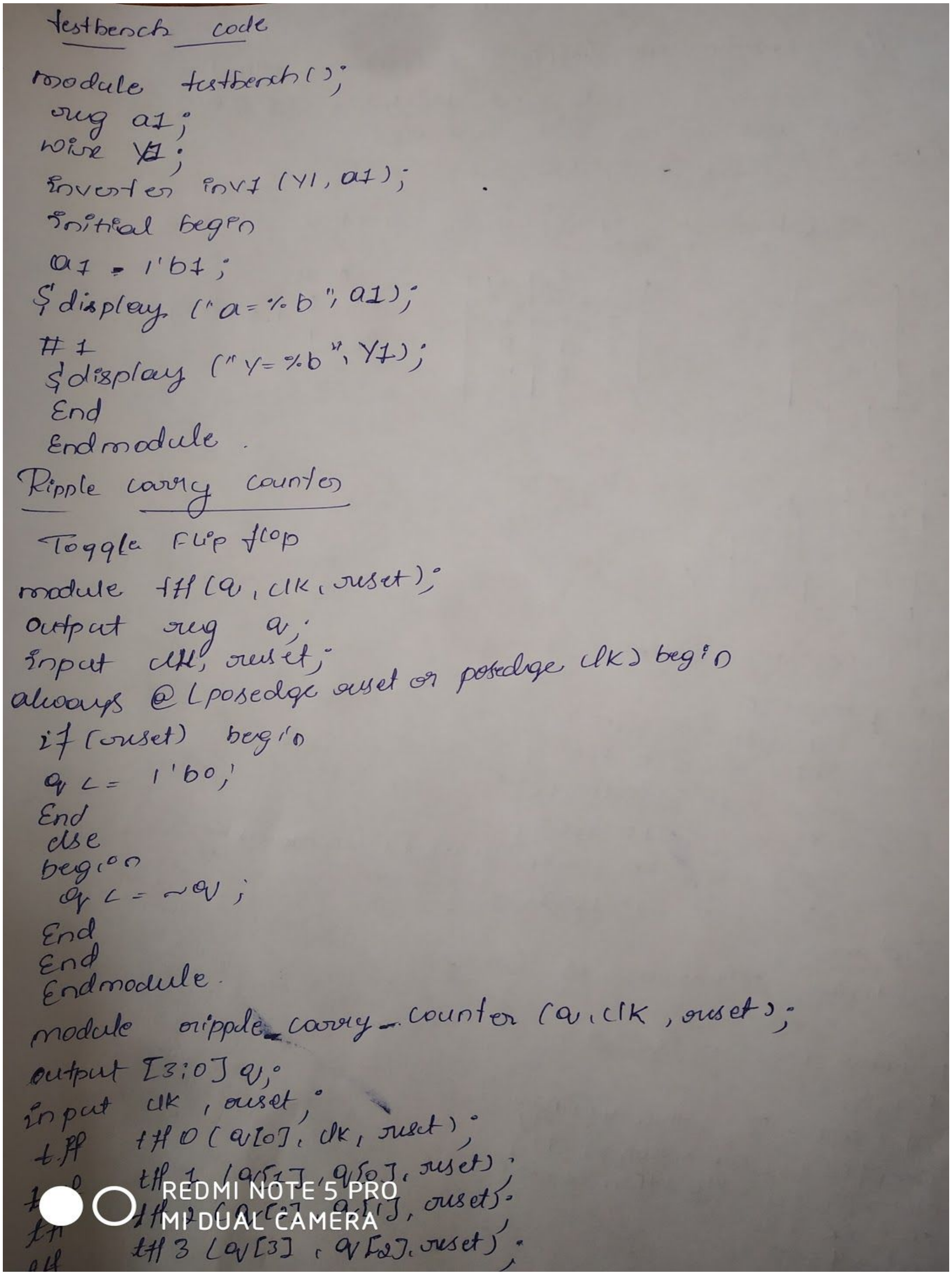
EDA playground Tutorial Demo video

CVL Example that demostrate cvl_server charactes

```
* define CVL-ASSERT
* define CVL-INIT
include "CVL-Server.v"
module CVL Example (
 input clock
 input reset
 input test, Expt);
cvl.never#)
* CVL.ERROR, // severity-level.
* CVL.ASSERT // property type.
 CVL-COVER.
 ) My cvl-server (
 .clock (clock)
 .reset (~ reset
 .Enable [1'b1]
 test-Expr (test-Expr)
 );
 Endmodule

module test;
initial
begin
   $display ("MY_DEFINE);
 End
Endmodule

// code your design here
module inverter (Y, a);
output Y;
input a;
[illegible]
Endmodule
```



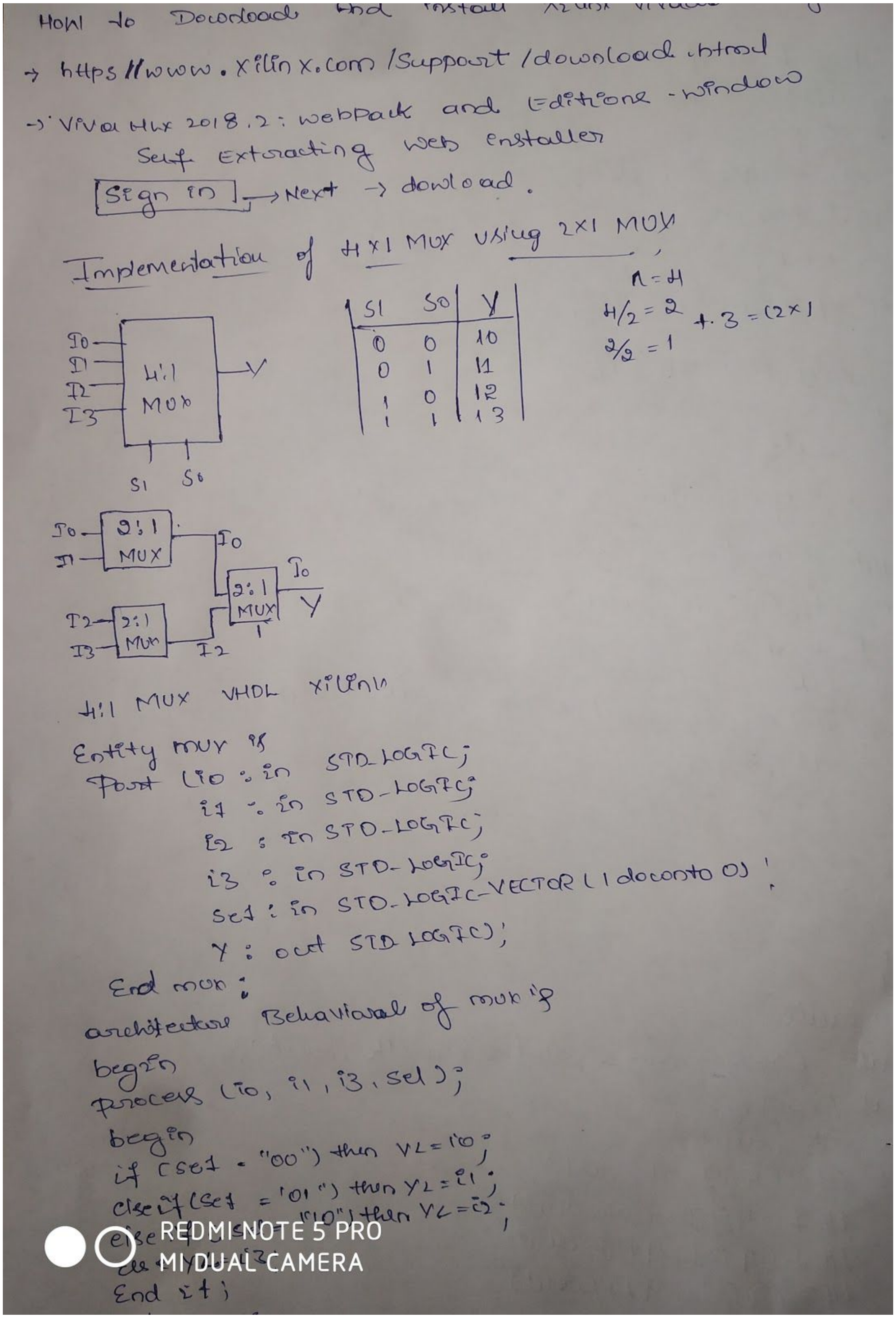
testbench code

```
module testbench();
 reg a1;
wire Y1;
 inverter inv1 (Y1, a1);
 initial begin
 a1 = 1'b1;
$display ("a=%b", a1);
 #1
 $display ("Y=%b", Y1);
 End
 Endmodule.
```

Ripple carry counter

Toggle Flip flop

```
module tff (q, clk, reset);
output reg q;
input clk, reset;
always @ (posedge reset or posedge clk) begin
 if (reset) begin
 q <= 1'b0;
 End
 else
 begin
  q <= ~q;
 End
 End
 Endmodule.
module ripple_carry_counter (q, clk, reset);
output [3:0] q;
input clk, reset;
t ff    tff0 (q[0], clk, reset);
tff     tff1 (q[1], q[0], reset);
tff     tff2 (q[2], q[1], reset);
tff     tff3 (q[3], q[2], reset);
tff
```



How to Dowoload And install xilinx vivado

→ https//www.xilinx.com/Support/download.html

→ Viva HLx 2018.2: webPack and Editione - window
Self Extracting web enstaller
[Sign in] → Next → dowload.

Implementation of 4×1 MUX using 2×1 MUX

I0
I1
I2
I3
4:1
MUX
Y
S1
S0

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

$n = 4$

$4/2 = 2$ + 3 = (2×1

$2/2 = 1$

I0
I1
2:1
MUX
I0
2:1
MUX
I0
Y
I2
I3
2:1
MUX
I2

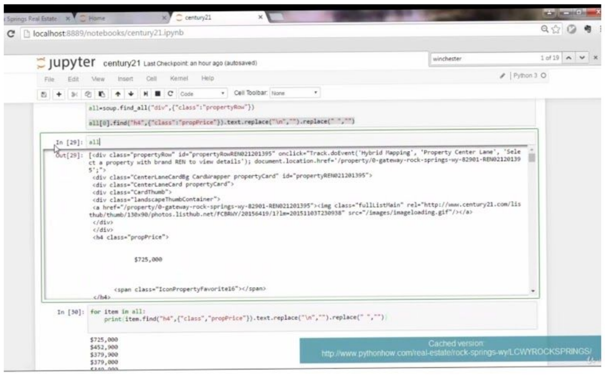
4:1 MUX VHDL xilinx

```
Entity mux is
 Port (i0 : in  STD_LOGIC;
       i1 : in STD_LOGIC;
       i2 : in STD_LOGIC;
       i3 : in STD_LOGIC;
       sel : in STD_LOGIC_VECTOR (1 downto 0);
       Y : out STD_LOGIC);
 End mux;
architecture Behavioral of mux is
begin
process (i0, i1, i3, sel);
 begin
 if (sel . "00") then Y<=i0;
 else if (sel = '01") then Y<=i1;
 else if (sel = "10") then Y<=i2;
 else Y<=i3
 End if;
```

DATE	**3-06-2020**	**Name:**	**MOUNITHA DM**
Course:	**PYTHON**	**USN:**	**4AL17EC055**
Topic:	**Application7:Scrape Real Estate Property Data from the web**	**Semester & Section:**	**6TH SEM "A" SEC**

AFTERNOON SESSION DETAILS

Image of session


Springs Real Estate
Home
century21
localhost:8889/notebooks/century21.ipynb
jupyter century21 Last Checkpoint: an hour ago (autosaved)
winchester 1 of 19
File Edit View Insert Cell Kernel Help
Python 3
Code
Cell Toolbar: None

```
all=soup.find_all("div",{"class":"propertyRow"})

all[0].find("h4",{"class":"propPrice"}).text.replace("\n","").replace(" ","")

In [29]: all

Out[29]: [<div class="propertyRow" id="propertyRowREN021201395" onclick="Track.doEvent('Hybrid Mapping', 'Property Center Lane', 'Sele
         ct a property with brand REN to view details'); document.location.href='/property/0-gateway-rock-springs-wy-82901-REN02120139
         5';">
          <div class="CenterLaneCardBg CardWrapper propertyCard" id="propertyREN021201395">
          <div class="CenterLaneCard propertyCard">
          <div class="CardThumb">
          <div class="landscapeThumbContainer">
          <a href="/property/0-gateway-rock-springs-wy-82901-REN021201395"><img class="fullListMain" rel="http://www.century21.com/lis
         thub/thumb/130x90/photos.listhub.net/FCBRWY/20156419/1?lm=20151103T230938" src="/images/imageloading.gif"/></a>
          </div>
          </div>
          <h4 class="propPrice">


                 $725,000

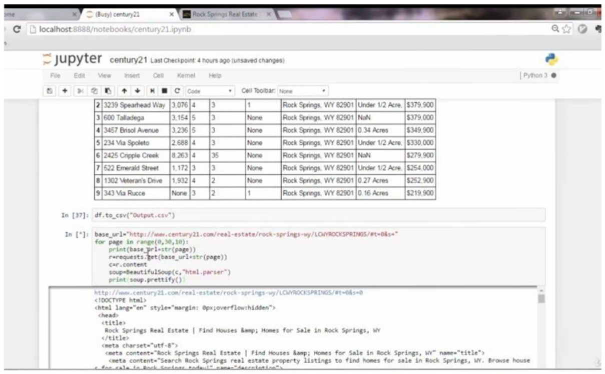


              <span class="IconPropertyFavorite16"></span>
          </h4>

In [30]: for item in all:
             print(item.find("h4",{"class","propPrice"}).text.replace("\n","").replace(" ",""))

         $725,000
         $452,900
         $379,900
         $379,000
```

Cached version:
http://www.pythonhow.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/

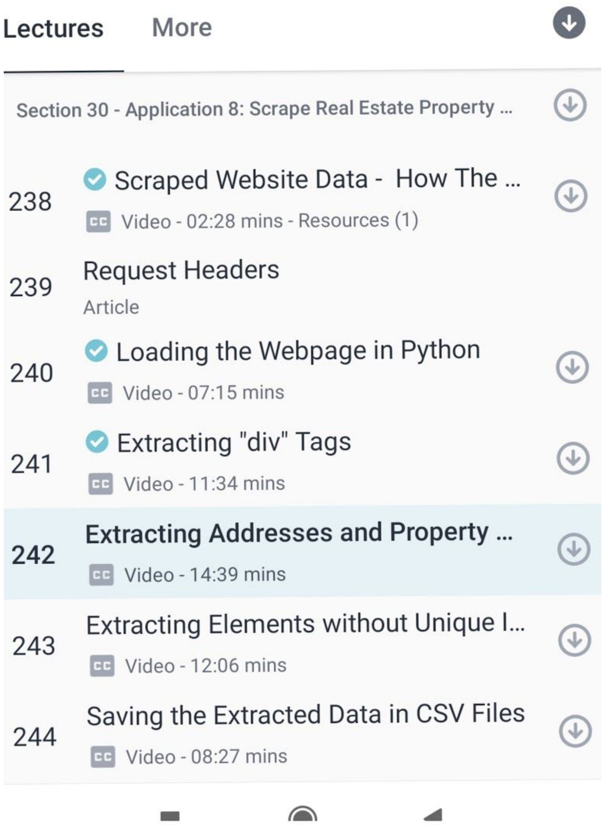

(Busy) century21
Rock Springs Real Estate
localhost:8888/notebooks/century21.ipynb
jupyter century21 Last Checkpoint: 4 hours ago (unsaved changes)
File Edit View Insert Cell Kernel Help
Python 3
Code
Cell Toolbar: None

2	3239 Spearhead Way	3,076	4	3	1	Rock Springs, WY 82901	Under 1/2 Acre,	$379,900
3	600 Talladega	3,154	5	3	None	Rock Springs, WY 82901	NaN	$379,000
4	3457 Brisol Avenue	3,236	5	3	None	Rock Springs, WY 82901	0.34 Acres	$349,900
5	234 Via Spoleto	2,688	4	3	None	Rock Springs, WY 82901	Under 1/2 Acre,	$330,000
6	2425 Cripple Creek	8,263	4	35	None	Rock Springs, WY 82901	NaN	$279,900
7	522 Emerald Street	1,172	3	3	None	Rock Springs, WY 82901	Under 1/2 Acre,	$254,000
8	1302 Veteran's Drive	1,932	4	2	None	Rock Springs, WY 82901	0.27 Acres	$252,900
9	343 Via Rucce	None	3	2	1	Rock Springs, WY 82901	0.16 Acres	$219,900

```
In [37]: df.to_csv("Output.csv")

In [*]: base_url="http://www.century21.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/#t=0&s="
        for page in range(0,30,10):
            print(base_url+str(page))
            r=requests.get(base_url+str(page))
            c=r.content
            soup=BeautifulSoup(c,"html.parser")
            print(soup.prettify())

        http://www.century21.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/#t=0&s=0
        <!DOCTYPE html>
        <html lang="en" style="margin: 0px;overflow:hidden">
         <head>
          <title>
           Rock Springs Real Estate | Find Houses &amp; Homes for Sale in Rock Springs, WY
          </title>
          <meta charset="utf-8">
           <meta content="Rock Springs Real Estate | Find Houses &amp; Homes for Sale in Rock Springs, WY" name="title">
            <meta content="Search Rock Springs real estate property listings to find homes for sale in Rock Springs, WY. Browse house
```



Section 30 - Application 8: Scrape Real Estate Property ...

238 Scraped Website Data - How The ...
Video - 02:28 mins - Resources (1)

239 Request Headers
Article

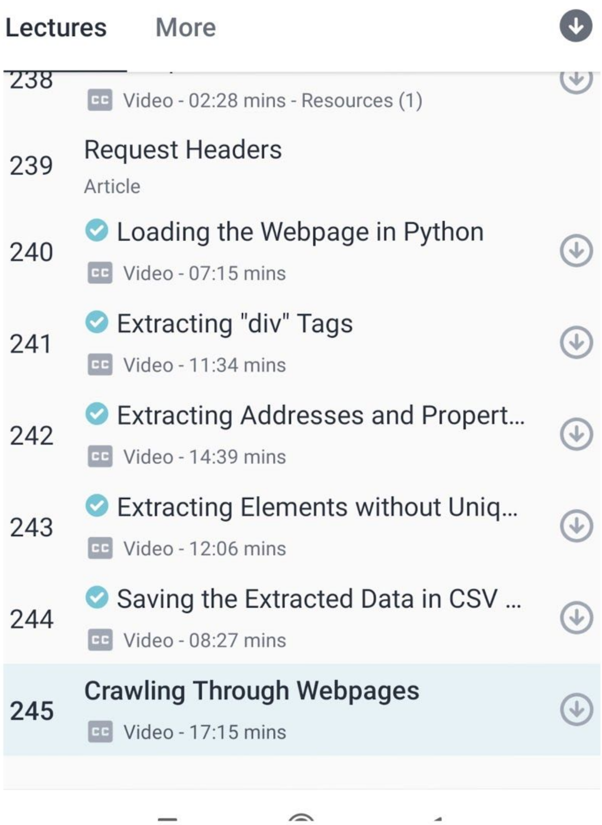
240 Loading the Webpage in Python
Video - 07:15 mins

241 Extracting "div" Tags
Video - 11:34 mins

242 Extracting Addresses and Property ...
Video - 14:39 mins

243 Extracting Elements without Unique I...
Video - 12:06 mins

244 Saving the Extracted Data in CSV Files
Video - 08:27 mins



238
Video - 02:28 mins - Resources (1)

239 Request Headers
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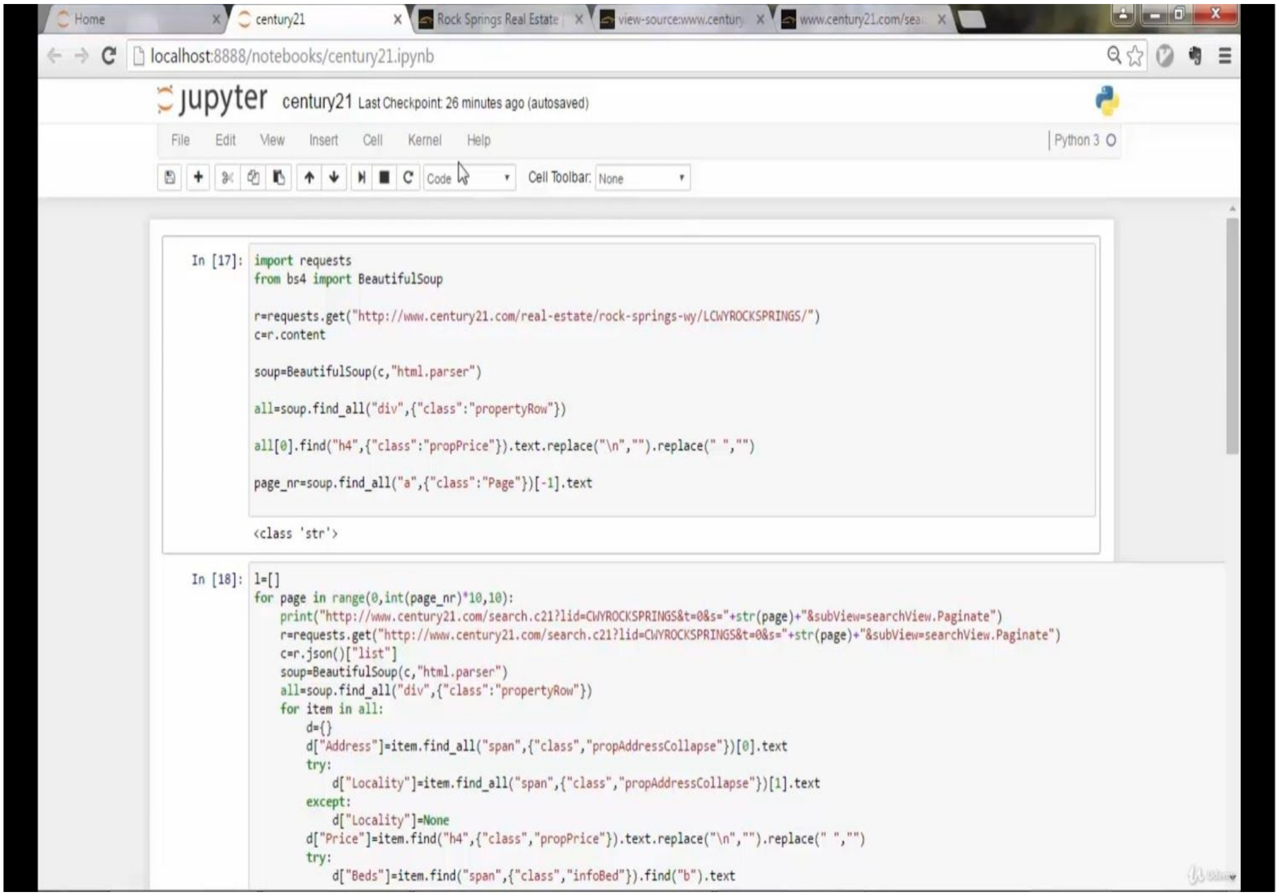
Video - 14:39 mins

243 Extracting Elements without Uniq...
Video - 12:06 mins

244 Saving the Extracted Data in CSV ...
Video - 08:27 mins

245 Crawling Through Webpages
Video - 17:15 mins



In [17]:

```
import requests
from bs4 import BeautifulSoup

r=requests.get("http://www.century21.com/real-estate/rock-springs-wy/LCWYROCKSPRINGS/")
c=r.content

soup=BeautifulSoup(c,"html.parser")

all=soup.find_all("div",{"class":"propertyRow"})

all[0].find("h4",{"class":"propPrice"}).text.replace("\n","").replace(" ","")

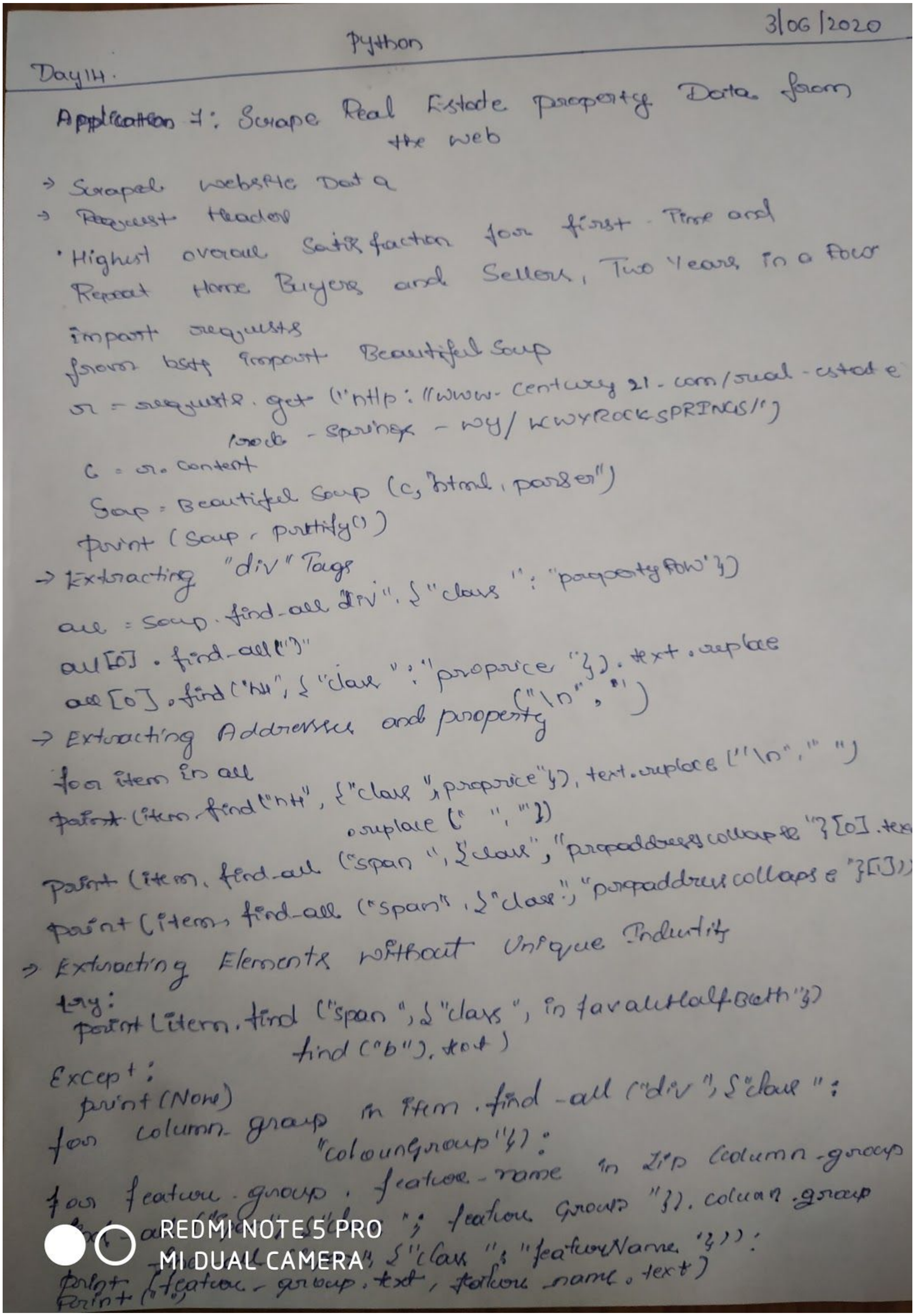
page_nr=soup.find_all("a",{"class":"Page"})[-1].text
```

```
<class 'str'>
```

In [18]:

```
l=[]
for page in range(0,int(page_nr)*10,10):
    print("http://www.century21.com/search.c21?lid=CWYROCKSPRINGS&t=0&s="+str(page)+"&subView=searchView.Paginate")
    r=requests.get("http://www.century21.com/search.c21?lid=CWYROCKSPRINGS&t=0&s="+str(page)+"&subView=searchView.Paginate")
    c=r.json()["list"]
    soup=BeautifulSoup(c,"html.parser")
    all=soup.find_all("div",{"class":"propertyRow"})
    for item in all:
        d={}
        d["Address"]=item.find_all("span",{"class","propAddressCollapse"})[0].text
        try:
            d["Locality"]=item.find_all("span",{"class","propAddressCollapse"})[1].text
        except:
            d["Locality"]=None
        d["Price"]=item.find("h4",{"class","propPrice"}).text.replace("\n","").replace(" ","")
        try:
            d["Beds"]=item.find("span",{"class","infoBed"}).find("b").text
```

Report – Report can be typed or hand written for up to two pages.



3|06|2020

Python

Day14.

Application 7: Scrape Real Estate property Data from the web

- → Scrapel website Dat a
- → Request Header
- Highest overall Satisfaction for first - Time and Repeat Home Buyers and Sellers, Two Years in a Row

```
import requests
from bs4 import Beautiful Soup
r = requests.get ("http://www.century21.com/real-estate
        rock-springs-wy/LCWYROCKSPRINGS/")
 c = r.content
  Soup = Beautiful Soup (c,"html.parser")
 print (Soup.prettify())
```

→ Extracting "div" Tags

```
all = soup.find-all "div", {"class": "propertyRow"})
all[0] . find-all("}"
all[0].find("h4", {"class": "propprice"}). text.replace
                         ("\n", "")
```

→ Extracting Addresses and property

```
for item in all
print (item.find("h4", {"class", propprice"}), text.replace ("\n", " ")
                 .replace ("  ", "")}
print (item. find-all ("span", {"class", "propaddresscollapse"}[0].tex
print (item, find-all ("span", {"class:) "propaddresscollapse"}[1]))
```

→ Extracting Elements without Unique Indentity

```
try:
  print (item.find ("span", {"class", in favalitHalfBath"})
                find ("b"). text )
Except:
  print (None)
for column group in item.find-all ("div", {"class":
                   "colounGroup"}):
for feature group, feature-name in zip (column-group
find-all ("div", {"class": feature Group"}). column.group
   [illegible] {"class": "featureName"})):
print (feature-group.text, feature name.text)
Print (" ")
```