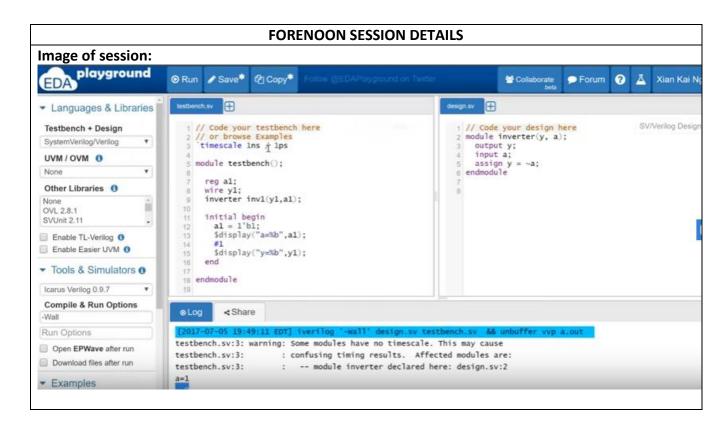
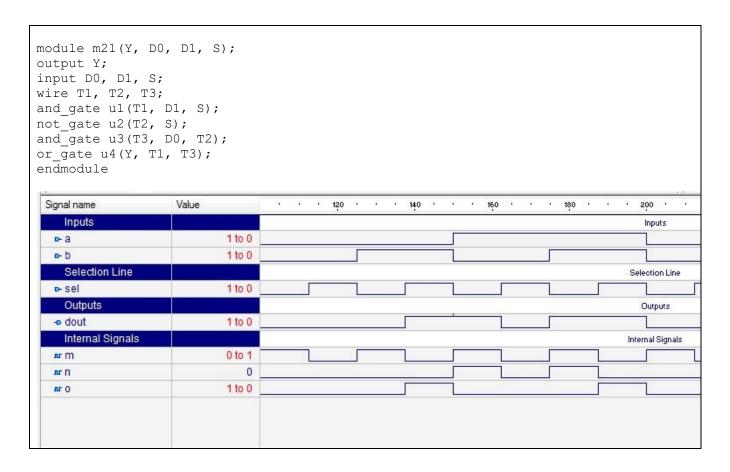
## **DAILY ASSESSMENT FORMAT**

Date:	03/06/2020	Name:	Nishanth
Course:	DIGITAL DESIGN USING HDL	USN:	4al17ec063
Topic:	<ol> <li>EDA Playground Tutorial Demo Video</li> <li>How to Download And Install Xilinx Vivado Design Suite</li> <li>Vivado Design Suite for implementation of HDL code</li> </ol>	Semester & Section:	6 <sup>th</sup> b-section
GitHub	nishanthvr		
Repository:			



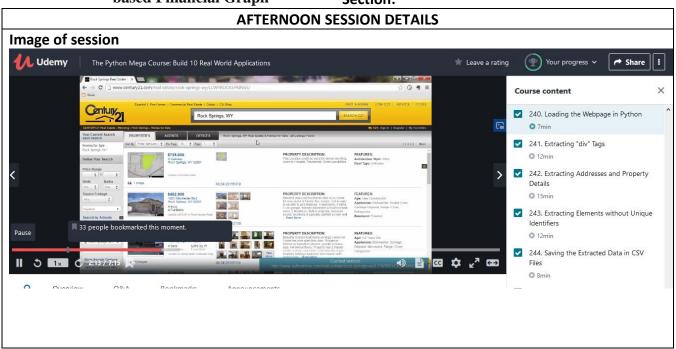
```
EDA playground
                    ⊙ Run / Save* ② Copy*
                                                                                     ▼ Languages & Libraries
                      1 // Code your testbench here
                                                             SV/Verlog Testbench
                                                                              // Code your design here
module inverter(a, y);
 Testbench + Design
                       // or browse Examples
'timescale ins/ips
 System/Verilog/Verilog
 UVM / OVM 0
 None
                        reg al;
wire yl;
inverter inv1(al, yl);
 Other Libraries 0
 OVL 2.8.1
                      initial begin
                       a1 = 1'b1;
5display("a=%b",a1);
end
 SVUnit 2.11
☐ Enable TL-Verilog 6
☐ Enable Easier UVM 0
▼ Tools & Simulators 6
                     17 endmodule
Icarus Verilog 0.9.7
                    Compile & Run Options
                    testbench.sv:3: warning: Some modules have no timescale. This may cause
                                   : confusing timing results. Affected modules are:
Open EPWave after run
                    testbench.sv:3:
☐ Download files after run
                    testbench.sv:3:
                                   : -- module inverter declared here: design.sv:2
                    Done
▼ Examples
 Verilog/System/Verilog
4:1 mux in structure modeling style:
module and gate (output a, input b, c, d);
assign a = b & c & d;
endmodule
module not gate(output f, input e);
assign e = \sim f;
endmodule
module or gate(output 1, input m, n, o, p);
assign l = m \mid n \mid o \mid p;
endmodule
module m41(out, a, b, c, d, s0, s1);
output out;
input a, b, c, d, s0, s1;
wire s0bar, s1bar, T1, T2, T3;
not_gate u1(s1bar, s1);
not gate u2(s0bar, s0);
and gate u3(T1, a, s0bar, s1bar);
and gate u4(T2, b, s0, s1bar);
and gate u5(T3, c, s0bar, s1);
and gate u6(T4, d, s0, s1);
or gate u7(out, T1, T2, T3, T4);
endmodule
code for 2:1 mux in structural style.
module and gate (output a, input b, c);
assign a = b \& c;
endmodule
module not_gate(output d, input e);
assign d = \sim e;
endmodule
module or gate(output 1, input m, n);
assign l = m \mid n;
endmodule
```



Date: 02/06/2020 Name: Nishanth
Course: Python USN: 4al17ec063

1. Application 8: Build a Web- Semester & 6<sup>th</sup> and b section

based Financial Graph Section:



**Application 7:** 

## Python program to extract details and plots and store csv files usinf pandas libray

A web-based application is any program accessed over a network that runs in a web browser and the browser supporting the programming language such as the combination of JavaScript, Hypertext Markup Language (HTML) and Cascading Style Sheets (CSS) are used for the creation of web-based applications. HTML is the communication standard used by the World Wide Web and a protocol that enables a web browser to retrieve text, graphics, sound and other information from a web server.CSS is a style sheet language used for describing the presentation(look) and formatting of a documents or web pages, including colors, layout, and fonts written in a markup language. Python programming language is used for web scraping. Web scraping is described as extracting and processing large amounts of data from the websites using programs or algorithms while using Python is a skill which can be used to extract the data into a useful form that can be imported and the main reason for preferring Python is Scrapy and Beautiful Soup, the most widely used and preferred frameworks; Python library is designed for fast and highly efficient data extraction.