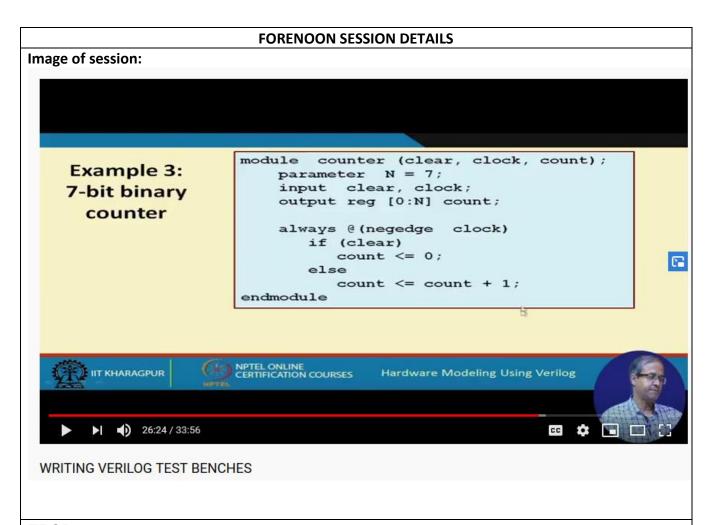
DAILY ASSESSMENT FORMAT

Date:	02/06/2020	Name:	Nishanth
Course:	DIGITAL DESIGN USING HDL	USN:	4al17ec063
Topic:	1.FPGA Basics: Architecture, Applications and Uses 2. Verilog HDL Basics by Intel 3. Verilog Testbench code to verify the design under test (DUT)	Semester & Section:	6 th b-section
GitHub Repository:	nishanthvr		



FPGA:

The <u>field-programmable gate array (FPGA)</u> is an integrated circuit that consists of internal hardware blocks with user-programmable interconnects to customize operation for a specific application. The interconnects can readily be reprogrammed, allowing an FPGA to accommodate changes to a design or even support a new application during the lifetime of the part.

FPGA Applications

Many applications rely on the parallel execution of identical operations; the ability to configure the FPGA's CLBs into hundreds or thousands of identical processing blocks has applications in image processing, artificial intelligence (AI), data center hardware accelerators, enterprise networking and automotive advanced driver assistance systems (ADAS).

```
Task:
module mux41(
  input i0,i1,i2,i3,sel0,sel1,
  output reg y);
  always @(*) //It includes all Inputs. You can use this instead of specifying all inputs in //sensivity
list. Verilog-2001 Feature
  begin
    case ({sel0,sel1})
    2'b00 : y = i0;
    2'b01 : y = i1;
    2'b10 : y = i2;
    2'b11 : y = i3;
    endcase
  end
endmodule
TestBench
module tb_mux41;
 reg I0,I1,I2,I3,SEL0,SEL1;
 wire Y;
 mux41 MUX (.i0(I0),.i1(I1),.i2(I2),.i3(I3),.sel0(SEL0),.sel1(SEL1),.y(Y));
 initial begin
    I0 = 1'b0;
    I1 = 1'b0;
    I2 = 1'b0;
    I3 = 1'b0;
    SEL0 = 1'b0;
    SEL1 = 1'b0;
    #45 $finish;
 end
 always #2 I0 = \sim I0;
 always #4 I1 =~I1;
 always #6 I2 =~I1:
 always #8 I3 =~I1;
 always #3 SEL0 = \simSEL0;
 always #3 SEL1 = \simSEL1;
```

always @(Y)

\$display("time =%0t INPUT VALUES: \t I0=%b I1 =%b I2 =%b I3 =%b SEL0 =%b SEL1 =%b \t output value Y =%b ",\$time,I0,I1,I2,I3,SEL0,SEL1,Y);

endmodule

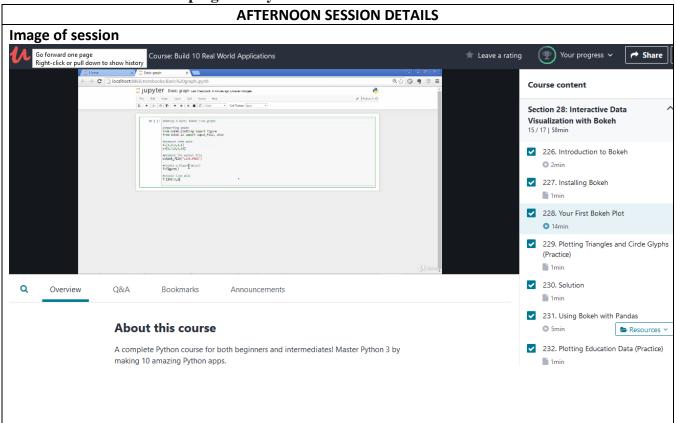
output

Date: 02/06/2020 Name: Nishanth
Course: Python USN: 4al17ec063

1.Interactive Data Visualization Semester & 6th and b section

with Bokeh Section:

2. Webscraping with Python



Plotting Triangles and Circle Glyphs (Practice)

code:

from bokeh.plotting import figure

```
from bokeh.io import output_file, show
import pandas

#prepare some data
df=pandas.read_csv("http://pythonhow.com/data/bachelors.csv")
x=df["Year"]
y=df["Engineering"]

#prepare the output file
output_file("Line_from_bachelors.html")

#create a figure object
f=figure()

#create line plot
f.line(x,y)
```

• #write the plot in the figure object

• show(f)