Morning session

Date - 28 may
Course - logic design
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Sem - IV sem

- Report

analysis of clocked sequential circuits (with D flip flop)

step 1 - find out the i/p & o/p eqn

$D_A = x Q_A + Q_B$

$D_B = \bar{Q}_A Q_B$

$y = x \bar{Q}_B + x Q_A$

$D(Q_{n+1}) = Q_A^+ = D_A$

$Q_B^+ = D_B$

step 2 - state table

P.S			N.S		
Q_A	Q_B	x	Q_A^+	Q_B^+	y
0	0	0	0	0	1
0	0	1	0	0	0

$Q_A^+ = D_A = x Q_A + Q_B$

$= 0.0 + 0 = 0$

$Q_B^+ = D_B = \bar{Q}_A Q_B$

$= 1.0 = 0$

$y = 1.1 + 0.0 = 1$

step 3 state diagram

- learning sequential logic diagram for a digital clock - 14

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