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Sem:- 6th B.

Course:- digital design using HDL.

Topic:- Hardware Modelling using Verilog & fpga Asic.

* Hardware Modelling using verilog it uses various Digital Circuit Modelling issues using Verilog, writing test benches and some case studies
* Here the paper provides an overview of some of the key Elements of FPGA for Engineers Interested in utilizing FPGA-based Technologies.
* This paper still give u a lot of help Information if you are New to the world of FPGA.
* Here We are not distinguishing the FPGA. We are using code to tell the chip how to configure Itself.
* lot of planning bugs happens more then we Excepted. If we are newbie developers.
* Application-specific Realities you to concern with Revolving around cyber security and safety.
* For Example, some have A/D Converters & PLL's.
* ASIC is the case of it, you're designing a digital logic Circuit, as in AND, OR etc:
* There are 4 Algorithmic/processing Attributes Defined below that FPGA's are generally well-suited for.
* High data-to-clock Rate Ratio, if we calculate the need to be Executed over & over continously.
* The Amount of Determinism that you can achieve with an FPGA will usually far surpass that of a Typical Sequential Processor.
* If there are too many operations to executed, we may Not have Enough time to close the loop to update all the I/O within the allotted time.
* It is more Advanced components Hard cores - These are functional blocks that have there own dedicated logical Resources).

Python Repost.

* The Aims to Inspect the stableness of Intersective Affinity b/w search interest of pBics of the stock and Evidence stock market out comes on world wide Equality market Indices.

* This study Represents and develop fasmes Explosn into financial graph by Registering the attributes and magnitudes of graph use and Embankment from Representational Impartially.

* Paradox could also called derived through Inves - tors behaviours and degree of disclosure Inclusion.

* Downloading Data sets with python.

```
from pandas - data 3readers import data
import data time
start = data time . datatime (2016, 3, 1)
end = datatime . datatime (2016, 3, 1)
data. Data Reader (name = "AAPL". data. 3rader
                   "yahoo", stust. end. end).
```

* @ app. 3route (/.)
  def home ():

    3ctusn 3readers_ template ("home. html")

@ app. 3router (/. about /")
def about ();
if - name - = = "= - main - ":
app. 3un (debug = time).
