* FPGA:- The fasst fpga project help students to understand the Basis of FPGA's and has verilog / VHDL works on FPGA

* D-flipflop code:-

```
module d-ff (clk, d, q, q-bar)
input d, clk;
output q, q-bar;
wire d, clk;
reg q, q-bar;
always @ (posedge(clk)
begin
q <= d;
q-bar <= !d;
end
endmodule.
```

* Bottom up design :- Each designed is performed at the gate level using the standerd gates with increasing complexity of new Designs this Appsoach is Newly Impossible to Maintain.

* Top-down Design :- A Real Top down design Allows Easly Testing easy of diffrent Technologies a structured s/m design and offer many other Advantages.

* Abstraction levels of Verilog:-

* Behavioral level
* Register-transfer level.
* Gate-level.

* Data types

There are two primary data types:-

* Nets &
* Registers

Python Repost

* Flask startup and configuration like most widely used Python libraries, the flask package is Installable from the Python package Index (PPI).
* First we should create a directory to work in i.e., (flask - todo) is then Install the flask package
* We have Install flask-sqlalchemy so our flask Application has a simple Way to talk to a Sql database.
* We should create setup.py which should look like this

```
Requires = [
        'flask'
        'flask-sqlalchemy',
        'psycopg2',
        ]
setup(
        name = 'flask-todo'
        version = '0.0'
        description = 'A To-Do List Built with Flask'
        author = <'you actual name here'>
        keywords = 'web flask'
        packages = find_packages
        Includes = packages - data = True
        Install_Requires = Requires.
        )
```

This is the way whenever we want to Install / deploy our project,,