

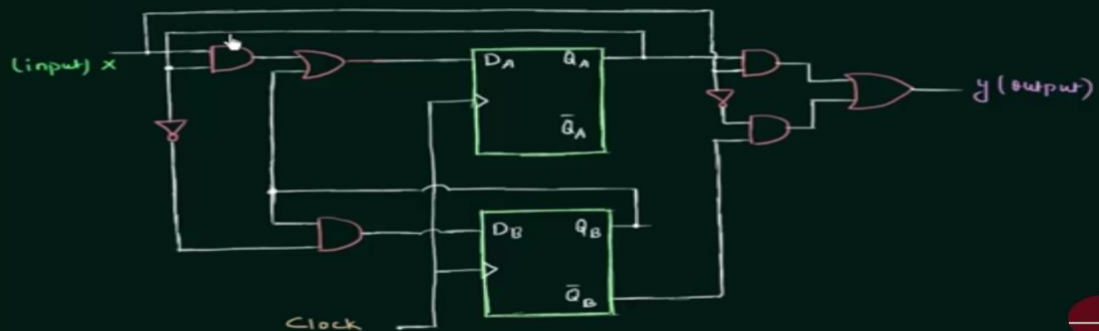
DAILY ASSESSMENT FORMAT

Date:	29-05-2020	Name:	Sahana S R
Course:	Logic design	USN:	4a117ec083
Topic:	<ul style="list-style-type: none"> • Analysis of clocked sequential circuits • Digital clock design 	Semester & Section:	6 th sem B sec
Github Repository:	sahanasr-course		

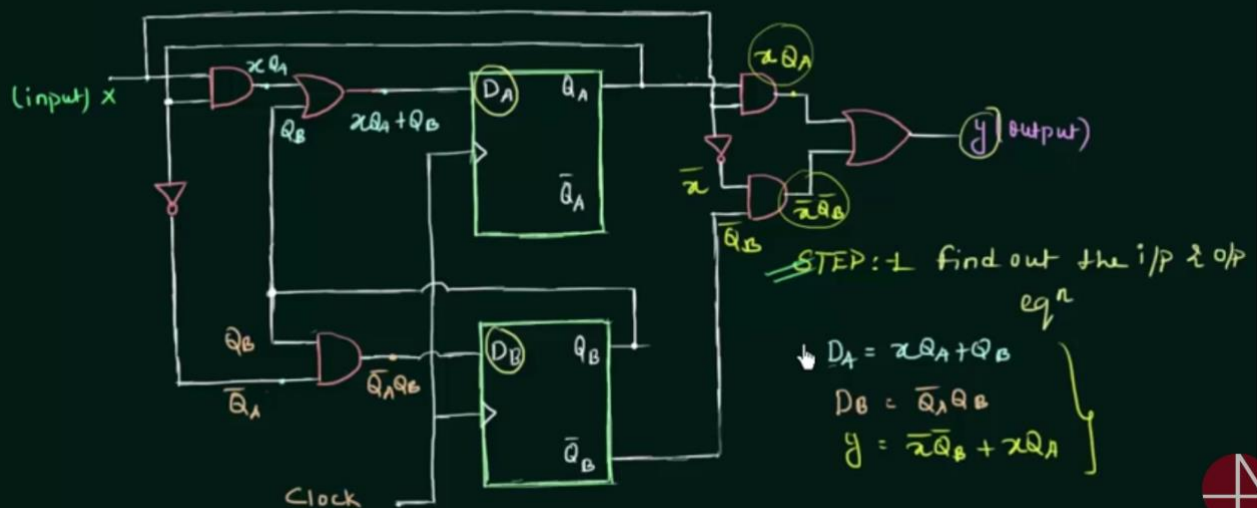
FORENOON SESSION DETAILS

Image of session

Analysis of Clocked Sequential Circuits (with D Flip Flop)



Analysis of Clocked Sequential Circuits (with D Flip Flop)



Q_A \bar{Q}_B
 Clock

$D_B = Q_A Q_B$
 $y = \bar{x} \bar{Q}_B + x Q_A$

$D = Q_{n+1}$
 $Q_A^+ = D_A$
 $Q_B^+ = D_B$

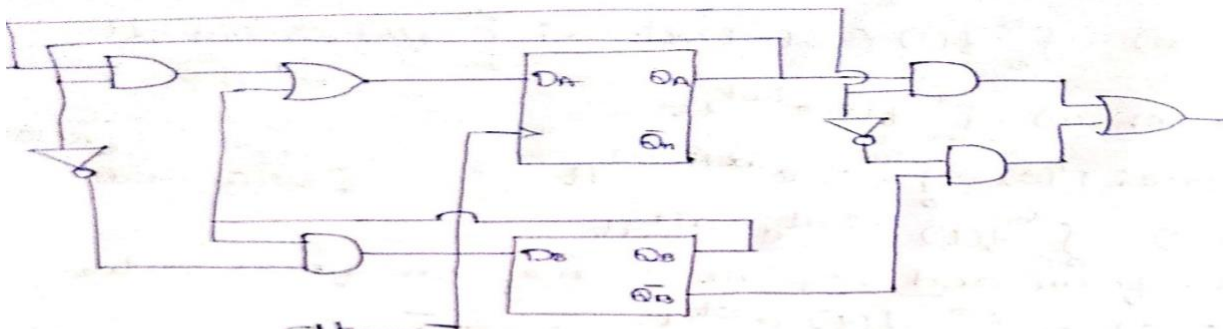
STEP: 2 State table

P.S.		x	N.S.		y
Q_A	Q_B		Q_A^+	Q_B^+	
0	0	0	0	0	1
0	0	1	0	0	0

$Q_A^+ = D_A = x Q_A + Q_B$
 $= 0 \cdot 0 + 0 = 0$
 $Q_B^+ = D_B = \bar{A}_1 Q_B$
 $= 1 \cdot 0 = 0$
 $y = 1 \cdot 1 + 0 \cdot 0 = 1$
 $y = 0 \cdot 1 + 1 \cdot 0 = 0$

Report – Report can be typed or hand written for up to two pages.

Analysis of Clocked Sequential Circuit

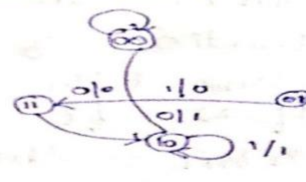


$D_A = 1Q_A + 0Q_B$
 $D_B = 0Q_A + 0Q_B$

State table

Q_A	Q_B	x	Q_A^+	Q_B^+	y
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	0	1

State diagram



Digital clock design

A digital clock is a type of clock that displays the time digitally as opposed to an analogue clock where the time is indicated by the positions of rotating hands.

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

- Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock
- The input that sets the **flip-flop to 1** is **called preset or direct set**. The input that clears the flip-flop to 0 is called **clear or direct reset**.
- When power is turned on in a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.

- The knowledge of the type of flip-flops and a list of the Boolean expressions of the combinational circuit provide the information needed to draw the logic diagram of the sequential circuit. The part of the combinational circuit that generates external outputs is described algebraically by a set of Boolean functions called **output equations**. The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean functions called flip-flop input equations (**or excitation equations**).
- The information available in a state table can be represented graphically in the form of a **state diagram**. In this type of diagram a state is represented by a circle and the (clock-triggered) transitions between states are indicated by directed lines connecting the circles.
- The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (transition table). The table has four parts present state, next state, inputs and outputs.

