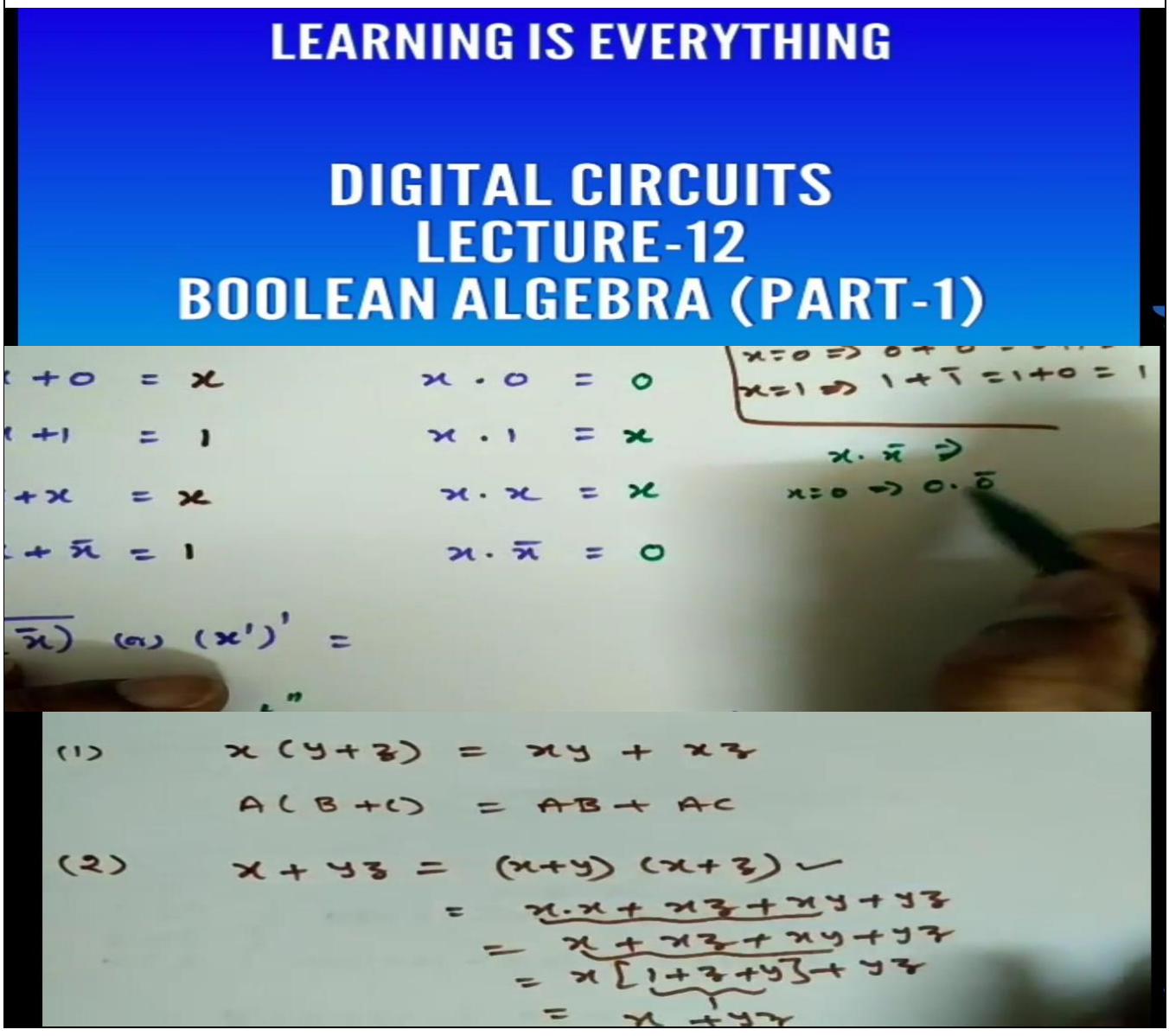
DAILY ASSESSMENT FORMAT

Date:	**28-05-2020**	**Name:**	**Sahana S R**
Course:	**Logic design**	**USN:**	**4al17ec083**
Topic:	**•Boolean equation for digital circuits. Combinational circuits Conversions of MUX and decoder to logic gate •Design of 7segment decoder with common anode display**	**Semester & Section:**	**6th sem B sec**
Github Repository:	**sahanasr-course**		

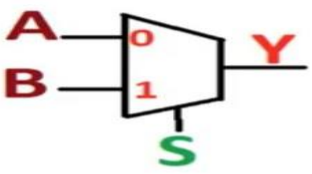
FORENOON SESSION DETAILS
Image of session



MUX TO LOGIC GATES

1. NAND, NOR -Universal gates
2. "Universal Logic"
3. **MUX** and Decoders are called "Universal Logic"

4.now we will see haw a 2:1 MUX can be used to create different logic gates.



SELECTION (S)	OUTPUT(Y)
0	A
1	B

$Y = A\bar{S} + BS$

$2^n - 1$

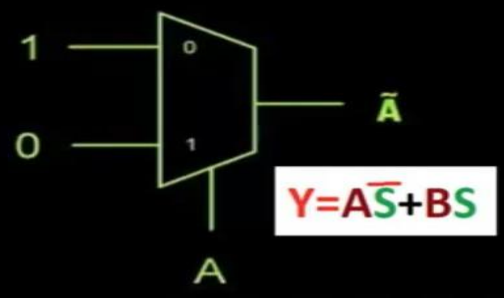
2^n =inputs

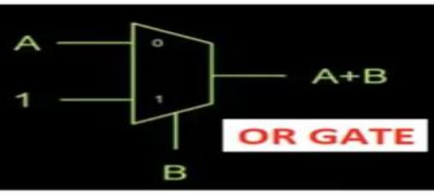
n =selection lines

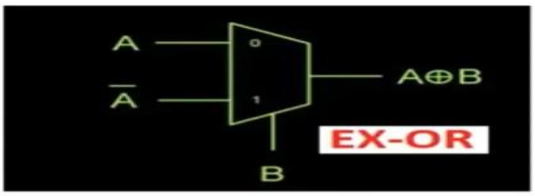
INVERTER DESIGN

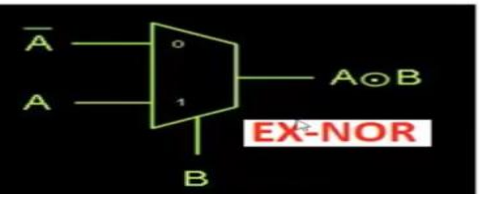
$Y = 1.\vec{A} + 0.A$

$Y = \vec{A}$

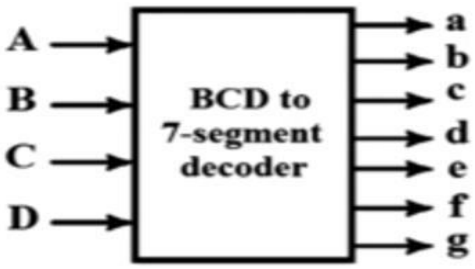






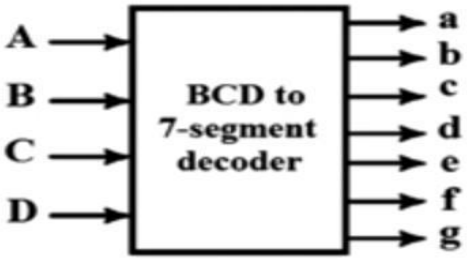


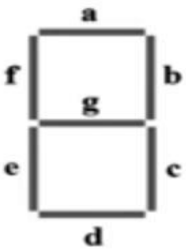
BCD to 7-segment decoder



A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

BCD to 7-segment decoder





A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Report – Report can be typed or hand written for up to two pages.

Boolean equations for digital circuits

-> In 1854, George Boole developed an algebraic system now called boolean algebra

and operation	Or operation	Not operation
$0 \cdot 0 = 0$	$0 + 0 = 0$	
$0 \cdot 1 = 0$	$0 + 1 = 1$	
$1 \cdot 0 = 0$	$1 + 0 = 1$	
$1 \cdot 1 = 1$	$1 + 1 = 1$	

In boolean algebra

$A + A = A$ & $A \cdot A = A$

$1 + 1 = 1$ & $1 \cdot 1 = 1$

In ordinary algebra

$A + A = 2A$ $\quad A \cdot A = A^2$

$1 + 1 = 2$ $\quad 1 \cdot 1 = 1$

In binary number system

$1 + 1 = (10)$ $\quad 1 \cdot 1 = 1$

$x + 0 = x$ $\quad x \cdot 0 = 0$

$x + 1 = 1$ $\quad x \cdot 1 = x$

$x + x = x$ $\quad x \cdot 2 =$

$x + \overline{x} = 1$

-> $(\overline{x})$ $\quad (x')' = x$

Identity element :- OR operation AND operation

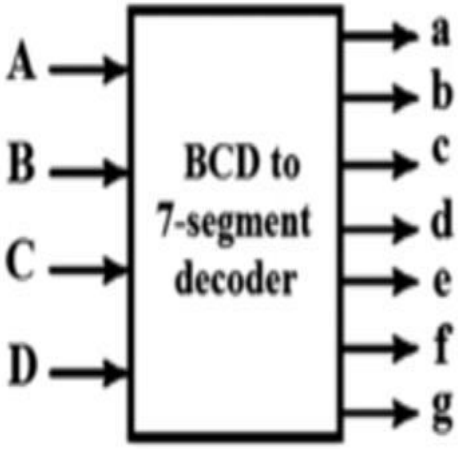
The additive identity = 0

The multiplicative identity = 1

Mux to Logic gate

1. NAND, NOR - Universal gates
2. MUX and Decoder are called "Universal logic"
4. Now we will see how 2:1 MUX can be used to create different logic gate.

BCD to 7-segment decoder



A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1