

## DAILY ASSESSMENT FORMAT

Date:	04-06-2020	Name:	Sahana S R
Course:	Digital design using HDL	USN:	4a117ec083
Topic:	• Hardware Modeling Using Verilog •FPGA and AISC Interview Questions	Semester & Section:	6 <sup>th</sup> sem B sec
Github Repository:	sahanasr-coures		

### FORENOON SESSION DETAILS

Image of session



## Main Objectives of the Course

### Hardware Modeling Using Verilog

1. Learn about the Verilog hardware description language.
2. Understand the difference between behavioral and structural design styles.
3. Learn to write test benches and analyze simulation results.
4. Learn to model combinational and sequential circuits.
5. Distinguish between good and bad coding practices.
6. Case studies with some complex designs.



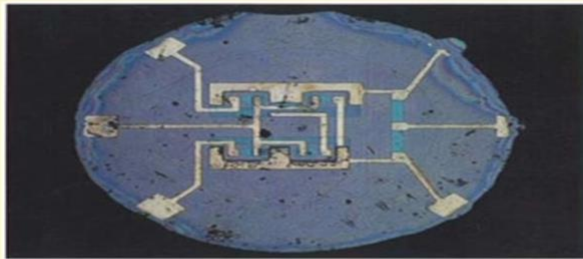
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Hardware Modeling Using Verilog





First Planar IC (1961) and Intel Nehalem Quad Core Die



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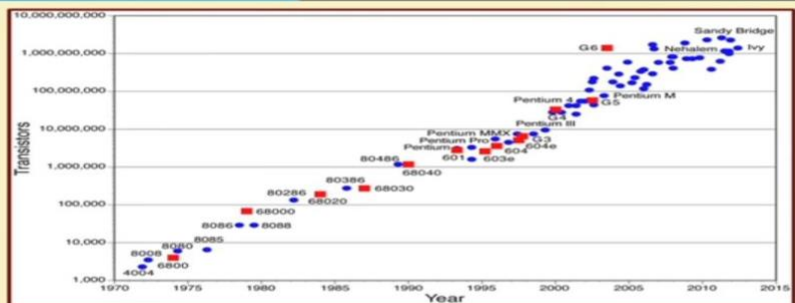
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## Moore's Law

- Exponential growth
- Design complexity increases rapidly
- Automated tools are essential
- Must follow well-defined design flow



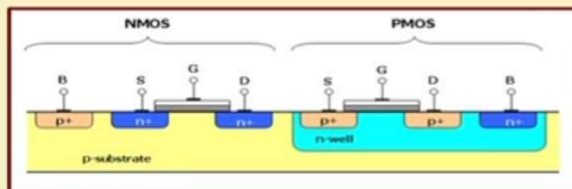
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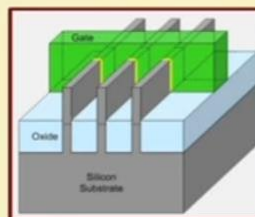
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Hardware Modeling Using Verilog

5



CMOS  
(up to 22nm)



FinFET  
(14nm)



QUANTUM?



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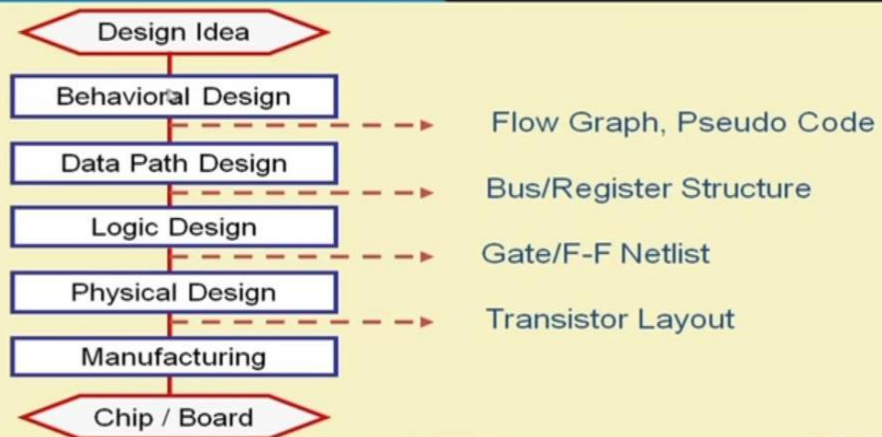


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## Simplistic View of Design Flow



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## Other Steps in the Design Flow

- Simulation for verification
  - At various levels: logic level, switch level, circuit level
- Formal verification
  - Used to verify the designs through formal techniques
- Testability analysis and Test pattern generation
  - Required for testing the manufactured devices



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Report – Report can be typed or hand written for up to two pages.

## Introduction

### Hardware Modeling Using Verilog

#### VLSI Design Process

- Design Complexity increasing rapidly
- The present trend

#### → Moore's Law

- Exponential growth
- Design Complexity ↑ rapidly
- Automated tools are essential
- Must follow well-defining flow.

#### → VLSI Design flow

- Standardized design procedure
- Encompasses many steps.
  - Specification – Synthesis – Simulation – layout
- Need to use Computer Aided Design (CAD) tools

#### → Two Competing HDLs

Verilog VHDL

#### → Simplistic view of design flow

#### → Steps in the Design flow

- Behavioral design
- Data path design
- Logic design
- Physical design and Manufacturing

#### → other steps in the design flow

- Simulation for Verification
- Testability analysis and Formal Verification
- Test pattern generation

#### 2. FPGA and ASIC Interview question.

#### 3. T-Flipflop

module tff (input clk, input rst, input t, output reg q)  
always @ (posedge clock)

begin  
if (rstn)  
q <= 0;

else  
if (t)

q <= ~q

else  
q <= q;

end  
endmodule

