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| **Date:** | **28 MAY 2020** | **Name:** | **Sampatkumar n m** |
| **Course:** | **logic design** | **USN:** | **4AL19EC401** |
| **Topic:** | **Day 2:analysis of clocked sequential circuits**  **digital clock design** | **Semester & Section:** | **4TH SEM**  **& A SEC** |
| **Github Repository:** | **Sampatkumar1** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS:-**   * Now that we have flip-flops and the concept of memory in our circuit, we might want   to determine what a circuit is doing.   * The behavior of a clocked sequential circuit is determined from its inputs, outputs   and state of the flip-flops (i.e., the output of the flip-flops).   * The analysis of a clocked sequential circuit consists of obtaining a table of a diagram   of the time sequences of inputs, outputs and states.   * We have a basic procedure for analyzing a clocked sequential circuit: * Write down the equations for the outputs and the flip-flop inputs. * Using these equations, derive a state table which describes the next state. * Obtain a state diagram from the state table. * It is the state table and/or state diagram that specifies the behavior of the circuit. |

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