**DAILY ASSESSMENT FORMAT**

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| **Date:** | **4 june 2020** | **Name:** | **Sanketh S Acharya** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC084** |
| **Topic:** | **1. Hardware modelling using verilog**  **2. FPGA and ASIC Interview questions** | **Semester & Section:** | **6TH SEM & ‘B’ SEC** |
| **Github Repository:** |  |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session**  **C:\Users\cw\Desktop\4 j1.png** |
| **Report –**   * **Hardware modeling using verilog:** * **Learn about the verilog hardware description language** * **Learn to write test benches and analyze simulation result** * **Learn to model combinational and sequential circuits** * **Distinguish between good and bad coding practices** * **Case studies with some complex designs**   **VLSI design process:**   * **Design complexity increasing rapidly** * **Increased size and complexity** * **Fabrication technology improving** * **CAD tools are essential** * **Conflicting requirements like area, speed ,and energy consumption** * **The present trend** * **Standardize the design flow** * **Emphasis on low-power-design , and increased performance**   **VLSI design flow:**   * **Standardized design procedure** * **Starting from the design idea down to the actual implementation** * **Encompasses many steps:** * **Specification** * **Synthesis** * **Simulation** * **Layout** * **Testability analysis** * **Data path design:** * **Generate a netlist of register transfer level components , like registers , adders , mulitiplexers , decoders , etc.** * **A netlist is a directed graph , where the vertices indicate components , and the edges indicate interconnections.** * **A netlist specification is also refered to as structural design.** * **Logic design** * **Generate a netlist of gates/flip-flops or standard cells.** * **A standard cell is a pre-designed circuit module at the layout level.** * **Various logic optimization techniques are used to obain a cost effective design .** * **There may be conflicting requirements during optimization:** * **Minimize number of gates** * **Minimize number of gate levels** * **Minimize signal transformation activities** * **Physical design and manufacturing** * **Generate the final layout that can be sent for fabrication.** * **The layout contains a large number of regular geometric shapes corresponding to the different fabrication layers.**     **Other steps in the design flow:**   * **Simulation for verification** * **At various levels: logic level, switch level ,circuit level** * **Formal verification** * **Used to verify the designs through formal techniques** * **Testability analysis and test pattern generation** * **Required for testing the manufactured devices** |

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| **Topic:** |  | **Semester & Section:6TH SEM&’B’ SEC** |  |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session**  **C:\Users\cw\Desktop\289.png** | | | |
| **Report –** | | | |