Course :- Hardware Description languages for FPGA Design:

Date :- 07-Sep-2020 Sindhu. S

- Introduction to the course:-
  - → Introduction to the hardware FPGA Design.
- Why learn VHDL?
  - → VHDL is a widely used design language.
  - → VHDL is a structured language for logic design
- FPGA Design Flow:-
  - → A Describing a hardware circuit implementation that your tool chain will eventually interpret and synthesize into FPGA logic cells.
  - → Explore FPGA design entry options
- Introduction to VHDL:- state Machine
  - → establish motivation for learning VHDL
  - → - Reinforce Key Concepts

→ Introduction to VHDL coding.

- FPGA Design for Embedded systems.
  → History and definition of VHDL
- VHDL Assignments: signals and variables
  → operators: add, Multiply and every body shift to the left. (Dial 0)
- VHDL Rules and Syntax:
  → Create readable code style by using spaces, tabs.
  - other readble code sources as ex
  → Library, Entity, Architectures.
- VHDL in Modelsim: Code and instal
  - How to download an HDL Simulator Modelsim from Mentor graphics
  - How to install Modelsim on your P
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