Course :- Hardware Description languages for FPGA Design.

APJ-18EC049
5th Sem
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e.R :- Sindhu_Course.

- The parts of a VHDL file are.
  - Libary
  - Entity
  - Architecture.
- Submitting VHDL programming Assignments
  - write VHDL code
  - → Download from coursera
  - → place files in Modelsim project directory.
  - → Run testbench Simulation in Modelsim
  - → upload the myvectorb.out file and your .vhd file to coursera
- VHDL 2-bit Comparator
- VHDL correct Errors

- VHDL Majority Vote:-

Mission 2-002:-

Using VHDL, design a Majority Vote Circuit, which outputs a logical 1 only if 2 @ more of 3 inputs are a 1. Using the entity below also given in AAC2M1P4.vhd, create the architecture

- VHDL 1-bit full adder:-

```
library ieee;
use ieee.std_logic_1164.all;
entity Full Add is port (A, B,
    Cin: in std_logic; Sum,
Cout: out std_logic);
end full Add;
```