**DAILY ASSESSMENT FORMAT**

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| **Date:** | **5/06/2020** | **Name:** | **Pv sai suraksha** |
| **Course:** | **Digital Design Using HDL** | **USN:** | **4AL17EC064** |
| **Topic:** | **1.Verilog Tutorials and Practice Programs**  **2.Building/Demo Projects using FPGA.** | **Semester & Section:** | **6th sem**  **B section** |
| **GitHub Repository** | **surakshacourses** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **Verilog Tutorials and Practice Programs**  **\* Verilog is a Hardware Description Language; a textual format for describing electronic circuits and systems. Applied to electronic design, Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis (testability analysis and fault grading) and for logic synthesis.**  **\* Verilog is a hardware description language or HDL. It is used to model electronic circuits and systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction.**  **Building/Demo Projects using FPGA.**  \* Build and Run a Sample Project Using the Command Line |

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| **Date:** | **5/06/2020** | **Name:** | **Pv sai suraksha** |
| **Course:** | **Python** | **USN:** | **4AL17EC064** |
| **Topic:** | **1.Advanced Dictionaries.**  **2.Advanced Lists.** | **Semester & Section:** | **6th sem**  **B section** |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |