Date:- 3rd june 2020 Name:- Poojary sushant

Course:- Digital Design using HDL USN:- 4AL18EC400

Topic:- EDA Playground online compiler, EDA Playground Tutorial Demo Video, How to Download & Sem:- 6th sem. 'B'

Report - EDA Playground Tutorial Demo

Implement Inverter using The EDA Tool

```
module inverter (y,a);
 output y;
 input a;
  assign y=~a;
endmodule
```

Test bench code

```
timescale ns/ps
module testbench();
 reg a1;
 wire y1;
 inverter inv1(a1,y1);
 initial begin
     a1 = 1'b1;
     $display ("a = %b", a1);
end
endmodule
```

Ripple carry counter

```
module ripple_counter_4 bit (q, clk, reset);
input clk, reset;
output [3:0] q;
T_FF tff0 (q[0], clk, reset);
T_FF tff0 (q[1], q[0], reset);
```

```
T_FF tff2 (q[2], q[1], reset);
T_FF tff3 (q[3], q[2], reset);
endmodule
module T_FF (q, clk, reset);
input clk, reset;
output q;
wire d;
D_FF dff0(q, d, clk, reset);
not n1 (d, q);
endmodule
module D_FF (q, d, clk, reset);
input d, clk, reset;
output reg q;
always @( negedge clk or posedge reset)
begin
if (reset)
q <= 1'b0;
else
q <= d;
end
endmodule
```

Test bench

```
module test
reg clk, reset;
wire [3:0] q;
ripple carry_counter rcc(q, clk, reset);
initial begin
$dumpfile ("dump.vcd");
$dumpvars (1, test);
clk = 1'b0;
reset = 1'b1;
#10 reset = 1'b0;
#200 $finish;
end
always #5 clk = ~clk;
endmodule
```

Task Day3

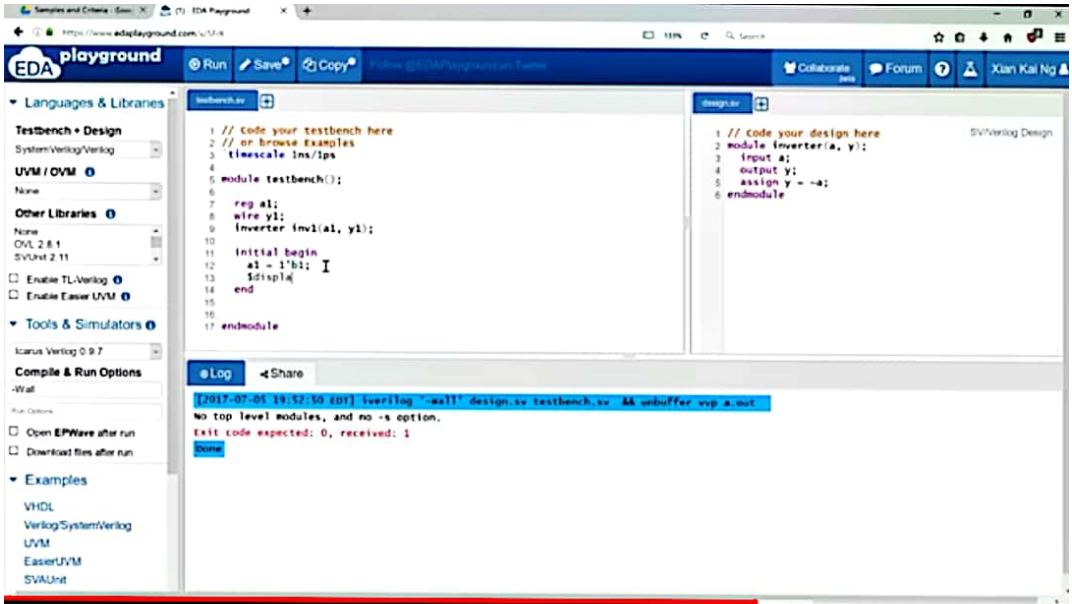
Implement 4to1 Mux using two 2:1 mux using structural modeling style & test the module in online/offline compiler

Code:

```
library IEEE;
use IEEE.STD_logic_1164.AL;
entity mux2_1 is
Port (A,B: in STD_LOGIC;
 S : in STD-LOGIC;
 Z: out STD-LOGIC);
end mux2_1;

architecture Behstructuralmodeling of mux2_1 is
begin
Process (A,B,S) is
begin
if (S='0') then
Z <= A;
else
Z <= B;
end if
end Process;
end Behavioural;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux4_1 is
Port (
A,B,C,D: in STD_logIC;
SOS1 : in STD_LOGIC;
Z: out STD-LOGIC;
```

```
);
end mux4-1;
architecture Structural of mux4-1 is
component mux2-1
Port(A,B : in STD-LOGIC;
S: in STD-LOGIC;
Z: out STD-LOGIC;
end component;
signal temp1, temp2 : std-logic;
begin
m1 : mux2-1port map(A,B,S0,temp1);
m2: mux2-1port map(C,D,S0 temp2);
m3: mux2-1port map(temp1,temp2,S1,Z);
end Structural;
```



Verilog on EDA Playground Starting Tutorial

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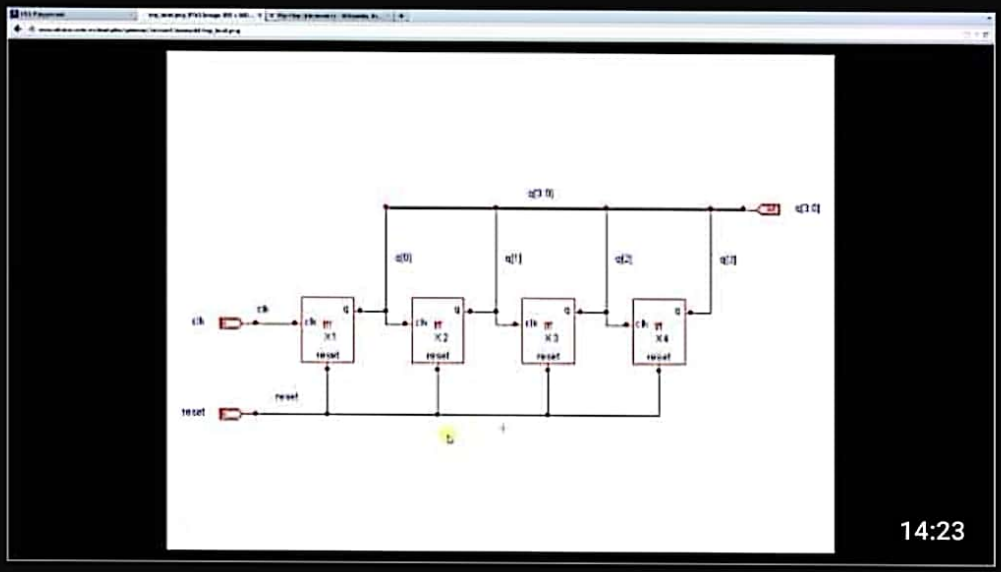

Verilog Tutorial 1 -- Ripple Carry Counter

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Date: 3 June 2020 Name: Poojary sushant

Course: Python USN: 4AL18EC400

Topic:- Build a web-based Financial graph Sem: 6th sem 'B' sec

```
from flask import Flask, render_template
app=Flask (__name__)
@app.route('/plot/')
def plot ():
    from pandas_datareader import data
    import datetime
    import fix_yahoo_finance as yf
    yf.pdr_override ()
    from bokeh.plotting import figure, show, output_file
    from bokeh.embed import components
    from bokeh.resources import CDN
    start = datetime.datetime(2015,11,1)
    end = datetime.datetime(2016,3,10)
    df = data.get_data_yahoo(tickers="GOOD",start=start,end=end)
    def inc_dec(c,o):
        if c>o:
            value = "Increase"
        elif c<o:
            value = "Decrease"
        else:
            value = "Equal"
        return value
df["status"] =[inc_dec(c,o) for c,o in zip(df.close,df.open)]
df["Middle"]=(df.open+df.close)/2
df["Height"]=abs(df.close-df.open)
```

```
p.rect(df.index[df.status=="Increase"], df.Middle[df.status=="Increase"],
df.Height[df.status=="Increase"], fill_color="#CCFFFF", line_color="black")
p.rect(df.index[df.status=="Decrease"], df.Middle[df.status=="Decrease"],
df.Height[df.status=="Decrease"], fill_color="#FF3333", line_color="black")
    script, div = components(p)
    cdn_js = CDN.js_files[0]
    cdn_css = CDN.css_files[0]
    return render_template("plot.html",
    script1=script1,
    div=div1
    cdn_css=cdn_css,
    cdn_js=cdn_js)
@app.route('/')
def home():
    return render_template("home.html")
@app.route('/about')
def about():
    return render_template("about.html")
if __name__=="__main__":
    app.run(debug=True)
```

Lite www.udemy.com/course/the-python-r 3

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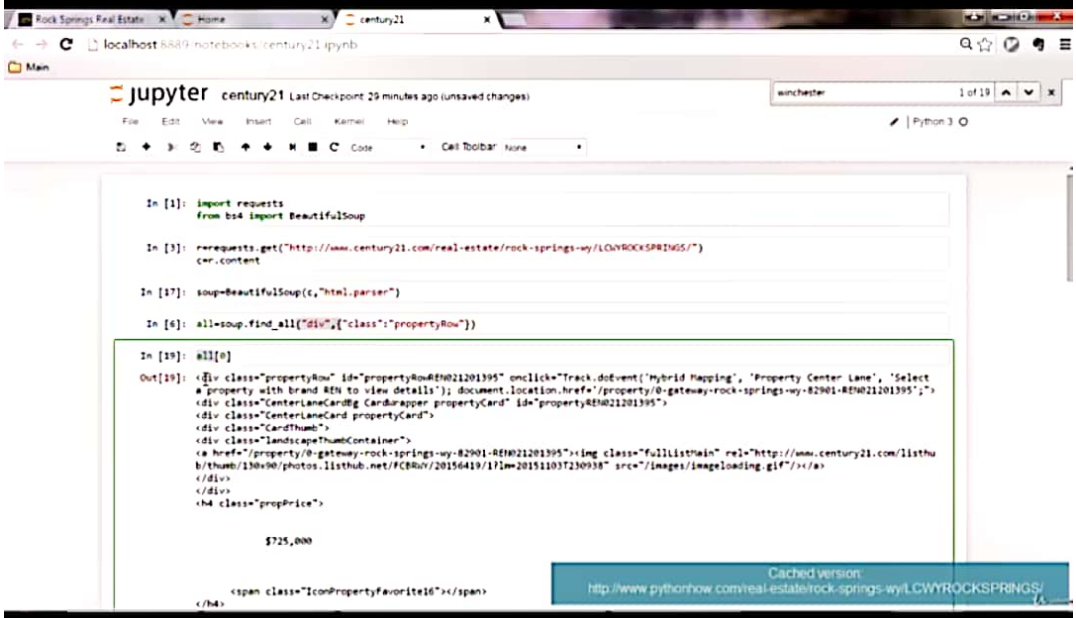

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