Date: 4 june 2000 Name: Poojary sushant

course! Digitel Design using HOL USN: 4AL18 EC400

Topic: Hardware Modeling using sem 6th B' sec

Report - Hardware Modeling using verilog Objective of Hardware Modeling using verilog

> Learn about the Muerilog hardware description language.

> understand the difference between behaviourd be structured design styles

> learn to write test benches & analysis simulation result

> learn to model combinational & sequential circuit.

-> Distinguish win good & bad coding practices

>> case studies with some complex designs

VLSI Design process

- Design complexity increasing rapidly

· Increwed Size & complexity

· Fobrication technology improving

-> The Present trend

· standardize the design flow

" Emphasis on low-power design, Lincreard performance

-> Exponential growth

>> Design complexity increases rapidly

-> Automated took are evential

> Mist hollow well defined design flow

stondardized design procedure

> Starting from the design idea down to the actual implementation. Need to use computer Aided Design

-> Hardware Description Longuage

-> Based on HDL provided

A CAD too, from form its HDL in put into a HDL ofp that contains more detailed information about the hardware

Tour competing HDLS

-> Venlog

-> VHOL

Behavioral design

-> specify the functionality of the design in term of its behavior

Dota path design

- -> henerate a nethist of register transfer level components, like register address adden Multiplier , Multiplexes decoder etc.
- -> A pretist is a directed graph, where the verties indicate components the edger indicate interconnections

Logic design

- -> Generate a nettist agoste (flip-flop or stondard cells
 - > A standard cell is a pre-designed clet module-
 - 2) Various logic optimization techniques are used to obtain a cost effective design

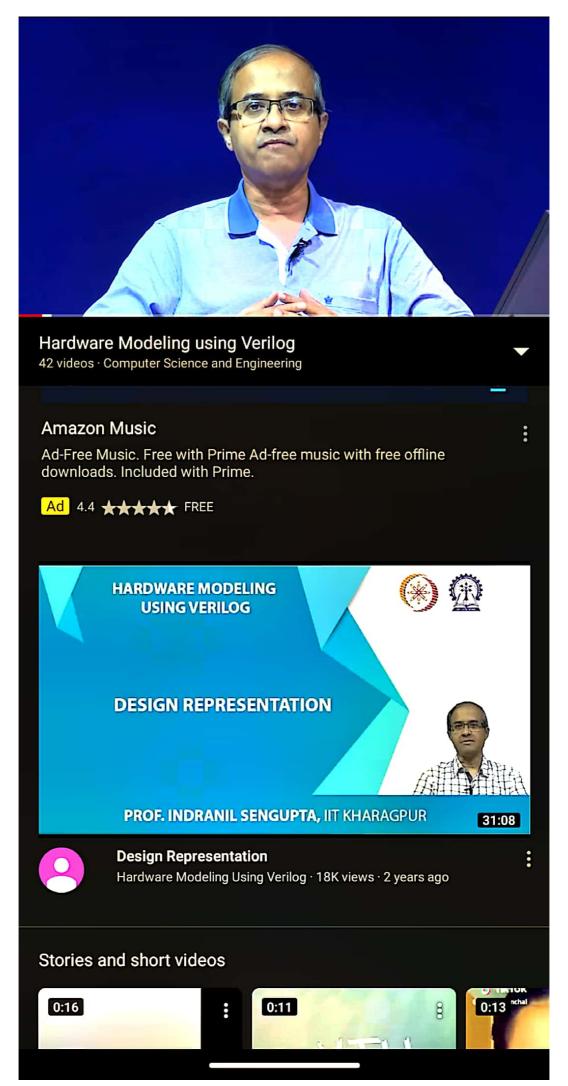
There may be conflicting requirements during optimization

- 5 Minimize the no of getter
- -> minimize no of get ferel
- -> minimize signed transition activities

Physical design & Manufacturing

- Generate the final layout that combe sent for tobrication
- The layout contains a large number of regular geometric shopes corresponding to the different fabrication layous
- -> Alternatively 1the final target may be Field Programmable Gade Array (FPGA), where technology mapping from the get level nedtist is used

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