# DAILY ASSESSMENT REPORT

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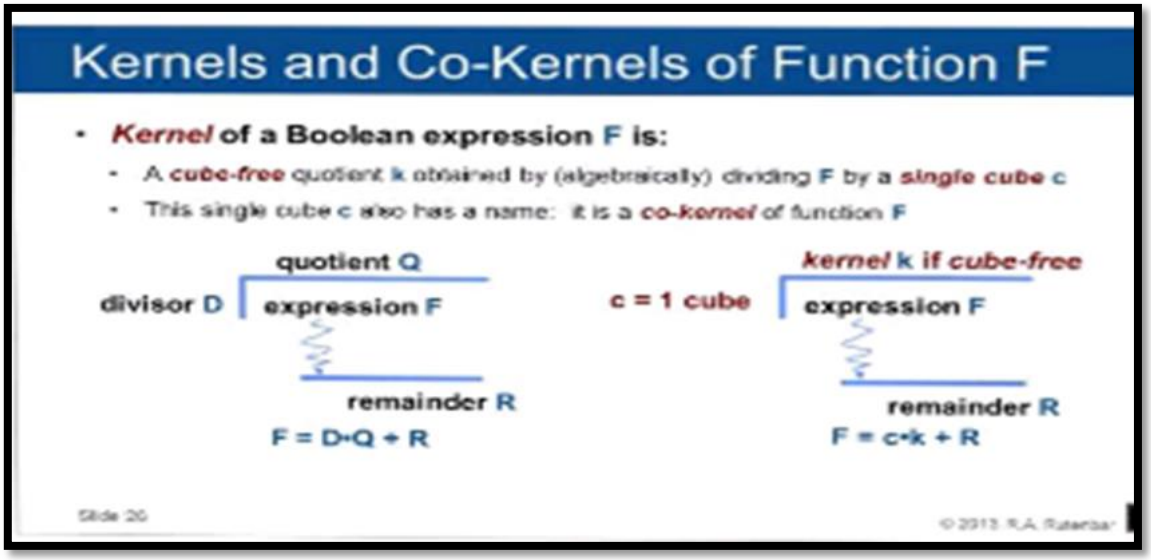
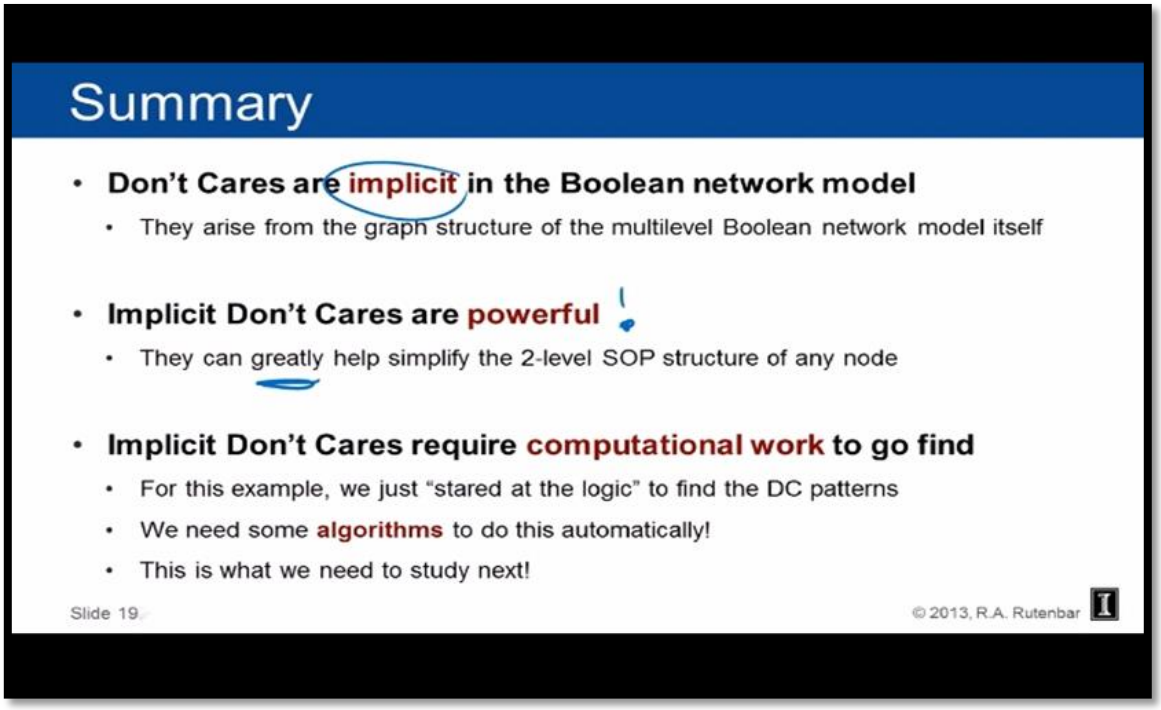
| **Date:** | **06-August-2020** | **Name:** | **Swastik R Gowda** |
| **Course:** | **VLSI CAD PART 1** | **USN:** | **4AL17EC091** |
| **Topic:** | **Week 4** | **Semester & Section:** | **6th Sem 'B' Sec** |
| **Github Repository:** | **swastik-gowda** | | |

**FORENOON SESSION DETAILS**

**Image of session**



**Report – Report can be typed or hand written for up to two pages.**

As we noted in the lectures, all of multi-level logic optimization is based on scripts that heuristically optimize a Boolean network model of your design. Thus, SIS has many commands and many options. For simplicity, we are using a standard, default synthesis script called the RUGGED script to optimize your designs.

SIS can also read logic design in many different file formats. But conveniently for us, it can read the same format that the ESPRESSO 2-level optimizer tool uses, the so-called PLA format. So, we will let you edit files in the ESPRESSO truth table format, and those can be uploaded and optimized by SIS.

The new information you need is how to read a SIS output result, since the result is an optimized Boolean network model, each of whose nodes is an optimized 2-level SOP form. Let's look at a few small examples to see how to read a SIS result.

EXAMPLE 1: 2 functions of 4 variables
Here are two functions named s1 and s0, each a function of input variables a1 a0 b1 b0. This is specified in the ESPRESSO PLA format:

***.i 4***
***.o 2***
***.ilb a1 a0 b1 b0***
***.ob s0 s1***
***0000 00***
***0001 00***
***0010 00***
***0011 00***
***0100 00***
***0101 01***
***0110 10***
***0111 11***
***1000 00***
***1001 10***
***1010 01***
***1011 00***
***1100 00***
***1101 11***
***1110 00***
***1111 00***
***.e***