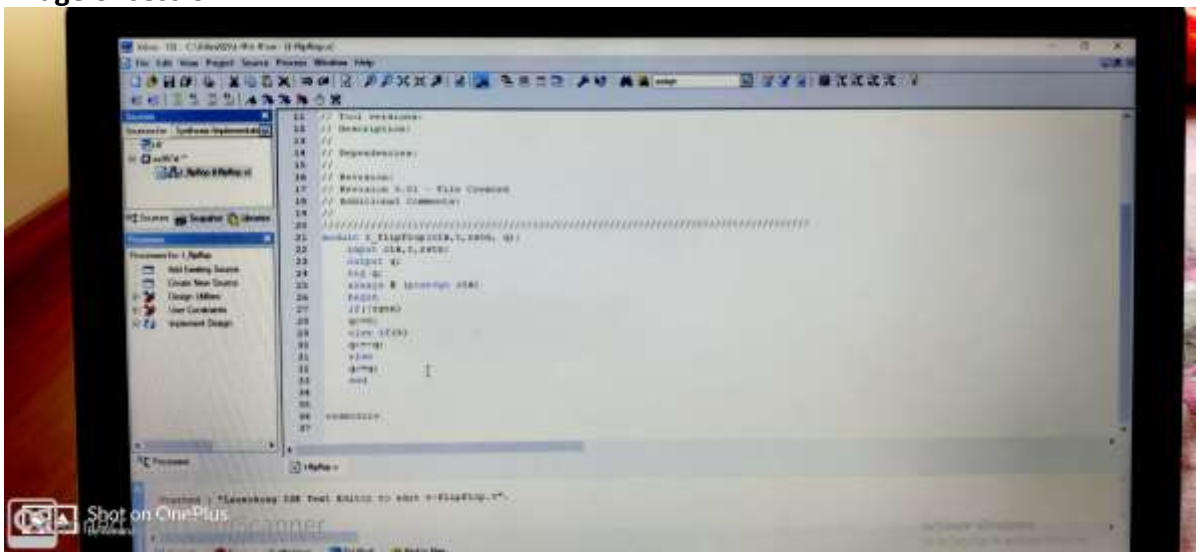
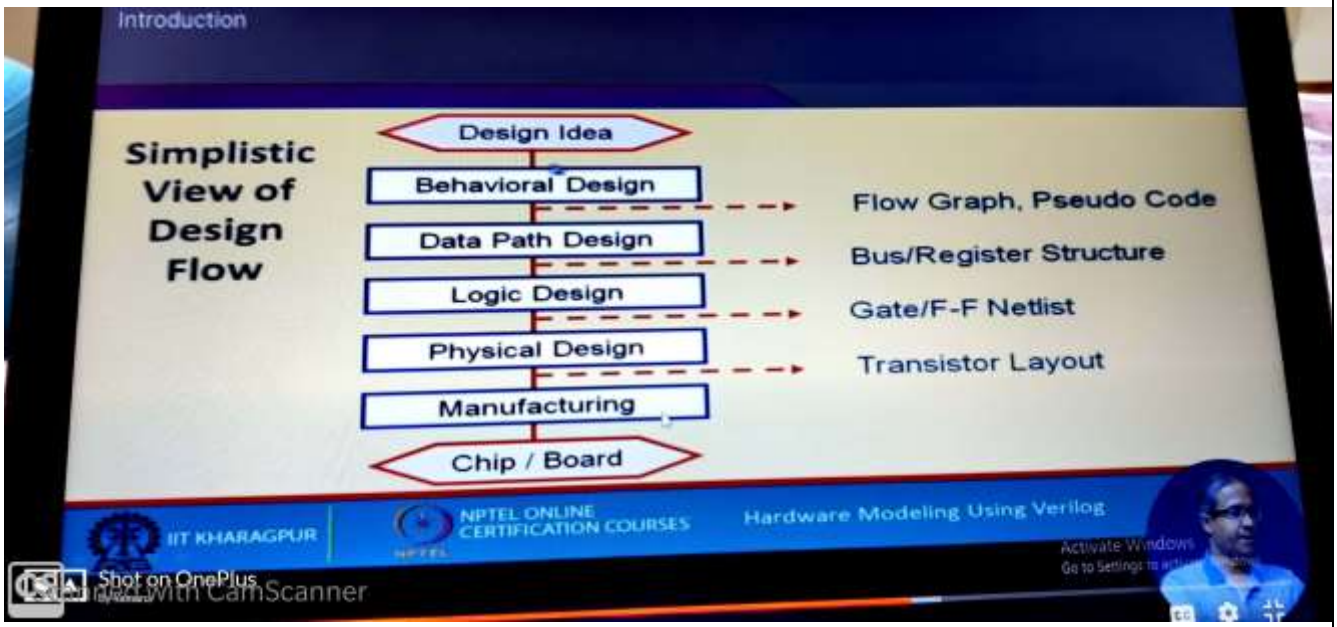
DAILY ASSESSMENT FORMAT

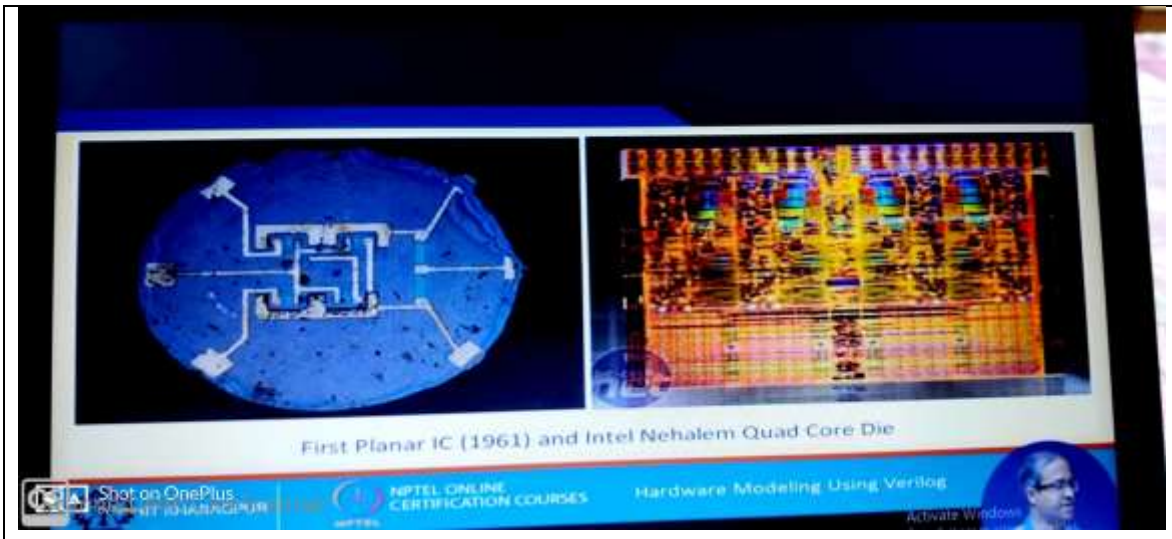
Date:	**04 june 2020**	**Name:**	**Yamunshree N**
Course:	**HDL**	**USN:**	**4AL17EC097**
Topic:	**Hardware modelling using Verilog FPGA and ASIC interview questions**	**Semester & Section:**	**6TH SEM B SEC**
Github Repository:	**yamunashree-courses**		

FORENOON SESSION DETAILS

Image of session







2) Difference between blocking and non-blocking?(Verilog interview questions that is most commonly asked)

The Verilog language has two forms of the procedural assignment statement: blocking and non-blocking. The two are distinguished by the = and <= assignment operators. The blocking assignment statement (= operator) acts much like in traditional programming languages. The whole statement is done before control passes on to the next statement. The non-blocking (<= operator) evaluates all the right-hand sides for the current time unit and assigns the left-hand sides at the end of the time unit. For example, the following Verilog program

```
// testing blocking and non-blocking assignment

module blocking;
reg [0:7] A, B;
initial begin: init1
A = 3;
#1 A = A + 1; // blocking procedural
```

asic.co.in/index_files/veri

Verilog interview Questions & answers for FPGA & ASIC

1) Write a verilog code to swap contents of two registers with and without a temporary register?

With temp reg :

```
always @ (posedge clock)
begin
temp=b;
b=a;
a=temp;
end
```

Without temp reg:

```
always @ (posedge clock)
begin
a <= b;
b <= a;
end
```

Click to view more

Show simplified view

Hardware Modelling using Verilog

Day 1

VLSI Design Process

* Design Complexity increasing rapidly
  -> increased size and complexity
  -> fabrication technology improving
  -> CAD tools are essential
  -> Conflicting requirements like area, speed and energy consumption

Moore's Law

Exponential Growth
Design complexity increases rapidly
Automated tools are essential
Must follow well-defined design flow.

VLSI design flow:

Standardized design procedure
-> starting from the design idea down to the actual implementation.

Encompasses many steps:
-> specification
-> Synthesis
-> Simulation
-> Layout
-> Testability analysis

Need to use Computer Aided Design (CAD) tools:
-> Based on Hardware Description Language
-> HDLs provide formats for representing the output

* various design steps

-> CAD tools transforms the HDL input into a HDL output that contains more detailed information about the hardware.

* Difference b/w blocking and non-blocking:

Task Day4:

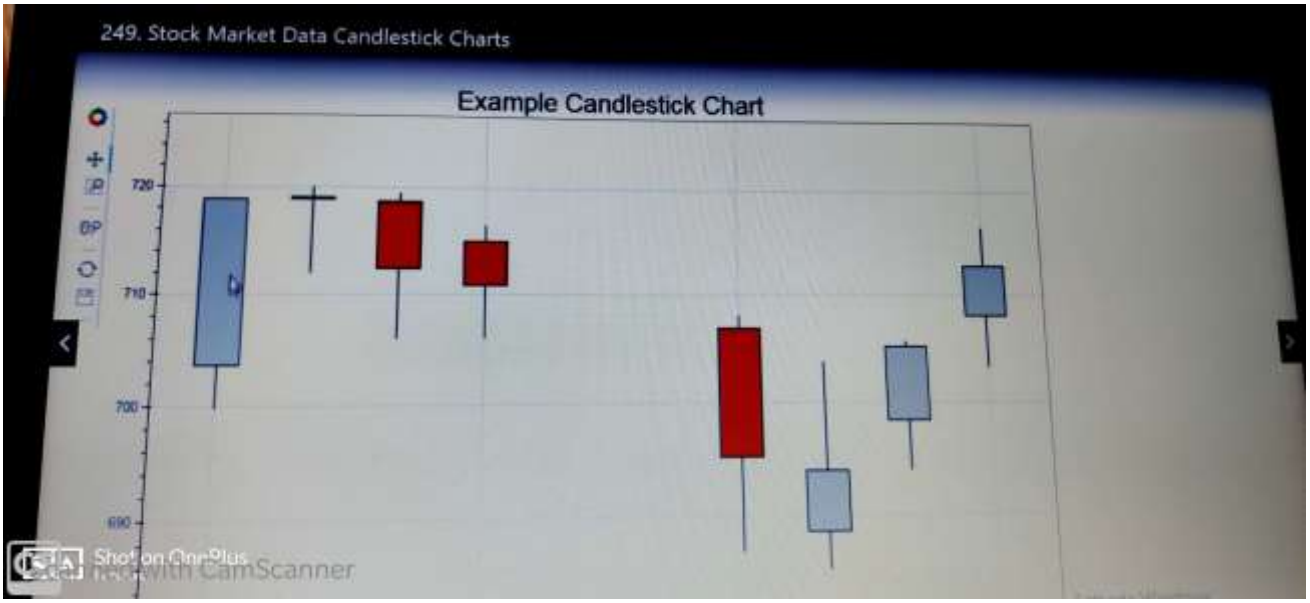
Implement a simple T flipflop and test the module using a compiler

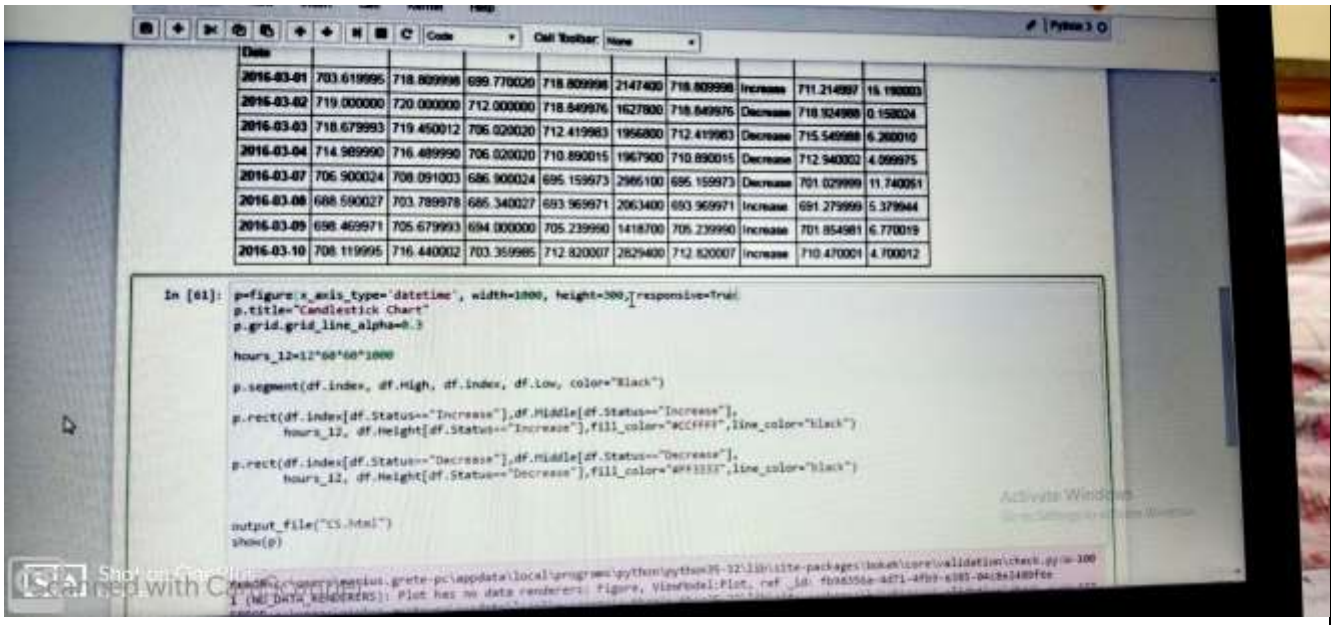
```
module tff (input clk, input rstn, input t,
                                output reg q);

always @ (posedge clk)
begin
 if (!rstn)
   q <= 0;
 else
   if (t)
     q <= ~q;
   else
     q <= q;
end
endmodule
```

Date:	04 june 2020	Name:	Yamunashree N
Course:	Python Programming	USN:	4AL17EC097
Topic:	Application 9: Build a web-based financial graph	Semester & Section:	6th sem B sec

AFTERNOON SESSION DETAILS

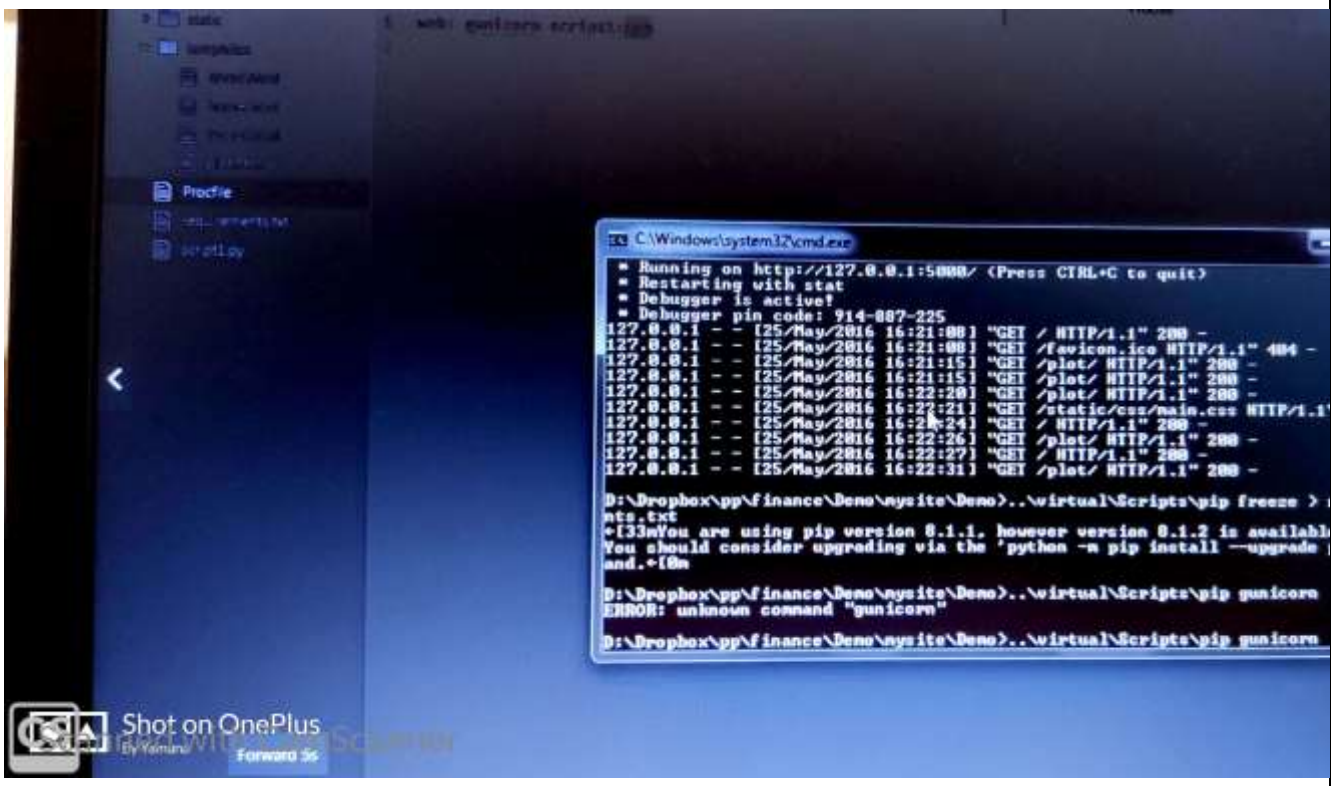
Image of session





Date									
2016-03-01	703.619995	718.809998	699.770020	718.809998	2147400	718.809998	Increase	711.214997	15.190003
2016-03-02	719.000000	720.000000	712.000000	718.849976	1627800	718.849976	Decrease	718.924988	0.150024
2016-03-03	718.679993	719.450012	706.020020	712.419983	1956800	712.419983	Decrease	715.549988	6.280010
2016-03-04	714.989990	716.489990	706.020020	710.890015	1967900	710.890015	Decrease	712.940002	4.099975
2016-03-07	706.900024	708.091003	686.900024	695.159973	2986100	695.159973	Decrease	701.029999	11.740051
2016-03-08	688.590027	703.789978	686.340027	693.969971	2063400	693.969971	Increase	691.279999	5.379944
2016-03-09	698.469971	705.679993	694.000000	705.239990	1418700	705.239990	Increase	701.854981	6.770019
2016-03-10	708.119995	716.440002	703.359985	712.820007	2829400	712.820007	Increase	710.470001	4.700012

```
In [61]: p=figure(x_axis_type='datetime', width=1000, height=300,responsive=True)
         p.title="Candlestick Chart"
         p.grid.grid_line_alpha=0.3

         hours_12=12*60*60*1000

         p.segment(df.index, df.High, df.index, df.Low, color="Black")

         p.rect(df.index[df.Status=="Increase"],df.Middle[df.Status=="Increase"],
                hours_12, df.Height[df.Status=="Increase"],fill_color="#CCFFFF",line_color="black")

         p.rect(df.index[df.Status=="Decrease"],df.Middle[df.Status=="Decrease"],
                hours_12, df.Height[df.Status=="Decrease"],fill_color="#FFCCCC",line_color="black")


         output_file("CS.html")
         show(p)
```

```
C:\Windows\system32\cmd.exe
 * Running on http://127.0.0.1:5000/ (Press CTRL+C to quit)
 * Restarting with stat
 * Debugger is active!
 * Debugger pin code: 914-887-225
127.0.0.1 - - [25/May/2016 16:21:00] "GET / HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:21:00] "GET /favicon.ico HTTP/1.1" 404 -
127.0.0.1 - - [25/May/2016 16:21:15] "GET /plot/ HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:21:15] "GET /plot/ HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:22:20] "GET /plot/ HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:22:21] "GET /static/css/main.css HTTP/1.1
127.0.0.1 - - [25/May/2016 16:22:24] "GET / HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:22:26] "GET /plot/ HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:22:27] "GET / HTTP/1.1" 200 -
127.0.0.1 - - [25/May/2016 16:22:31] "GET /plot/ HTTP/1.1" 200 -

D:\Dropbox\pp\finance\Demo\mysite\Demo>..\virtual\Scripts\pip freeze > r
nts.txt
←[33mYou are using pip version 8.1.1, however version 8.1.2 is availabl
You should consider upgrading via the 'python -m pip install --upgrade
and.←[0m

D:\Dropbox\pp\finance\Demo\mysite\Demo>..\virtual\Scripts\pip gunicorn
ERROR: unknown command "gunicorn"

D:\Dropbox\pp\finance\Demo\mysite\Demo>..\virtual\Scripts\pip gunicorn
```

Application 9 :- Build a Web - Based Financial Graph

Day 16

Downloading Datasets with Python :-

```
from pandas-datareader import data
import datetime
start = datetime.datetime(2016, 3, 1)
end = datetime.datetime(2016, 3, 1)
data = DataReader("AAPL", data_source
                  = "yahoo", start=start, end=end)

from flask import Flask, render_template
app = Flask(__name__)
@app.route('/')
def home():
    return render_template("home.html")
@app.route('/about/')
def about():
    return render_template("about.html")
if __name__ == "__main__":
    app.run(debug=True)
```