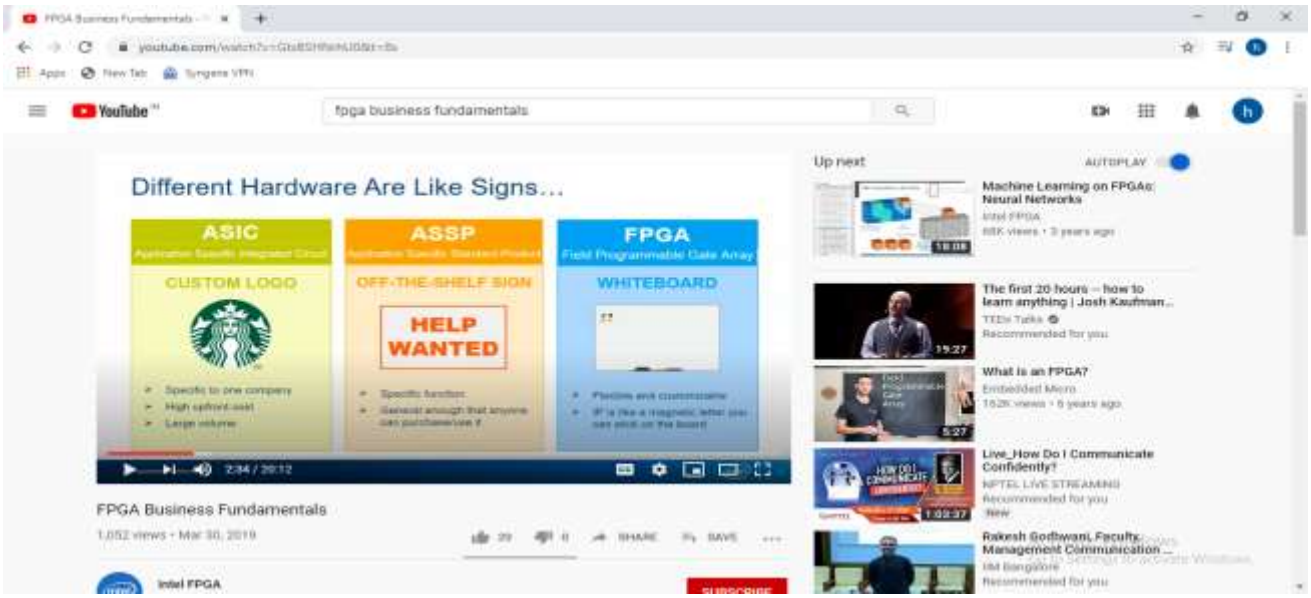
DAILY ASSESSMENT FORMAT

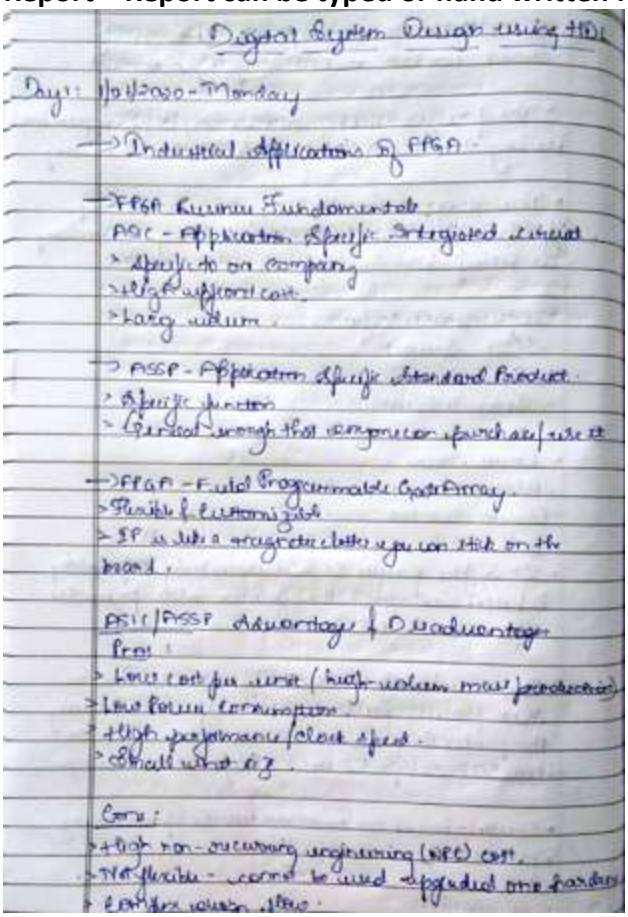
Date:	**01-06-2020**	**Name:**	**Yamunashree N**
Course:	**Digital Design using HDL**	**USN:**	**4AL17EC097**
Topic:	**1.Industry Applications of FPGA 2.FPGA Business Fundamentals 3.FPGA vs ASIC design flow 4.FPGA Basics-A look under the hood**	**Semester & Section:**	**6 SEM & 'B' SEC**
Github Repository:	**yamunashree-courses**		

FORENOON SESSION DETAILS

Image of session



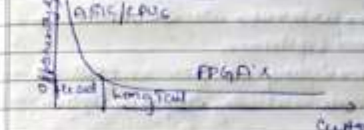
Report – Report can be typed or hand written for up to two pages.



Why FPGA?

> Reprogrammable & Flexible
> Product Longevity
> Reduced Time-to-Market
> Market-Size Optimized

Broad Customer Base



Reduced Time to Market

Developing & prototyping on FPGA's can reduce TTM, especially in emerging markets where standards have not yet been developed.

Software Enabled on Hardware

- Intel heavily invests in Quartus, because it is paramount to the success of our FPGAs
- In order to play in the FPGA market, companies need to first have good tools.

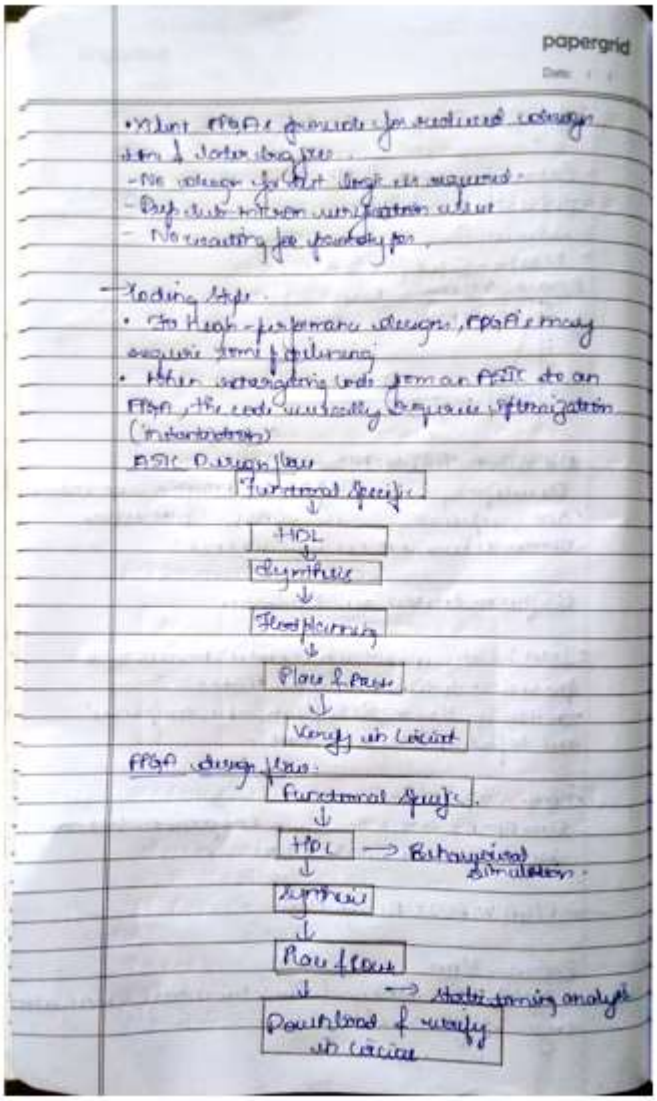
Future with Intel

Our FPGAs are more than a component. We are part of an Entire Intel Solution.

→ FPGA vs ASIC Design Flow

Design Flow

- ASIC & FPGA design & implementation methodologies differ somewhat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Functional Specific
HDL
Synthesis
Floor Planning
Place & Route
Verify in Circuit
Functional Specific.
HDL
Bitstream
Synthesis
Route
Static timing analysis
Download & verify in circuit

papergrid

Date / /

-> FPGA Basics - A look under the hood
- Strengths & weaknesses of FPGA's
- How FPGA's work.
- What's inside an FPGA.

> What is an FPGA?

An FPGA is a (mostly) [illegible] (re)-configurable ASIC because there are [illegible] & [illegible] aspects to modern FPGAs.

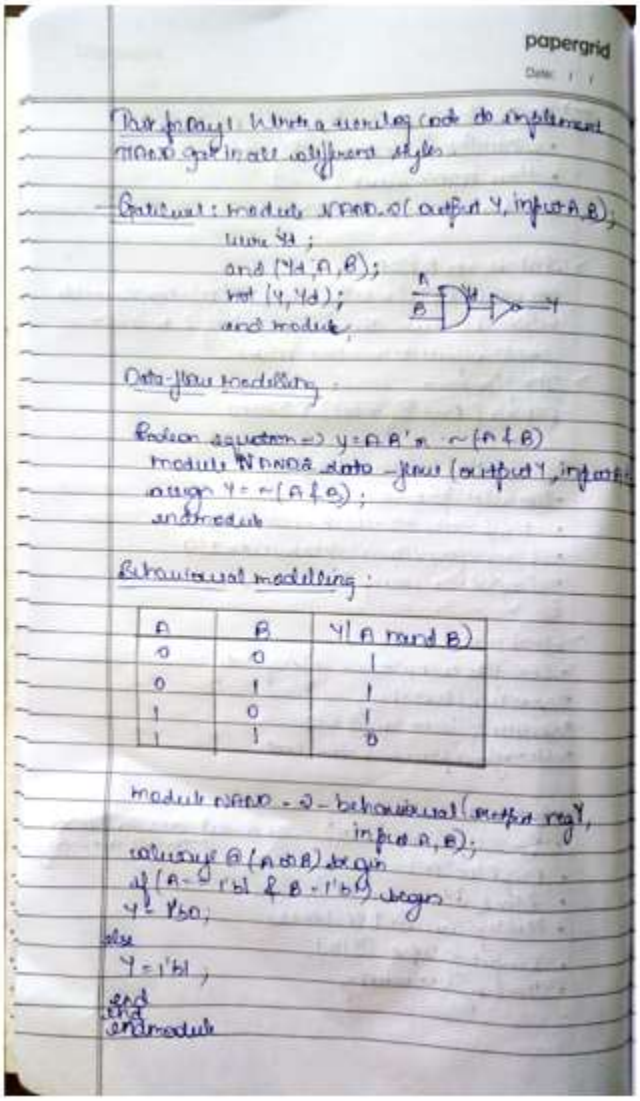
> The players -

Altera (Part of intel) & Xilinx.

> Strengths / well suited for
- Parallel process
- High data-to-clock-rate-ratio
- Large quantities of deterministic I/O.
- Signal Processing.

> Weakness
- Complex calculations infrequently
- Sorting / searching
- Floating point arithmetic
- Very low power & low cost.

> What inside - Core Components
- Look Up Table (LUT) - acts as a [illegible] register also small memory
- Flip Flop (FF)
- Block Memory (BM)
- Multiplier or DSP blocks
- Input/Output (I/O)
- Clocking & [illegible]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Aim for today: Write a verilog code to implement NAND gate in all different styles.

Gate level: module NAND_G(output Y, input A, B);
wire Yd;
and (Yd, A, B);
not (Y, Yd);
endmodule;

Data-flow modelling:

Boolean equation => Y = A B)' = ~(A & B)
module NAND_DF data_flow (output Y, input A, B);
assign Y = ~(A & B);
endmodule

Behavioural modelling:

A	B	Y (A nand B)
0	0	1
0	1	1
1	0	1
1	1	0

module NAND_B behavioural (output reg Y, input A, B);
always @ (A or B) begin
if (A == 1'b1 & B == 1'b1) begin
Y = Y50;
else
Y = 1'b1;
end
endmodule

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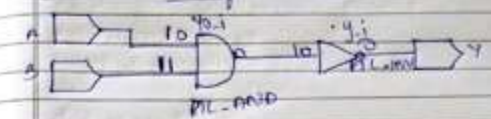
Date: / /

A) Schematic of the NAND gate.

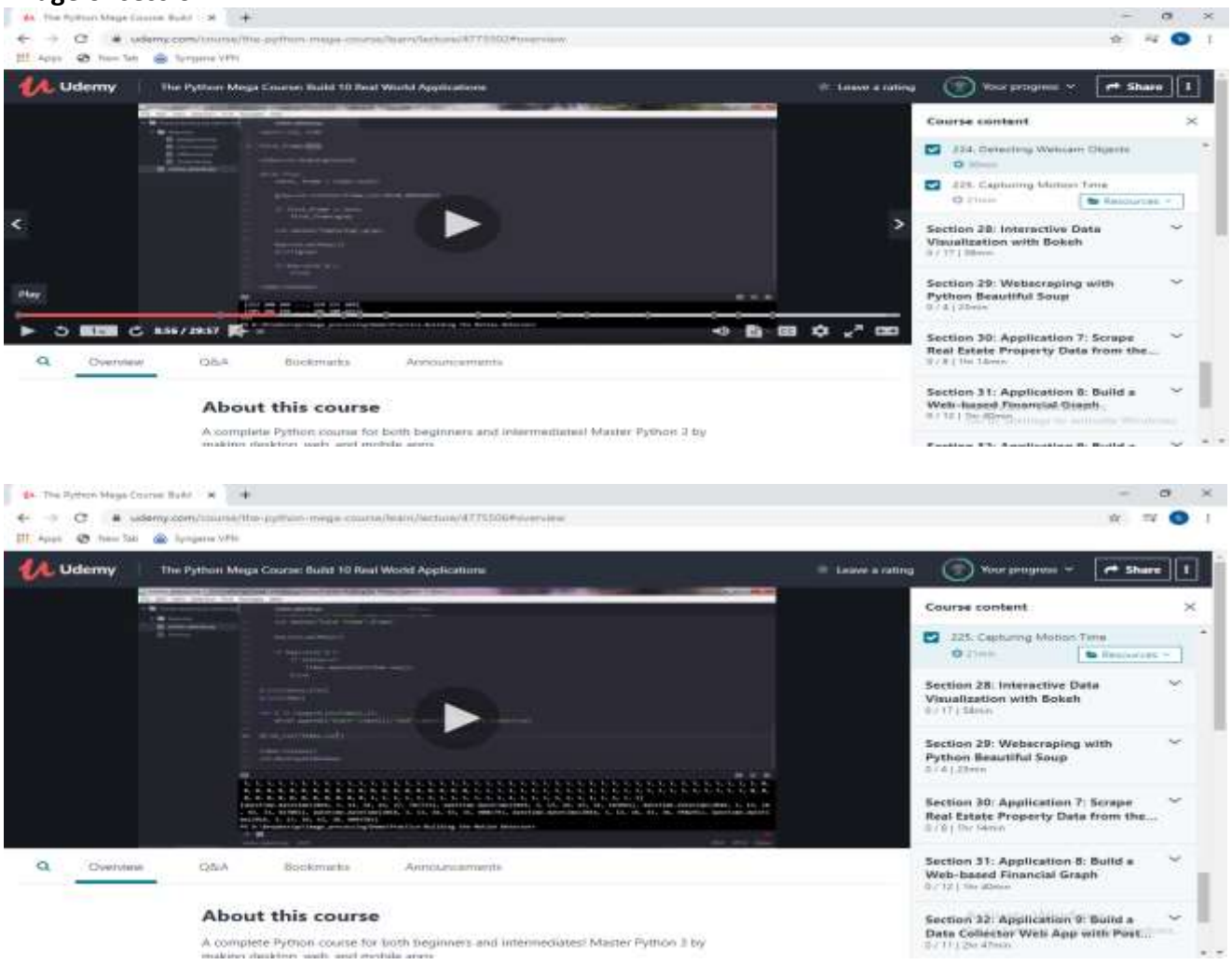


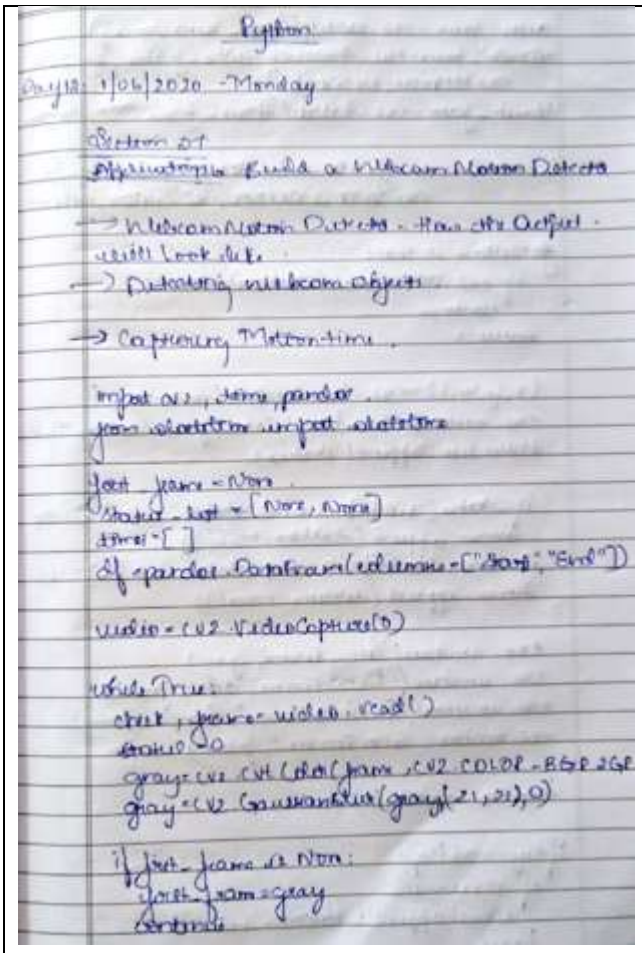

```
include "NAND_2_behavioural.v"
module NAND_2_behavioural_th;
reg A,B;
wire Y;
NAND_2_behavioural Instance1 (Y,A,B);
initial begin
    A=0; B=0;
#1  A=0; B=1;
#1  A=1; B=0;
#1  A=1; B=1;
end
initial begin
    $monitor("T=%t|A=%d\B=%d\Y=%d",
                $time,A,B,Y);
    $dumpfile("dump.vcd");
    $dumpvars();
end
endmodule.
```

Date:	**01-06-2020**	**Name:**	**Yamunashree N**
Course:	**PYTHON Programming**	**USN:**	**4AL17EC097**
Topic:	**Section 27**	**Semester & Section:**	**6 SEM & 'B' SEC**
Github Repository:	**yamunashree-courses**		

AFTERNOON SESSION DETAILS

Image of session





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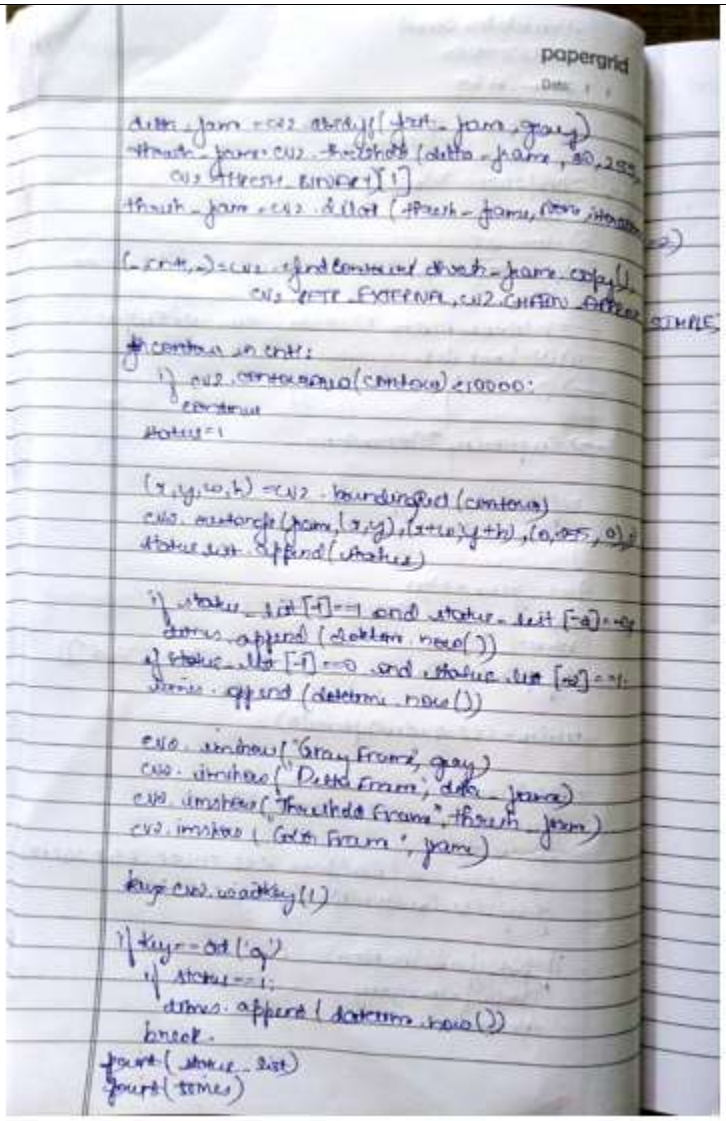
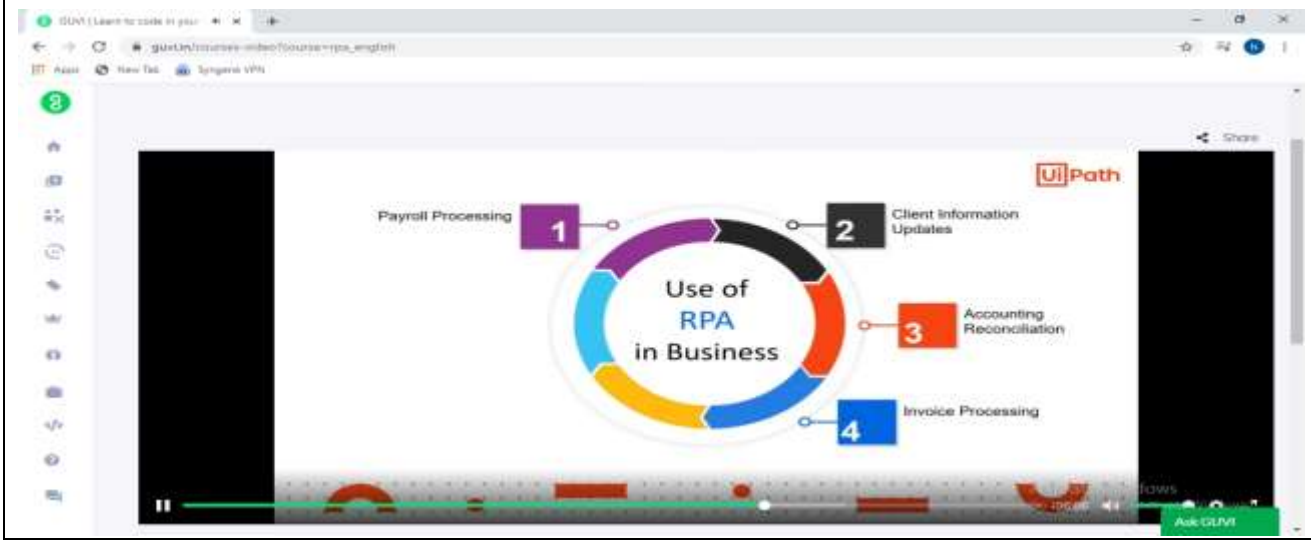
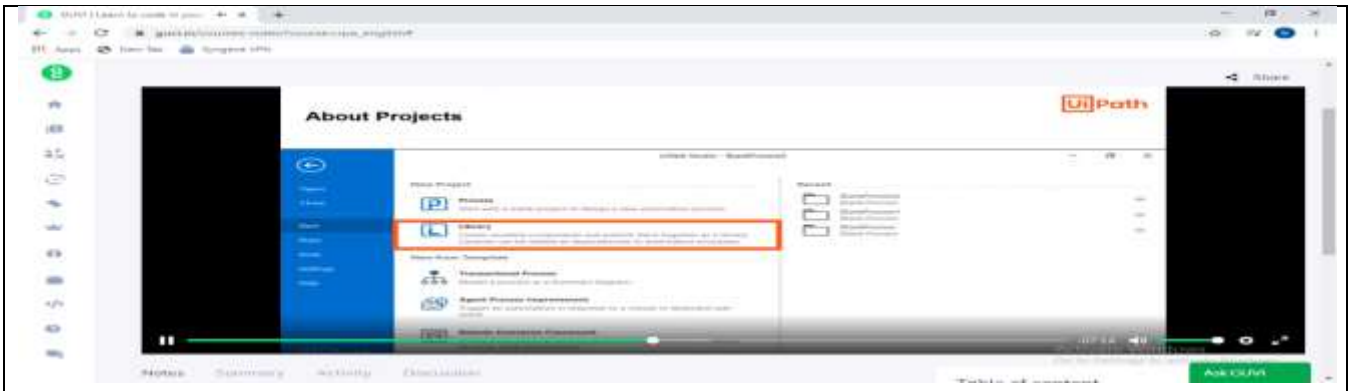


Certification course on RPA Skill-A-Thon : Step into RPA





RPA : (Robotic Process Automation)

1/06/2020

→ Introduction to RPA
- Limits human action
- Work seamlessly with existing IT systems
- Easy to configure & powerful to scale
- Work without mistakes & 24x7
- Reads & processes data in a structured form.

→ RPA is about automating human digital interfaces.

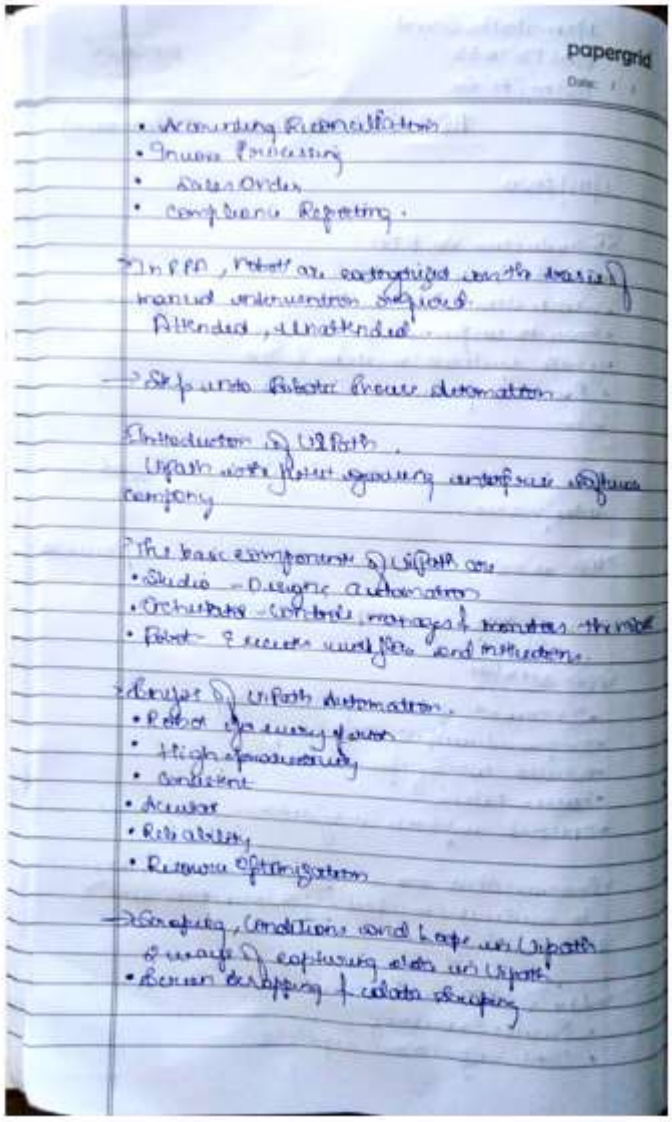
→ RPA is not a humanoid robot, human replacement

→ The future of work with RPA

→ RPA benefits
- Increased process productivity
- Improved output accuracy
- Reduced cost of process execution
- Process velocity
- Ensured uniform regulatory compliance

→ Process that are simple, structured & can be easily automated by a machine are best suited for RPA

→ Use of RPA in Business
- Payables Processing
- Client [illegible]



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- Accounting Reconciliation
- Invoice Processing
- Sales Order
- Compliance Reporting.

→ In RPA, Robots are categorized with degree of manual intervention required.
Attended, Unattended

→ Steps into Robotic Process Automation.

Introduction of UiPath.
UiPath uses Robot Operating enterprise software company

The basic components of UiPath are
- Studio - Designs automations
- Orchestrator - Controls, manages & monitors the robot
- Robot - Executes workflows and instructions.

Benefits of UiPath Automation.
- Robots are very powerful
- High productivity
- Consistent
- Accurate
- Reliability
- Resource optimization

→ Scraping, Conditions and Loops use UiPath
- Usage of capturing data in UiPath
- Screen scraping & data scraping

> Data Scraping: It is the process of extracting structured data from a [illegible], application or document to a database, csv file or to Excel spreadsheets.

> Types of Recording in Uipath Studio.

- Basic Recorder
- Desktop Recorder
- Web Recorder
- Image Recorder
- Native Citrix Recorder

> Sequence:

It is the smallest type of project suitable for linear processes as they enable you to go from one activity to another seamlessly & act as a single block activity.

> Flowchart: A flowchart is a type of project in Uipath that offers a very good representation of the activities used & the underlying projects.

> Loop: A loop is a programming structure that depends on repeat a sequence of instructions until a specific condition is met.

> Basic Automation workflows.

> Data Persistence: It is the property of data to survive in the same form after the process or application which has created it has ended. For data to persist it needs to be stored in a non-volatile memory > RAM > Data is saved on hard drive

GUVI

tech deserves you

Yamunashree N

is here by awarded the certificate of achievement for

the successful completion of

Step into Robotic Process Automation

during GUVI's RPA SKILL-A-THON 2020

S.P.Balamurugan

Co-founder, CEO

Valid certificate ID G0C0uX384c1059lv95

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