Trabajo Fin de Máster
Máster en Ingeniería Electrónica, Robótica y Automática

Aerial co-workers: a task planning approach for multi-drone teams supporting inspection operations

Autor: Álvaro Calvo Matos

Tutor: Jesús Capitán Fernandez

Dpto. Ingeniería de Sistemas y Automática
Escuela Técnica Superior de Ingeniería
Universidad de Sevilla

Sevilla, 2021

Trabajo Fin de Máster
Máster en Ingeniería Electrónica, Robótica y Automática

Aerial co-workers: a task planning approach for multi-drone teams supporting inspection operations

Autor:
Álvaro Calvo Matos

Tutor:
Jesús Capitán Fernandez
Associate Professor

Dpto. Ingeniería de Sistemas y Automática
Escuela Técnica Superior de Ingeniería
Universidad de Sevilla

Sevilla, 2021

Trabajo Fin de Máster: Aerial co-workers: a task planning approach for multi-drone teams supporting inspection operations

Autor: Álvaro Calvo Matos
Tutor: Jesús Capitán Fernandez

El tribunal nombrado para juzgar el trabajo arriba indicado, compuesto por los siguientes profesores:

Presidente:

Vocal/es:

Secretario:

acuerdan otorgarle la calificación de:

El Secretario del Tribunal

Fecha:

Agradecimientos

A mi tutor, Hipólito, por guiarme en este proyecto, pero sobre todo, por darme la oportunidad de formar parte de su equipo desde tan temprano, otorgándome la plaza de alumno interno que me ha llevado a la realización de este TFG. A pesar de los momentos en los que ha escaseado el tiempo, ha sido una experiencia muy buena que reperitía sin dudarlo.

A María, por su ayuda cada vez que la he necesitado, a Luis, por guiarme en los inicios con la programación y solucionarme cada nuevo problema que me surgía, y a Dani, por las pequeñas ayudas que ha realizado.

A todos aquellos profesores que demostraban día a día la pasión por su trabajo y que hacían de aprender la mejor de las experiencias.

A mis maestros y maestras del Colegio Salesiano de Utrera, por su dedicación. Especialmente a mis profesores Elena y Fernando, por sus enseñanzas, pero sobre todo por su cariño, su comprensión y su paciencia conmigo. Y en particular a Eduardo, por todo lo que aprendí de informática y de física, pero sobre todo, por hablarme de los campus científicos que me han traído directamente hasta aquí.

A mis compañeros de clase, por acompañarme durante todo el camino.

A Damián, por su apoyo y amistad en todo momento durante este último año.

A mis amigos de Utrera, por tener paciencia y no haberme abandonado tras cuatro años desaparecido con mis estudios.

A mi familia, por su amor y apoyo incondicional.

A mi abuelo, que a pesar de no haber podido estar aquí, se ha ido dejándome la mejor herencia que se puede dejar, una buena educación.

Álvaro Calvo Matos
Grado en Ingeniería Electrónica, Robótica y Mecatrónica

Sevilla, 2020

Abstract

Lorem itsum

Short Outline

Contents

1 Introduction

Lorem itsum

1.1 Motivation

1.2 Objectives

Hypothesis 1.2.1 *"Dos Single Event Upset (SEU) próximos entre sí provocarán patrones de error similares a la salida".*

2 State of the art

2.1 Task planning in multi-drone teams

2.2 Drone behavior management

2.2.1 Finite state machines

2.2.2 Behaviour Trees

3 Problem Description

Lorem itsum

4 Design of the proposed solution

Lorem itsum

5 Conclusions and future work

5.1 Conclusions

5.2 Future work

List of Figures

List of Tables

List of Codes

Bibliography

[1] M. Santarini, "Cosmic radiation comes to asic and soc design," May 2005. [Online]. Available: https://www.edn.com/cosmic-radiation-comes-to-asic-and-soc-design/

[2] H. G. Miranda, "Aportaciones a las técnicas de emulación y protección de sistemas microelectrónicos complejos bajo efectos de la radiación," Ph.D. dissertation, Universidad de Sevilla, May 2010.

[3] J. M. Mogollón, J. Nápoles, H. Guzmán-Miranda, and M. A. Aguirre, "Real time seu detection and diagnosis for safety or mission-critical ics using hash library-based fault dictionaries," in *2011 12th European Conference on Radiation and Its Effects on Components and Systems*, 2011, pp. 705–710.

[4] M. G. Valderas, M. P. García, C. López, and L. Entrena, "Extensive seu impact analysis of a pic microprocessor for selective hardening," in *2009 European Conference on Radiation and Its Effects on Components and Systems*, 2009, pp. 333–336.

[5] C. Carmichael, "Triple module redundancy design techniques for virtex fpgas," *Xilinx Application Note XAPP197*, vol. 1, 2001.

[6] Zhou Jing, Liu Zengrong, Chen Lei, Wang Shuo, Wen Zhiping, Chen Xun, and Qi Chang, "An accurate fault location method based on configuration bitstream analysis," in *NORCHIP 2012*, 2012, pp. 1–5.

[7] W. Tao and W. Xingsong, "Fault diagnosis of a scara robot," in *2008 15th International Conference on Mechatronics and Machine Vision in Practice*, 2008, pp. 352–356.

[8] S. Jian, J. Jiang, K. Lu, and Y. Zhang, "Seu-tolerant restricted boltzmann machine learning on dsp-based fault detection," in *2014 12th International Conference on Signal Processing (ICSP)*, 2014, pp. 1503–1506.

[9] R. Pettit and A. Pettit, "Detecting single event upsets in embedded software," in *2018 IEEE 21st International Symposium on Real-Time Distributed Computing (ISORC)*, 2018, pp. 142–145.

[10] N. Naber, T. Getz, Y. Kim, and J. Petrosky, "Real-time fault detection and diagnostics using fpga-based architectures," in *2010 International Conference on Field Programmable Logic and Applications*, 2010, pp. 346–351.

[11] Su Wei, Fan Tongshun, and Du Mingfang, "Research for digital circuit fault testing and diagnosis techniques," in *2009 International Conference on Test and Measurement*, vol. 1, 2009, pp. 330–333.

[12] S. Wei, Z. Shide, and X. Lijun, "Research on digital circuit fault location procedure based on lasar," in *2008 ISECS International Colloquium on Computing, Communication, Control, and Management*, vol. 2, 2008, pp. 322–326.

[13] B. K. Sikdar, N. Ganguly, and P. P. Chaudhuri, "Fault diagnosis of vlsi circuits with cellular automata based pattern classifier," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 7, pp. 1115–1131, 2005.

[14] S. S. Yau and Yu-Shan Tang, "An efficient algorithm for generating complete test sets for combinational logic circuits," *IEEE Transactions on Computers*, vol. C-20, no. 11, pp. 1245–1251, 1971.

[15] S. S. Yau and M. Orsic, "Fault diagnosis and repair of cutpoint cellular arrays," *IEEE Transactions on Computers*, vol. C-19, no. 3, pp. 259–262, 1970.

[16] V. Amar and N. Condulmari, "Diagnosis of large combinational networks," *IEEE Transactions on Electronic Computers*, vol. EC-16, no. 5, pp. 675–680, 1967.

[17] D. R. Schertz and G. Metze, "A new representation for faults in combinational digital circuits," *IEEE Transactions on Computers*, vol. C-21, no. 8, pp. 858–866, 1972.

[18] J. P. Roth, W. G. Bouricius, and P. R. Schneider, "Programmed algorithms to compute tests to detect and distinguish between failures in logic circuits," *IEEE Transactions on Electronic Computers*, vol. EC-16, no. 5, pp. 567–580, 1967.

[19] A. D. Friedman, "Fault detection in redundant circuits," *IEEE Transactions on Electronic Computers*, vol. EC-16, no. 1, pp. 99–100, 1967.

[20] R. Zhang, L. Xiao, J. Li, X. Cao, C. Qi, and M. Wang, "A fast fault injection platform of multiple seus for sram-based fpgas," in *2017 Prognostics and System Health Management Conference (PHM-Harbin)*, 2017, pp. 1–5.

[21] A. da Silva and S. Sanchez, "Leon3 vip: A virtual platform with fault injection capabilities," in *2010 13th Euromicro Conference on Digital System Design: Architectures, Methods and Tools*, 2010, pp. 813–816.

[22] J. M. Mogollon, H. Guzmán-Miranda, J. Nápoles, J. Barrientos, and M. A. Aguirre, "Ftunshades2: A novel platform for early evaluation of robustness against see," in *2011 12th European Conference on Radiation and Its Effects on Components and Systems*, 2011, pp. 169–174.

[23] Wikipedia, "Distancia de levenshtein — wikipedia, la enciclopedia libre," 2020, [Internet; descargado 15-junio-2020]. [Online]. Available: https://es.wikipedia.org/w/index.php?title=Distancia_de_Levenshtein&oldid=125248609

[24] M. Muñoz-Quijada, S. Sanchez-Barea, D. Vela-Calderon, and H. Guzman-Miranda, "Fine-grain circuit hardening through vhdl datatype substitution," *Electronics*, vol. 8, no. 1, p. 24, 2019.

[25] "Vhdl implementation of fft algorithm(s)," Available online: https://github.com/thasti/fft, accessed on 17 June 2020.

[26] "Vhdl standard fifo," Available online: http://www.deathbylogic.com/2013/07/vhdl-standard-fifo/, accessed on 17 June 2020.

[27] "Fpga4student. a low pass fir filter for ecg denoising in vhdl," Available online: https://www.fpga4student.com/2017/01/a-low-pass-fir-filter-in-vhdl.html, accessed on 17 June 2020.

[28] "I^2s interface designed for the pcm3168 audio interface from texas instruments," Available online: https://github.com/wklimann/PCM3168, accessed on 17 June 2020.

[29] "Simple uart controller for fpga written in vhdl," Available online: https://github.com/jakubcabal/uart-for-fpga, acceded on 17 June 2020.

[30] Wikipedia, "Momentos de imagen — wikipedia, la enciclopedia libre," 2020, [Internet; descargado 18-junio-2020]. [Online]. Available: https://es.wikipedia.org/w/index.php?title=Momentos_de_imagen&oldid=124767713

[31] C. Wolf, J. Glaser, and J. Kepler, "Yosys-a free verilog synthesis suite," in *Proceedings of the 21st Austrian Workshop on Microelectronics (Austrochip)*, 2013.

Glossary

SEU Single Event Upset. 1