

DSD

COURSEWORK

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Requirements to complete this coursework:

Quartus Prime Lite (v.18.1 or v20.1);

Nios II Embedded Design Suite (v.18.1 or v 20.1);

Modelsim (Modelsim-Altera or ActiveHDL);

Matlab (or Python);

Terasic DE1-SoC board;

Coursework source files including DE1-SoC documentation;

On-line references from Intel.

Windows 10

Legend:



Important information.



Reference material that you should read before proceeding.




Work you should deliver. A set of tasks for you to do, and deliverables to include in your report.



Debug hints



Helpful information

 Please read this document carefully before starting the coursework as it will guide you to complete the coursework efficiently. There are links to references that explain, and exemplify, procedures you will need to know how to do. You're advised to read and understand them.

INTRODUCTION

In this coursework you will acquire experience in the design of digital systems. As a case study, we will focus on the acceleration of computationally intensive applications and we will see how having customising hardware blocks tuned for a certain application can lead to a better performing system compared to one that does not have these computational units.

In this coursework we will start by running applications on a generic central processing unit (CPU), assess the system's performance and then focus on the design of dedicated hardware processing elements for the acceleration of the same applications.

The system design will target a Field-Programmable Gate Array (FPGA) from Intel. They are generic digital devices that support the implementation of any digital hardware design after their fabrication, including the implementation of soft-processors. The FPGA you're going to use is on a development kit (DE1-SoC) from Terasic, which is available in the lab. The target CPU is the soft-processor NIOS II, also provided by Intel. More information about NIOS II can be found here:



<https://www.intel.co.uk/content/www/uk/en/products/programmable/processor/nios-ii.html>

The main application for configuration of the FPGA is Quartus from Intel. It allows to design and program digital systems based on FPGAs. The Platform Designer tool allows the implementation of a complex digital system including a CPU and all the required components to make it work. You can find more about it here:



<https://www.intel.com/content/www/us/en/programmable/products/design-software/fpga-design/quartus-prime/features/qts-platform-designer.html>

You will program the NIOS II processor by writing C code using EDS. How to do this is described in the tutorial pointed out in the hand-out.

In the coursework you are about to do, you'll start by describing your system in Platform Designer (which you can access from Quartus), synthesize it in Quartus, and then configure the FPGA. At this point you don't need to write any Verilog/VHDL. Verilog is a hardware description language. Later you can use Verilog /block diagrams/VHDL to describe your customized hardware blocks.

Objective: Acceleration of Arithmetic Functions

In this coursework you are going to see how dedicated hardware can be applied to a general-purpose digital system in order to accelerate certain parts of the calculations. The more specialised the hardware blocks are, the faster the computation becomes, but that's reflected in FPGA resources or circuit area.

The main purpose of this coursework is to create a digital system that evaluates the following function:

$$f(x) = \sum_{i=1}^N 0.5 * x_i + x_i^2 \cos((x_i - 128)/128) \quad (1)$$

under **single-precision number representation**, for **any** given input vector **x**, where each element of the **vector is a single-precision floating-point number taking values between 0 and 255**.

In order to test and assess the performance of your system, you should use the following test cases (Matlab notation):

1. X=0:5:255
2. X=0:1/8:255

3. $X = 0:1/1024:255$

where x is a single-precision floating-point number. For example, the first case describes an input vector X with the following elements: $[0, 5, 10, 15, \dots, 255]$.¹ Please note that these are specific test examples. **Your system should not be optimised for these instances.**

Your design should be assessed under the following metrics (when they are applicable).

- FPGA resources used by your system (Logic Elements, Embedded Multipliers, Memory Bits). As the target device is fixed, the proposed metric for FPGA resources is the weighted sum of the utilised resources. For example, if your design uses LE Logic Elements, EM Embedded Multipliers, and MB Memory Bits, then the FPGA resources are:

$$\text{FPGA resources} = \frac{1}{3} \left(\frac{LE}{\text{Total } LE \text{ in the device}} + \frac{EM}{\text{Total } EM \text{ in the device}} + \frac{MB}{\text{Total } MB \text{ in the device}} \right)$$

- Latency or Execution time – This is the time that is needed for your system to compute (1) for an input vector X . This includes only the time needed for the evaluation of (1) for the whole vector, without taking into account any initialisation time and so on.
- Application size (program).

Thus, you should be able to plot the performance of your design in a performance vs FPGA resources plot and compare different solutions.

Task 1: NIOS II Setup

In this task you will get familiar with the design of a NIOS II processor and the design choices that impact the system's performance.

Altera, the manufacturer of your target FPGA, offers an embedded processor (also known as soft-processor), named NIOS II, which can be instantiated in any design, and even more than once. The software programming for NIOS II is done in EDS (Eclipse) using C code.



Learn how to setup a system with a NIOS II processor, and start building your project. Download the project template (system_template_de1_soc) available on the DSD coursework page. Place the files to a directory of your choice.

Do not use spaces in the directory path name.

Do not download and install the design files from Altera.

¹ Hint: When you generate the input vector in Matlab/Python for comparing your system's result, you need to generate the elements in the same way as your C code, otherwise the Matlab/Python input and your C code input will differ (think about it). You need to make Matlab/Python to match the generated vectors from your C code.

Your main file is the `hello_word.qpf`. Open the file to see what has been given to you. You will see just some input/output pins only. These pins are connected to specific pins on the FPGA of your board in order to allow your design to communicate with the outside world. In the Project Navigator you will see that the Cyclone V device has been selected as the target device. This is the device that comes with your DE1-SoC board.

The rest of the section is a summary extracted by the NIOS II tutorial provided by Intel (http://www.altera.com/literature/tt/tt_nios2_hardware_tutorial.pdf, <https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an717.pdf>)

Create a New Platform Designer System

The design of the processor is a complex process, but Altera provides a tool (Platform Designer) to help you with this task. Through Platform Designer, you can generate a NIOS II processor system, add the desired components, and configure how they connect together.

Click Platform Designer on the Tools menu in the Quartus II software. A new window will open and your system will have on the clock signal.

Define the System in Platform Designer

You use Platform Designer to define the hardware characteristics of the Nios II system, such as which Nios II core to use, and what components to include in the system. Platform Designer does not define software behaviour, such as where in memory to store instructions or where to send the stderr character stream.

In this section, you perform the following steps:

1. Specify target FPGA and clock settings.
2. Add the Nios II core, on-chip memory, and other components.
3. Specify base addresses and interrupt request (IRQ) priorities.
4. Generate the system.

The Platform Designer design process does not need to be linear. The design steps in this tutorial are presented in the most straightforward order for a new user to understand. However, you can perform Platform Designer design steps in a different order.

Specify Target FPGA and Clock Settings

The **Clock Settings** and the **Project Settings** tabs specify the system's relationship to other devices in the system.

Perform the following steps:

1. On the Platform designer view, select the **Device Family** tab in the bottom left (or go to View -> Device Family) and ensure the device matches the Altera FPGA you are targeting. If a warning appears stating the selected device family does not match the Quartus project settings, ignore the warning. You specify the device in the Quartus project settings later in this tutorial. Since you have run Platform Designer from your project, where the device has been already specified, these fields should be already populated.
2. In the documentation for your board look up the clock frequency of the oscillator that drives the FPGA.
3. In the Platform designer view there should already be a Clock Source (`clk_0`) instantiated. Double click the name to edit the clock frequency. The frequency you specify for `clk_0` must match the oscillator that drives the FPGA. Your board has a 50MHz oscillator. Set this value, if it has not been already populated.

Next, you begin to add hardware components to the Platform Designer system. As you add each component, you configure it appropriately to match the design specifications.

Add the On-Chip Memory

Processor systems require at least one memory for data and instructions. As a starting point, let's use one 20 KB on-chip memory for both data and instructions. To add the memory, perform the following steps:

1. On the **IP Catalog** tab (to the left of the **System Contents** tab), expand **Basic Functions**, expand **On Chip Memory**, and then click **On-Chip Memory (RAM or ROM)**.
2. Click **Add**. The On-Chip Memory (RAM or ROM) parameter editor appears.
3. In the **Type** list, select **RAM (Writeable)**.
4. In the **Block type** list, select **Auto**.
5. In the **Total memory size** box, type 20480 to specify a memory size of 20 KB.

Do not change any of the other default settings

6. Click **Finish**. You return to Platform Designer.
7. Click the **System Contents** tab. An instance of the on-chip memory appears in the system contents table.
8. In the **Name** column of the system contents table, right-click the on-chip memory and click **Rename**.
9. Type onchip_mem and press Enter.

In the System Contents you can see that the memory has been added and possible connections to existing signals have been highlighted. We will come back to these connections later.

Add the Nios II Processor Core

In this section you add the Nios II/f core and configure it to use 2 KB of on-chip instruction cache memory, and without any hardware support for multiplication or division operations.

Perform the following steps to add a Nios II/f core to the system:

1. On the **IP Catalog** tab, expand **Processors and Peripherals -> Embedded Processors**, and then click **Nios II Processor**.
2. Click **Add**. The Nios II Processor parameter editor appears, displaying the **Main** tab. A new GUI pops-up.
3. Under **Select a Nios II core**, select **Nios II/f**.
4. Switch to the **Arithmetic Instructions** tab for **Multiply/Shift/Rotate Hardware** select **Manual Selection**.
5. Set **Multiply Implementation** and **Multiply extended Implementation** to **None**.
6. Set **Divide Hardware** to **None**.
7. Click **Finish**. You return to the **Platform Designer System Contents** tab, and an instance of the Nios II core appears in the system contents table. Ignore the exception and reset vector error messages. You resolve these errors in steps 13 and 14.
8. In the **Name** column, right-click the Nios II processor and click **Rename**.
9. Type cpu and press Enter.
10. In the **Connections** column, connect the clk port of the **clk_0** clock source to both the clk1 port of the on-chip memory and the clk port of the Nios II processor by clicking the hollow dots on the connection line. The dots become solid indicating the ports are connected.

11. Connect the `clk_reset` port of the **clk_0** clock source to both the `reset1` port of the on-chip memory and the `reset` port of the Nios II processor.
12. Connect the `s1` port of the on-chip memory to both the `data_master` port and `instruction_master` port of the Nios II processor.

This last step connects the NIOS processor with the on-chip memory that you have instantiated through the Avalon bus. The NIOS processor serves as the master in this connection (as it initiates transactions) where the memory has a slave interface. The `jtag` signals are used for debugging purposes.

13. Double-click the Nios II processor row of the system contents table to reopen the Nios II Processor parameter editor.
14. Switch to the **Vectors** tab. Under **Reset Vector**, select **onchip_mem.s1** in the **Reset vector memory** list and type `0x0` in the **Reset vector offset** box. This tells to the processor where to set its Program Counter (PC) in case of a reset.
15. Under **Exception Vector**, select **onchip_mem.s1** in the **Exception vector memory** list and type `0x20` in the **Exception vector offset** box.
16. Click the **Caches and Memory Interfaces** tab.
17. In the **Instruction cache** list, select **2 Kbytes**.
18. In the **Add burstcount signal to instruction_master** list, select **Disable**.
19. In the **Number of tightly coupled instruction master port(s)** list, select **None**.

Do not change any settings on the **Advanced Features**, **MMU and MPU Settings**, **JTAG Debug Module**, or **Custom Instruction** tabs.

Add the JTAG UART

The JTAG UART provides a convenient way to communicate character data with the Nios II processor through the USB-Blaster download cable. Perform the following steps to add the JTAG UART:

1. On the **IP Catalog** tab, expand **Interface Protocols**, expand **Serial**, and then click **JTAG UART Intel FPGA IP**.
2. Click **Add**. The JTAG UART parameter editor appears. Do not make any changes.
3. Click **Finish**. You return to the Platform Designer **System Contents** tab, and an instance of the JTAG UART appears in the system contents table.
4. In the **Name** column, right-click the JTAG UART and click **Rename**.
5. Type `jtag_uart` and press Enter.
6. Connect the `clk` port of the **clk_0** clock source to the `clk` port of the JTAG UART.
7. Connect the `clk_reset` port of the `clk_0` clock source to the `reset` port of the JTAG UART.
8. Connect the `data_master` port of the Nios II processor to the `avalan_jtag_slave` port of the JTAG UART.

Please note that the `instruction_master` port of the Nios II processor does not connect to the JTAG UART because the JTAG UART is not a memory device and cannot send instructions to the Nios II processor.

Add the Interval Timer

Most control systems use a timer component to enable precise calculation of time. To provide a periodic system clock tick, the Nios II HAL requires a timer. Perform the following steps to add the timer:

1. On the **IP Catalog** tab, expand **Processors and Peripherals -> Peripherals** and then click **Interval Timer Intel FPGA IP**.
2. Click **Add**. The Interval Timer parameter editor appears.
3. In the **Presets** tab (on the right), select **Full-featured** and press **Apply**. Please make a note of the Timeout period setting.
4. Click **Finish**. You return to the Platform Designer **System Contents** tab, and an instance of the interval timer appears in the system contents table.
5. In the **Name** column, right-click the interval timer and click **Rename**.
6. Type `sys_clk_timer` and press Enter.
7. Connect the `clk` port of the **clk_0** clock source to the `clk` port of the interval timer.
8. Connect the `clk_reset` port of the **clk_0** clock source to the `reset` port of the interval timer.
9. Connect the `data_master` port of the Nios II processor to the `s1` port of the interval timer.

Add the System ID Peripheral

The system ID peripheral safeguards against accidentally downloading software compiled for a different Nios II system. If the system includes the system ID peripheral, the Nios II SBT for Eclipse can prevent you from downloading programs compiled for a different system.

Perform the following steps to add the system ID peripheral:

1. On the **IP Catalog** tab, expand **Basic Functions -> Simulation; Debug and Verification -> Debug and Performance**, and then click **System ID Peripheral Intel FPGA IP**.
2. Click **Add**. The System ID Peripheral parameter editor appears.
3. Click **Finish**. You return to the Platform Designer **System Contents** tab, and an instance of the system ID peripheral appears in the system contents table.
4. In the **Name** column, right-click the system ID peripheral and click **Rename**.
5. Type `sysid` and press Enter.
6. Connect the `clk` port of the **clk_0** clock source to the `clk` port of the system ID peripheral.
7. Connect the `clk_reset` port of the **clk_0** clock source to the `reset` port of the system ID peripheral.
8. Connect the `data_master` port of the Nios II processor to the `control_slave` port of the system ID peripheral.

Add the PIO

PIO signals provide an easy method for Nios II processor systems to receive input stimuli and drive output signals. Complex control applications might use hundreds of PIO signals which the Nios II processor can monitor. This design example uses eight PIO signals to drive LEDs on the board.

Perform the following steps to add the PIO.

1. On the **IP Catalog** tab, expand **Processors and Peripherals -> Peripherals**, and then click **PIO (Parallel I/O) Intel FPGA IP**.
2. Click **Add**. The PIO (Parallel I/O) parameter editor appears.

3. Do not change the default settings. Click Finish and return to the Platform Designer **System Contents** tab. In the name column right-click the PIO and click rename. Give the name **led_pio** and press enter.
4. Connect the **clk** port to **clk_0** clock source, connect the **reset** port to **clk_reset** of **clk_0**, and connect the **data_master** port of the NIOS II processor to the **s1** port of PIO
5. In the external connection row, click **Double-click to export** (grayed out) in the **Export** column to export the PIO ports.

Specify Base Addresses and Interrupt Request Priorities

At this point, you have added all the necessary hardware components to the system. Now you must specify how the components interact to form a system. In this section, you assign base addresses for each slave component, and assign interrupt request (IRQ) priorities for the JTAG UART and the interval timer. Platform Designer provides the **Assign Base Addresses** command which makes assigning component base addresses easy. For many systems, including this design example, **Assign Base Addresses** is adequate. However, you can adjust the base addresses to suit your needs. Below are some guidelines for assigning base addresses:

- Nios II processor cores can address a 31-bit address span. You must assign base address between 0x00000000 and 0x7FFFFFFF.
- Nios II programs use symbolic constants to refer to addresses. Do not worry about choosing address values that are easy to remember.
- Address values that differentiate components with only a one-bit address difference produce more efficient hardware. Do not worry about compacting all base addresses into the smallest possible address range, because this can create less efficient hardware.
- Platform Designer does not attempt to align separate memory components in a contiguous memory range. For example, if you want an on-chip RAM and an off-chip RAM to be addressable as one contiguous memory range, you must explicitly assign base addresses.

Platform Designer also provides an **Assign Interrupt Numbers** command which connects IRQ signals to produce valid hardware results. However, assigning IRQs effectively requires an understanding of how software responds to them. Because Platform Designer does not know the software behavior, Platform Designer cannot make educated guesses about the best IRQ assignment.

The Nios II HAL interprets low IRQ values as higher priority. The timer component must have the highest IRQ priority to maintain the accuracy of the system clock tick.

To assign appropriate base addresses and IRQs, perform the following steps:

1. On the System tab on the toolbar, click **Assign Base Addresses** to make Platform Designer assign functional base addresses to each component in the system. Values in the **Base** and **End** columns might change, reflecting the addresses that Platform Designer reassigned.
2. In the **IRQ** column, connect the Nios II processor to the JTAG UART and interval timer.
3. Click the IRQ value for the **jtag_uart** component to select it.
4. Type 16 and press Enter to assign a new IRQ value.
5. Click the IRQ value for the **sys_clk_timer** component to select it.
6. Type 1 and press Enter to assign a new IRQ value.

Generate the System

You are now ready to generate the system. Perform the following steps:

1. Click the **Generate HDL** in the bottom right corner.
2. Select **None** in the **Create simulation model** list. Because this tutorial does not cover the hardware simulation flow, you can select these settings to shorten generation time.
3. Under **Output Directory** for **Path** select an appropriate path. **Click Generate**. The **Save changes?** dialog box appears, prompting you to save your design.
4. Type `first_nios2_system` in the **File name** box and click **Save**. The **Generate** dialog box appears and system generation process begins. The generation process can take several minutes. Output messages appear as generation progresses. When generation completes, the final "Info: Finished: Create HDL design files for synthesis" message appears.
5. Click **Close** to close the dialog box.
6. On the File menu, click **Exit** to close Platform Designer and return to the Quartus Prime Lite software. Press **OK** on the pop up box.
7. In Quartus, select **Add/Remove Files in Project** from the **Project** tab in the toolbar. Browse for the `first_nios2_system.qsys` file and once it is added, click Apply and OK. This will add the system to the Quartus project.
8. In the **Add/Remove Files in Project** window, select the libraries tab on the left. Under **Project Libraries**, select the top-level folder for the project (`system_template_de1_soc`) which contains the `first_nios2_system.qys` file. Add this folder and click Apply and OK.

Congratulations! You have finished creating the Nios II processor system. You are ready to integrate the system into the Quartus II hardware project and use the Nios II SBT for Eclipse to develop software.

Integrate the Platform Designer System into the Quartus II Project

To instantiate the system module in the .bdf (i.e. your schematic capture file), perform the following steps (by closing Platform Designer, you should have gone back to Quartus on your `hello_world` system):

1. Double-click in the empty space to the right of the input and output wires. The Symbol dialog box appears.
2. Under Libraries, expand Project.
3. Click `first_nios2_system`. The Symbol dialog box displays the `first_nios2_system` symbol.
4. Click OK. You return to the .bdf schematic. The `first_nios2_system` symbol tracks with your mouse pointer.
5. Position the symbol so the pins on the symbol align with the wires on the schematic.
6. Click to anchor the symbol in place.
 - a) Make the connections:
 - b) connect `clk_clk` to `iCLK_50`
 - c) connect `reset_reset_n` to Vcc (Symbol dialog box -> `/home/e2/intelFPGA_lite/20.1/quartus/libraries -> primitives -> other`)
 - d) connect the leds.
 - e) leave the DRAM pins unconnected.
7. To save the completed .bdf, click Save on the File menu.

Compile the Quartus II Project and Verify Timing

At this point you are ready to compile the Quartus II project and verify that the resulting design meets timing requirements. You must compile the hardware design to create a .sof that you can download to the board. After the compilation completes, you must analyze the timing performance of the FPGA design to verify that the design will work in hardware. In this case, the sdc file (i.e. the Synopsys Design Constraints File) has already been included to your project (by us), so you do not have to worry about this. You just need to know that the target clock frequency for the design is 50MHz.

To compile the Quartus II project, perform the following steps:

1. On the Processing menu, click **Start Compilation**. The Tasks window and percentage and time counters in the lower-right corner display progress. The compilation process can take several minutes. When compilation completes, a dialog box displays the message "Full Compilation was successful."
2. Click **OK**.
3. Expand the **Timing Analyzer** category in the compilation report.
4. Click **Multicorner Timing Analysis Summary**.
5. Verify that the **Worst-case Slack** values are positive numbers for **Setup, Hold, Recovery, and Removal**. If any of these values are negative, the design might not operate properly in hardware. To meet timing, adjust Quartus assignments to optimize fitting, or reduce the oscillator frequency driving the FPGA. (You should not have to worry for any of the above). You can ignore errors from the unconstrained paths report.

Congratulations! You have finished integrating the Nios II system into the Quartus II project. You are ready to download the .sof to the target board.

Download the Hardware Design to the Target FPGA

In this section you download the .sof to the target board. Perform the following steps:

1. Connect the board to the host computer with the download cable, and apply power to the board.
2. In the VirtualBox toolbar go to Devices->USB and ensure Altera DE_SoC [0139] is checked. If only Altera [0001] is displayed, check this for now, and once you are looking for hardware, check Devices->USB again and Altera DE_SoC [0139] should now be available.
3. On the Tools menu in the Quartus Prime Lite software, click **Programmer**. The Quartus Prime Lite Programmer appears and automatically displays the appropriate configuration file (**hello_world.sof**)
4. Click **Hardware Setup** in the upper left corner of the Quartus Programmer to verify your download cable settings. The **Hardware Setup** dialog box appears.
5. Select the appropriate download cable in the **Currently selected hardware** list. If the appropriate download cable does not appear in the list, you must first install drivers for the cable.
6. Click **Close**.
7. Click **Auto Detect**. A window will pop up and you should select the relevant serial code for the device.
8. Remove the <none> file for the 5CSEMA device and leave both the **hello_world_time_limited.sof** file and the **SOCVHPS** device. If this removed the **hellow_world_time_limited.sof** file, just add it back in using the **Add File** button.
9. In the **hello_world_time_limited.sof** row, turn on **Program/Configure**.

10. Click **Start**. The **Progress** meter sweeps to 100% as the Quartus II software configures the FPGA.

At this point, the Nios II system is configured and running in the FPGA, but it does not yet have a program in memory to execute.

Develop Software Using the Nios II SBT for Eclipse

In this section, you start the Nios II SBT for Eclipse and compile a simple C language program. This section presents only the most basic software development steps to demonstrate software running on the hardware system you created in previous sections.

Create a New Nios II Application and BSP from Template

In this section you create new Nios II C/C++ application and BSP projects. Perform the following steps:

1. Start the Nios II SBT for Eclipse. If you are running on the provided VM, open a Terminal window and type `eclipse`. On Windows computers, click **Start**, point to **Programs, Altera, Nios II EDS <version>**, and then click **Nios II <version> Software Build Tools for Eclipse**. On Linux computers (and not running the provided VM), run the executable file `<Nios II EDS install path>/bin/eclipse-nios2`.
2. If the **Workspace Launcher** dialog box appears, click **OK** to accept the default workspace location or choose one if you prefer a non-default location.
3. On the Window menu, point to **Perspective->Open Perspective**, and then either click **Nios II**, or click **Other** and then click **Nios II** to ensure you are using the Nios II perspective.
4. On the File menu, point to **New**, and then click **Nios II Application and BSP from Template**. The Nios II Application and BSP from Template wizard appears.
5. Under **Target hardware information**, next to **SOPC Information File name**, browse to locate the *<design files directory>*.
6. Select **first_nios2_system.sopcinfo** and click **Open**. You return to the Nios II Application and BSP from Template wizard showing current information for the **SOPC Information File name** and **CPU name** fields.
7. In the **Project name** box, type `hello_world`.
8. In the **Templates** list, select **Hello World**.
9. Click **Finish**.

The Nios II SBT for Eclipse creates and displays the following new projects in the Project Explorer view, typically on the left side of the window:

■ **hello_world**—Your C/C++ application project

■ **hello_world_bsp**—A board support package that encapsulates the details of the Nios II system hardware

Compile the Project

In this section you compile the project to produce an executable software image. For the tutorial design example, you must first adjust the project settings to minimize the memory footprint of the software, because your Nios II hardware system contains only 20 KB of memory.

Perform the following steps:

1. In the Project Explorer view, right-click **hello_world_bsp** and click **Properties**. The **Properties for hello_world_bsp** dialog box appears.

2. Click the **Nios II BSP Properties** page. The **Nios II BSP Properties** page contains basic software build settings (it may take a while).
3. Adjust the following settings to reduce the size of the compiled executable:
 - a. Turn on **Reduced device drivers**.
 - b. Turn off **Support C++**.
 - c. Turn off **GPROF support**.
 - d. Turn on **Small C library**.
 - e. Turn off **ModelSim only, no hardware support**.
4. Click **OK** (Do not click **Apply**). The BSP regenerates, the **Properties** dialog box closes, and you return to the Nios II SBT for Eclipse.
5. Right click on **hello_world_bsp** then go to **NIOS II->Generate BSP**
6. In the Project Explorer view, right-click the **hello_world** project and click **Build Project**.

The **Build Project** dialog box appears, and the Nios II SBT for Eclipse begins compiling the project. When compilation completes, a "hello_world build complete" message appears in the Console view.

The console provides info on the size of your program (hello_world.elf), which is the total size of the code and the initialised data, plus info on how much memory has been left free for stack and heap.

Run the Program on Target Hardware

In this section you download the program to target hardware and run it. If you are using a windows machine, you should be able to right click on your project and select **Run as -> Run Nios II Hardware**

If you are using Linux or the provided VM then to download the software executable to the target board, perform the following steps:

1. If this is the first time running a program on the NIOSII, open a new terminal window and copy the provided bashrc file and save it at **~/bashrc**.
2. Open a new terminal and run the command **nios2_shell** followed by **nios2-terminal**. This opens the nios2 terminal of the output of the FPGA. The output of running the program will appear in this terminal window.
3. Open a new terminal window, run **nios2_shell**, and then run **nios2-download -g <path to quartus project>/software/hello_world/hello_world.elf**. This will result in an output appearing on the other terminal window. If you create a new project in eclipse, it will always appear at **<path to quartus project>/software/** and contain a .elf file which is what runs on the NIOSII processor.
4. If the **Run Configurations** dialog box appears, verify that **Project name** and **ELF file name** contain relevant data, then click **Run**.

In all configurations, you may encounter problems launching your application on the FPGA resulting in:

[Target Connection]: Connected system ID hash not found on target at expected base address.

To mitigate this, ensure the most recently compiled .sof file is programmed to your FPGA which should resolve any timestamp and system ID differences. To see the system ID and timestamp values, click the System ID Properties button. If the system ID and/or timestamp report "Not Found", power cycle the board and reprogram. If this does not resolve the "Not Found" issue, restart eclipse and Quartus and recompile and

reprogram the Quartus design. You are advised to run both *binary_counter* and *hello_world* examples to familiarise yourselves with the system.

If you get the message “Downloading ELF Process failed”, then this may be for a number of reasons. Unfortunately, the tools (even though they are commercial tools, have bugs). Possible steps to solve the problem:

1. Make sure that the Programmer window from Quartus is closed.
 2. Your Quartus design may be wrong. Check the connections carefully and also check whether you have connected the reset input to Vcc.
-
3. Restart the board and Eclipse. Try to resynthesize the design and download again to the board.
 4. If the launch of the program gets stuck at “Launching: Flush any cached byte stream chars from input stream”, restart Eclipse and try again.

If you encounter

nios2-terminal: Unable to connect to JTAG UART because another application

nios2-terminal: is using it (or is using something else which clashes). Please close

nios2-terminal: the other application and try again.

Ensure that there are no other connections to the nios2 terminal, close eclipse, power cycle the FPGA, redownload the .sof file using programmer, and then try again.

When the target hardware starts running the program, the Nios II Console view displays character I/O output.

2. To disconnect from the FPGA, in the terminal hosting the NIOSII terminal, just press ctrl+C and it will disconnect from the FPGA. You can edit the **hello_world.c** program in the Nios II SBT for Eclipse text editor and repeat these two steps to witness your changes executing on the target board. If you rerun the program, buffered characters from the previous run session might display in the Console view before the program begins executing.

The final generated system has an Arithmetic Logic Unit (ALU) that supports fixed-point arithmetic, where all the arithmetic operators are implemented using LUTs. The FPGA on the DE1-SOC board is the Cyclone V SE5CSEMA5F31C6N FPGA. Make sure you keep track of your NIOS settings throughout the coursework.

In summary, you have designed a system in Quartus, and then moved on to program the system through Eclipse. If you make any changes in the hardware, you need to regenerate the BSP file. Otherwise, you can create new SW programs targeting the same HW without going back to Quartus.

Further details on the use of command line instructions (cli) can be found in the “nios2_cli.pdf”.



Record the FPGA resources used by your baseline system (i.e. Total logic elements, Total memory bits, Embedded Multiplier 18-bit elements, and Total PLLs).

Task 2: Computing a simple function

Now that you have your system running on the FPGA, you can start using it to evaluate mathematical expressions.

From here on out, it is recommended to create backups of your project. Copying the `system_template_de1_soc` directory is enough to create a backup. Be sure that if working in a copied directory to update any file paths that may have changed.



The first task is to write a function that takes as input a vector x and its length N , and returns y where $y = \sum_{i=1}^N x_i + x_i^2$. The elements of the input vector are single-precision (floats) and are in the range between 0 and 255.

Starting from the **Hello World** template, modify the `hello_world.c` file as follows:

```
#include <stdlib.h>
#include <sys/alt_stdio.h>
#include <sys/alt_alarm.h>
#include <sys/times.h>
#include <alt_types.h>
#include <system.h>
#include <stdio.h>
#include <unistd.h>

// Test case 1
// #define step 5
// #define N 52

// Test case 2
#define step 1/8.0
#define N 2041

// Test case 3
// #define step 1/1024.0
// #define N 261121

// Generates the vector x and stores it in the memory
void generateVector(float x[N])
{
    int i;
    x[0] = 0;
    for (i=1; i<N; i++)
        x[i] = x[i-1] + step;
}

float sumVector(float x[], int M)
{
    // YOUR CODE GOES HERE
}

int main()
{
    printf("Task 2!\n");

    // Define input vector
    float x[N];

    // Returned result
    float y;

    generateVector(x);

    // The following is used for timing
    char buf[50];
    clock_t exec_t1, exec_t2;

    exec_t1 = times(NULL); // get system time before starting the process

    // The code that you want to time goes here
    y = sumVector(x, N);

    // till here
    exec_t2 = times(NULL); // get system time after finishing the process

    int i;
    for (i=0; i<10; i++)
        y = y/2.0;

    return 0;
}
```

Complete the code in `sumVector()` function and compute the results for the three test cases presented in the beginning of this coursework. Increase the onchip memory as much as you can to accommodate the maximum problem size.



NOTE: You should assume that the vector x is stored in the memory prior calling your function. Not all three test cases need to be in the memory of the system at the same time. This assumption applies to the whole project.

More detailed information about programming NIOS II in EDS is offered here:



http://www.altera.com/literature/hb/nios2/n2sw_nii52017.pdf



To debug your application running on NIOS II use  instead of . Make use of the perspectives to switch between NIOS II project and debug (**Window → Open perspective**). You're encouraged to make use of the available debug tools, e.g. watch and breakpoint, to facilitate the development of the software.



Good to know:

The `printf()` command in NIOS by default does not support floating point printing on the screen in order to reduce the size of the generated code. As you have available only the on-chip memory to store your program, the result can be shown on the screen by printing an approximate output of the calculated result. Thus, if **result** is your floating point result, you can divide it by 1024 and provide to the output the integer part only as follows:

```
For (int i=0; i<<10; i++)

    resultf = resultf/2.0;

printf("Result: %d \n", (int) result);
```



Good to know:

Since we are interested in accelerating a certain computational process we need to be able to know how long it takes to execute that process. The time required to complete any statement/block of statements can be determined using the following statements in C code:

```
char buf[40];

clock_t exec_t1, exec_t2;

exec_t1 = times(NULL); // get system time before starting the process
*** your C statement(s) here ***
exec_t2 = times(NULL); // get system time after finishing the process

gcvt((exec_t2 - exec_t1), 10, buf);
alt_putstr(" proc time = ");    alt_putstr(buf);    alt_putstr(" ticks \n");
```

which requires the following includes:

```
#include <stdlib.h>
#include <sys/alt_stdio.h>
#include <sys/alt_alarm.h>
#include <sys/times.h>
#include <alt_types.h>
#include <system.h>
#include <stdio.h>
#include <unistd.h>
```

It also requires the Interval Time block to be in your system and running in the Hardware Abstraction Layer (HAL). Please refer to the tutorial for more details about this. Please note that the above code may require extra memory that your system may not have.



Good to know:

See command `nios2-elf-size` to get the size of your application. Alternatively, you can look at the `.map` file, or at the output of the building project process.

Read the reference about application profiling at the end of this hand-out.

Provide answers to the following questions:

How many resources does your system occupy on the FPGA?

Is your system able to evaluate the given function for all test cases? If not, why?

What is the size of your NIOS II application? How does it correspond to different vector sizes and what is the maximum memory required for each of the test cases?

Compare your results to Python/Matlab implementation which uses double precision. Do the results agree? If not, why not? Note that we are interested in the result that we calculate and not on the approximated result that we print due to the current memory limitations.

What is the time required to evaluate the `sumVector()` function for each test case in seconds? If you require more accuracy in the calculation of the time required by `sumVector()` function, you can call the function a number of times and get the average time spend in the function.

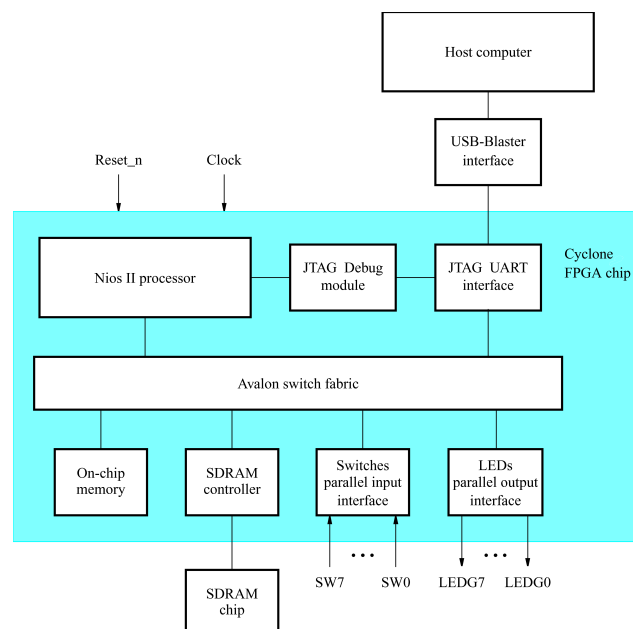
In designing HW systems, there is a relationship between the HW resources used by your system and the performance that you get out of it. If we assume that the accuracy is fixed and is not affected by the HW resource allocation, then the performance in your case is the latency of the function `sumVector()`. The best design is the one that provides the least latency for the least possible resources. Where is your current design in that space?

Task 3: Storing the Program and Data on External Memories

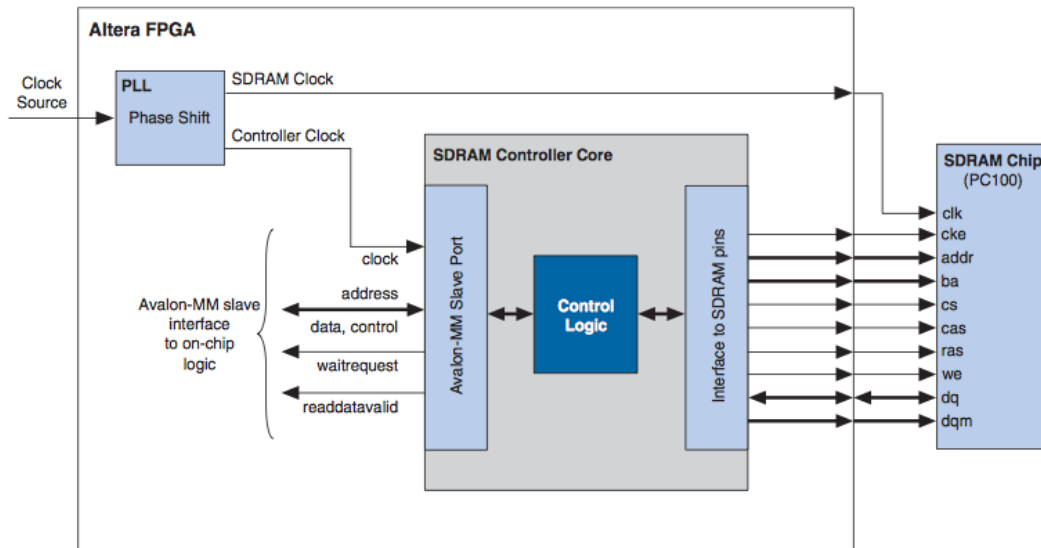
The system that you created has its application stored on on-chip memory. Despite the fact being the fastest one available on an FPGA, it is the smallest and the most expensive one available in your system. On the DE0 boards there are different types of memories, including SDRAM memory. The main benefit of using SDRAM is that it has much more capacity and it has lower cost. That's why it is often used in real-life applications. The main drawback of using these memories is their interface, which requires a controller, and a consequent penalty on the system's complexity and performance, when compared to on-chip memory.

In this task, we will assess how the SDRAM memory allows to address problems with large memory requirements but also how its performance impacts the overall performance of the system.

The Altera DE1-SOC board contains an SDRAM chip that can store 64 Mbytes of data. The SDRAM chip requires careful timing control. To provide access to the SDRAM chip, Platform Designer implements an SDRAM Controller circuit. This circuit generates the signals needed to deal with the SDRAM chip. The figure below shows the resulting system by including the SDRAM controller (Please note that the "Switches parallel input interface" block is missing from your current system). You can notice that all the connections to on-chip memory and SDRAM controller are through the Avalon switch fabric.



The signals needed to communicate with this chip are shown in the figure below. All of the signals, except the clock, can be provided by the SDRAM Controller that can be generated by using Platform Designer. The clock signal is provided separately. It has to meet the clock-skew requirements (it will be explained in the lectures). Note that some signals are active low, which is denoted by the suffix N. Due to clock skewness a PLL is needed to generate a shifted version of the clock that drives the SDRAM.



In order to include the SDRAM controller in your existing system, open your current design in Platform Designer and in the IP Catalog select Memory Interfaces and Controllers > SDRAM > SDRAM Controller Intel FPGA IP and click Add in the new window.

Set the Data Width parameter to 16 bits and leave the default values for the rest. The rest of the parameters of the SDRAM controller for the DE1-SOC are given below.

Memory Profile:
 bits: 16; chip select: 1; banks: 4; row: 12; col: 8;
 Timing:
 cas: 3; init: 2; refresh: 15.625; delay: 100; t_rfc: 70; t_rp: 20; t_rcd: 20;
 t_ac: 5.5; t_wr: 14.0;

Click Finish. Now, in your final system, there will be an sdrum module added to the design. Rename the module to **sdrum**, and make the clk and reset connection as in the other modules. Connect the s1 signal to both cpu.data_master and cpu.instruction_master. Export the wire signal by double clicking on the export column.

So far, we have instantiated an SDRAM controller in the design, and have made the necessary connections to the rest of the design. We have also told to the tool to export the wire signal, which will be connected to the SDRAM memory directly.

The next stage is to integrate this memory in the memory address space of the system and inform the CPU where our reset_vector and exception_vector addresses are. Deselect the check box for onchip memory as this is now no longer necessary to keep active.

Select the command System > Assign Base Addresses. Observe that the SOPC Builder assigned the base address 0x00800000 to the SDRAM. To make use of the SDRAM, we need to configure the reset vector and exception vector of the Nios II processor. Right-click on the cpu and then select Edit. Select sdrum to be the memory device for both reset vector and exception vector. Click Finish to return to the main window regenerate the system.

Close Platform Designer and go back to Quartus. Right click on your system and select Update System or Block. This should now reflect the extra wire connections from the SDRAM controller that we selected to export. Connect these to the relevant DRAM output pins already existing in your design.

Using the Clock Signals IP Core

The clock skew depends on physical characteristics of the DE1-SOC board. For proper operation of the SDRAM chip, it is necessary that its clock signal, DRAM_CLK, leads the Nios II system clock, iCLK_50, by 3 nanoseconds.

This can be accomplished by using a phase-locked loop (PLL) circuit which can be manually created using the MegaWizard plug-in.

To add the PLL IP core, in the IP Catalog tab search for the PLL Intel FPGA IP and click the Add button. Select either Verilog or VHDL (either is fine) and then name the unit pll.v or pll.vhdl respectively. The Megawizard plugin will open.

There are many parameters that you can set in the block, but what you need is to provide an input clock of 50MHz and provide two output clocks at the same frequency but one of them with some phase difference enough to compensate for the clock skew.

Provide the 50MHz reference clock frequency. In the Output Clocks section, set Number of Clocks to the required value. outclk0 clock should be kept the same as the input clock (i.e. same freq and zero phase diff). outclk1 should be set to have a 50MHz freq, but the requested phase diff to be -2.55ns (You may have to fine-tune the PLL time shift to a different value for your particular DE1-SOC board, but the value should be between -2.62ns and -2.50ns (a phase shift of about -46 degrees for 50MHz clock). No other clock is needed, so click on Finish. (There is no need to have a reset and lock signal in your PLL). One indicator of such problem is the absence of output in the console terminal, when you run the application or the fact that ELF failed to download/verify.



Place the new block in the design and make the necessary connections to the clocks. Which clock output from the PLL should drive which module?

You also can place the PLL inside Platform Designer. The only difference is if you have to change the parameters of the PLL, you will have to re-generate your Platform Designer system, whereas if you have the PLL in your top design, you'll only need to re-synthesize the design.



Please note that SDRAM is very sensitive to clock variations. It is recommended that you use an external PLL in your design.



You can read more about this here: http://www.altera.com/literature/ug/ug_embedded_ip.pdf

To assess the correct functioning of your system with SDRAM, change your application so that it prints a different statement in the console output. Below there's the example of the **count_binary** template application. Please note that you can use the whole support for the C++ language as you have enough memory to store your programs (i.e. printf to print the floating point number).

```

*****
* Hello from Nios II!
* running on SDRAM!
* Counting from 00 to ff
*****
00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0a, 0b, 0c, 0d, 0e, 0f, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1a, 1b,
1c, 1d, 1e, 1f, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2a, 2b, 2c, 2d, 2e, 2f, 30, 31, 32, 33, 34, 35, 36, 37,
38, 39, 3a, 3b, 3c, 3d, 3e, 3f, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4a, 4b, 4c, 4d, 4e, 4f, 50, 51, 52, 53,
54, 55, 56, 57, 58, 59, 5a, 5b, 5c, 5d, 5e, 5f, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 6a, 6b, 6c, 6d, 6e, 6f,
70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 7a, 7b, 7c, 7d, 7e, 7f, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 8a, 8b,
8c, 8d, 8e, 8f, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 9a, 9b, 9c, 9d, 9e, 9f, a0, a1, a2, a3, a4, a5, a6, a7,
a8, a9, aa, ab, ac, ad, ae, af, b0, b1, b2, b3, b4, b5, b6, b7, b8, b9, ba, bb, bc, bd, be, bf, c0, c1, c2, c3,
c4, c5, c6, c7, c8, c9, ca, cb, cc, cd, ce, cf, d0, d1, d2, d3, d4, d5, d6, d7, d8, d9, da, db, dc, dd, de, df,
e0, e1, e2, e3, e4, e5, e6, e7, e8, e9, ea, eb, ec, ed, ee, ef, f0, f1, f2, f3, f4, f5, f6, f7, f8, f9, fa, fb,
fc, fd, fe, ff,
Waiting.....

```

As you the memory storage is not a limit anymore for using the extended C library, go to the **Nios II BSP Properties** page and adjust the settings to have extended support (i.e. do not use the C reduced library, ...). Now you should be able to print on the screen floating point numbers directly with printf. Make this change

in your code. The memory footprint of your programme and the overall execution latency will increase slightly, but it will be easier to write software.



Evaluate the performance of your system using the same test cases as in the introduction of this hand-out and discuss the obtained results. Answer the following questions:

How long does it take to complete the evaluation of the function for each of the test cases?

What is the size of your NIOS II application for the different vector sizes?

How many resources does the final system occupy on the FPGA?

Investigate the impact of increasing the cache memory size (for both Data and Instruction caches) of the NIOS processor to the required resources and the achieved latency of the system. Investigate configurations for 2KB, 4KB and 8KB for each type of memory (no need to do the combinations). What do you observe?

Focus on the main loop of your code and disassemble ELF file using the `nios2-elf-objdump` command. This will produce a disassembly of the `.text` section of your code like the example below:

```
prog.elf:  file format elf32-littlenios2
```

Disassembly of section `.text`:

01000000 <main>:

```
1000000: 02c04034  movhi r11,256
1000004: 5ac01804  addi r11,r11,96
1000008: 5a400037  ldwio r9,0(r11)
100000c: 02c04034  movhi r11,256
1000010: 5ac01904  addi r11,r11,100
1000014: 5a800037  ldwio r10,0(r11)
1000018: 4a91883a  add r8,r9,r10
100001c: 02c04034  movhi r11,256
1000020: 5ac01704  addi r11,r11,92
1000024: 5a000035  stwio r8,0(r11)
```

The format of each line is: “address in memory”, “binary encoding of the instruction”, “textual representation of the instruction”. Using this information you can calculate the size of your mail loop. How this can explain the behaviour that you see on the performance of the system when you change the I cache size?

Hints:

- If you experience problems running your application on the updated system, try to create a new Board Support Package (BSP) project and copy only the C source files from your previous project. **It is advised to create a new project with BSP.** Avoid using existent BSPs after updating your system.

- If you copy the folder of your previous project, pay attention to the paths on files: **create-this-bsp** and **settings.bsp**. They may not be relative to the new project folder!
- Stop the execution of your application before trying to re-program the FPGA, as you may lose connection to it.
- As you have now added off-chip memory to your system, you can use the traditional way to output information on the screen and make use of the available libraries.

Task 4: Evaluate a More Complex Mathematical Expression

By completing Task 3, you should have a good understanding on how an embedded digital system is constructed and how certain design decisions affect its performance. Your basic embedded system is based on the NIOS processor and has a large amount of memory (64MB). From now on, we will focus on the initial objective of the project, which was to evaluate the following function and design accelerators to improve the design's performance.

$$f(x) = \sum (0.5 * x + x^2 * \cos((x-128)/128))$$

As now your system includes access to enough memory, the math.h library can be utilised to help with the evaluation of the cosine function.



Make use of the math.h library and implement the new mathematical expression in software.

Run the application for all three test cases and report the performance of your design regarding: HW resources, latency to evaluate the function in seconds, and accuracy of the final result (compared to a MATLAB double precision implementation).

Note: For the final assessment, an extra test case will be used which generates N random floats to populate x based on a seed provided during the assessment. This will require the following function and #define to be present in your source code.

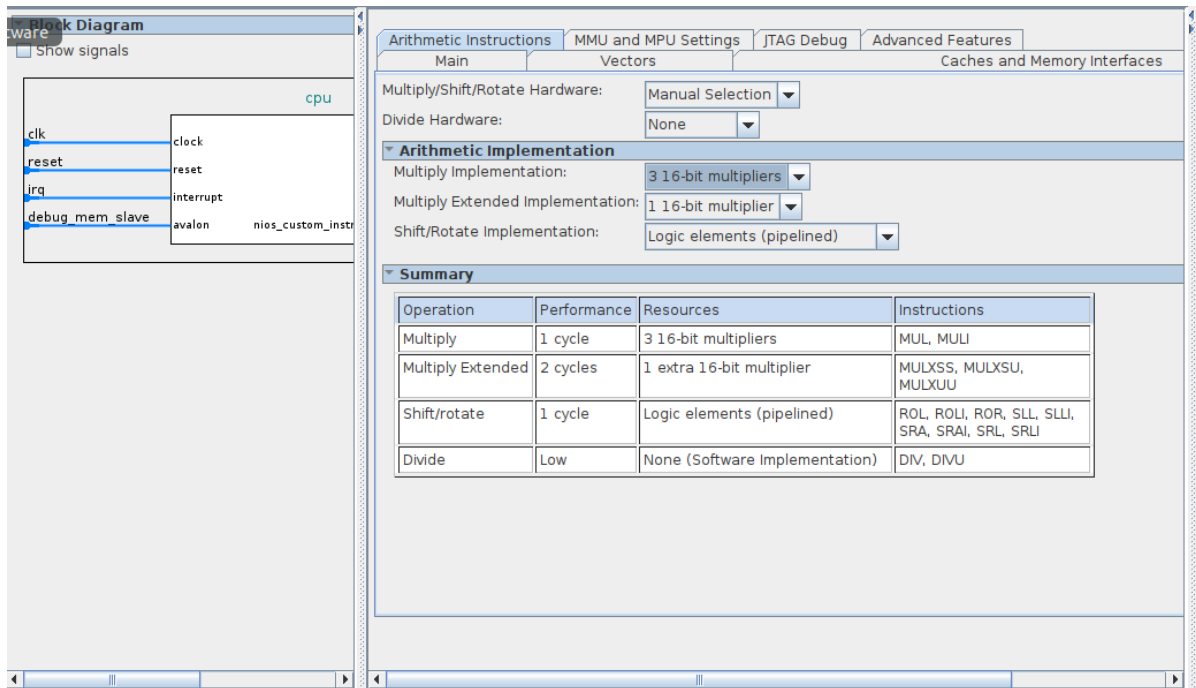
```
// Test Case 4
#define N 2323
#define RANDSEED 334

void generateRandomVector(float x[N])
{
    int i;
    srand(RANDSEED);
    for (i=0; i<N; i++)
    {
        x[i] = ((float) rand() / (float) RAND_MAX) * MAXVAL;
    }
}
```

Task 5: Add Multiplier Support

When you first created your NIOS II it had no multiplication support, which means that the floating-point multiplications have been emulated in software at the expense of fixed-point addition operations.

Now you're going to add hardware support for multiplication. NIOS II provides three possibilities: Logic Elements, 3 16-bit multipliers and 1 32-bit multiplier .



LUT-based multipliers are often used on FPGAs due to the flexibility of their word-length configuration, allowing faster multiplications at the expense of computing fewer bits than generic fixed word-length hard-multipliers. In the case of floating-point arithmetic the significand (also known as mantissa) has 23 bits, which is long enough to benefit from the performance of dedicated embedded multipliers.

So far you have been using floating-point arithmetic with non-floating-point units on your system. The software has been emulating these functions relying on a basic ALU implemented with generic LUTs (FPGA's basic logic elements). The FPGA that you are using, Cyclone V has dedicated hardware multiplier blocks that can be used to do fixed-point multiplications faster. Please note that you just add support for integer multiplication and the floating-point arithmetic has to be emulated again (signs, exponents, rounding and packing).



In order to improve the performance of your system, we are going to add HW support for fixed-point multiplications.

Go back to the Platform Designer, and edit the **cpu**. Select the **3 16-bit multipliers** from the drop-down menu in Platform Designer, update the system and compare the new performance results with the previous version of your system for all three test cases. Report the execution time (i.e. latency) of the function that computes $F(x)$, resource utilisation, code size, and error between the result of your system and the reference double precision Matlab/Python implementation for each test case.

Assuming that maximum performance is required by the application, which design choice should be selected? Justify your choice.

Task 6: Add Hardware Floating-Point Units

FLOATING-POINT (BACKGROUND)

In many applications there is a requirement to process data with large dynamic range and approximate data that takes values from the real number set. A possible way to represent the above numbers in a physical system is to use the "universally adopted" IEEE-754 floating-point standard.

The intention of the IEEE Standard for Binary Floating-Point Arithmetic, also known as IEEE-754, is to specify floating-point formats, arithmetic, conversions and exceptions. Floating-point numbers have three components: sign, significand and exponent, generically given by the following equation:

$$x = \pm \text{significand} \times 2^{\text{exponent}}$$

The sign is represented with one bit indicating whether the number is positive (0) or negative (1). The significand represents the fractional part of the number, in a fixed-point format. The exponent indicates the magnitude of the number, and has an embedded biased value. The number of bits of the significand determines its precision. In the IEEE standard, the significand is a real number in the interval [1; 2[. The integer component, value 1 is not included, so the significand contains only the fractional part of the floating-point value. The standard defines two formats: single precision (32-bit) and double precision (64-bit). In this coursework only the single precision format is considered. This format uses 8 bits to represent the exponent and 23 bits + 1 hidden bit for the significand, as shown in the figure below.

sign	exponent	significand
1 bit	8 bits	23 bits

Some values encoded using single precision floating-point representation:

Exponent	Significand	Value
0	0	± 0
0	Not 0	$\pm 2^{-126} \times (0.\text{significand})$ [denormal]
1-254	-	$\pm 2^{(\text{exponent} - 127)} \times (1.\text{significand})$
255	0	$\pm \infty$
255	Not 0	Not a Number

Example: $\pi = 3.1415926535897932384626433832795$

To be between 1 and 2 we need to divide it by two, which means the exponent needs to be $127 + 1$.

With 23 bits left we represent digits from the left to the right of 0.57079632679489661923132169163975

sign	exponent	significand
0	10000000	10010010000111111011011

So far there's no support for floating-point arithmetic in NIOS II. All your floating point operations are emulated through SW. Now you are going to add floating-point adder, subtraction and multiplier hardware, so that the elementary arithmetic operations used by the function can be performed faster, thereby reducing the execution time, in the expense of dedicating more FPGA resources.

In order to implement such functionality in dedicated hardware you'll need to design a hardware block that performs this functionality, attach it to a bus in the system so the processor can access it, and then create a custom instruction so you can access it from your software.

To design the hardware block in Quartus II you can use schematic capture², Verilog or VHDL. Before you attach your HW block to the NIOS system, you are advised to make a functional simulation of your hardware block to verify that it works correctly. You can do simulations using Modelsim³ or Active-HDL. After that, you will add it to the system using Platform Designer (**IP Catalog panel**→**Project**→**New Component**).



Good to know:

We can add Floating-Point Hardware in our system in two different ways. One way is to go through the Platform Designer, add **Floating-Point Hardware** from MegaWizard to your system, and then connect it to the **Custom Instruction Master** port on your processor. In this case the floating-point hardware will automatically be mapped to a custom instruction and all floating-point arithmetic in software will be using this hardware block. The main limitation of this approach is that you cannot pipeline the instruction, making inefficient use of resources for our application.

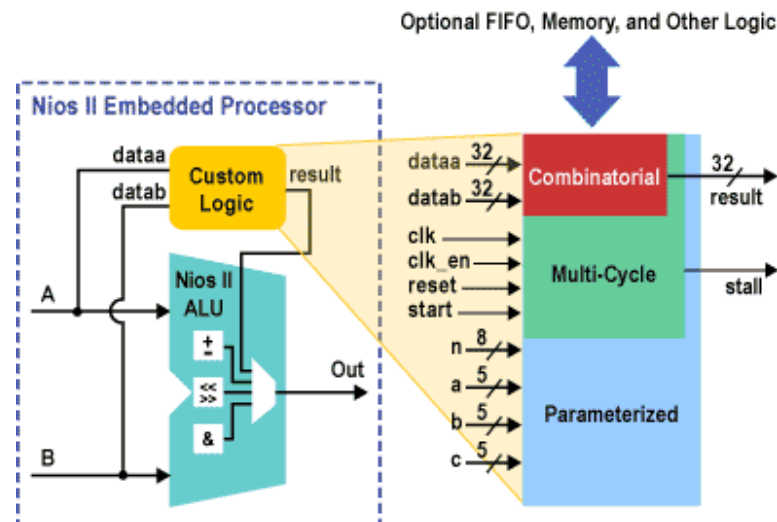
The focus is to learn how to design a new custom instruction in general in order to be able to design future acceleration units. **As such, the Floating-Point Hardware in Platform Designer is not permitted as a design choice in this project.** However we will use the Floating Point Ips provided in MegaWizard but treated them as general IPs that need to be interfaced with our CPU, and dealing with them as custom instructions.

NIOS II CUSTOM INSTRUCTIONS

NIOS II supports different types of custom instructions depending on the type of hardware block connected to it. The following diagram shows how the custom logic is interfaces with the rest of the system.

² Recommended (w/ help available), but you can use any alternative.

³ Again, recommended (w/ help available), but you can use another. There's a Modelsim tutorial at the end of this hand-out.



The supported custom instructions/logic blocks are:

- Combinatorial: single clock cycle logic block; In this case, your HW block should be able to produce a valid results within one clock cycle.
- Multi-cycle: fixed or variable number of clock cycles to complete execution;
- Extended: block capable of performing multiple operations (e.g. ALU); In this case, your block has an extra input that specifies the operation to be performed.
- Internal register file: logic blocks that access internal register files for I/O (e.g. Multiply-Accumulate unit);
- External interface: logic blocks that interface to logic outside of the Nios II processor's data-path.

A high level view of the steps that you need to follow in order to create your own custom instruction component is shown below:

- Do a block diagram / Verilog / VHDL with your circuit;
- If you're doing block diagram, generate Verilog from it;
- Simulate your block using Modelsim or one of the other tools. If it performs as intended move on, otherwise revise your circuit design;
- Add the new block to your system as a new component;
- Synthesise your system;
- Get FPGA resources, latency and throughput;
- Add the "software interface" for your new block.

Add custom instruction tutorial

In order to familiarise yourself with the process of adding a custom instruction to your existing system, the following section provides a tutorial on how to map a simple one-cycle fixed point multiplier to your system as a custom instruction. This tutorial should be followed in parallel with the [ug_nios2_cusotm_instruction.pdf](#)

document (http://www.altera.com/literature/ug/ug_nios2_custom_instruction.pdf) where more detailed information on the process is provided.

Firstly we need to identify the type of the custom instruction. As we need to implement a single one-cycle integer multiplier, the *Combinatorial* type is appropriate.

Type	Application	Hardware ports
Combinational	Single Clock cycle custom logic blocks	dataa[31:0] datab[31:0] result[31:0]

Details on the available types can be found in Table 1-1 of http://www.altera.com/literature/ug/ug_nios2_custom_instruction.pdf

Design the module

Create a new project in Quartus, and insert a new symbol from the IP Catalog tab. You should select the LPM_MULT (this is an integer multiplier). Configure your multiplier to take two 32 bit inputs. Select your multiplier to be unsigned and without any pipeline stages (no clock). Your final multiplier should produce a 32 bit output, which are the 32 LSBs from the LPM_MULT component. This will produce a verilog module.

The Megawizard plugin has been known to cause some performance issues. To circumvent this, please setup ssh on the device following this link: <https://linuxize.com/post/how-to-enable-ssh-on-ubuntu-18-04/>

Once the ssh has been setup, as sudo edit “/etc/ssh/sshd_config” and uncomment and edit the lines to produce:

X11Forwarding yes

X11UseLocalhost yes

Then access quartus by running

ssh -X localhost home/e2/intelFPGA_lite/20.1/quartus/bin/quartus.

The performance of quartus should be fixed now.

Verify its functionality

After having instantiated your IP code, add input and output ports and simulate it to verify its functionality. The simulation must be done through ModelSim. Please note that you have kept only part of the result (32 LSBs).

Modelsim is the application where you can run a simulation of your design before deploying into the FPGA, saving development time.

1. Download from blackboard the file testbench_1.v which contains a module tb.
2. Press **Assignments->Settings**, then go to **EDA Tool Settings**
3. For **Tool Type->Simulation** select **ModelSim-Altera** under **Tool Name**.
4. Then go to **EDA Tool Settings->Simulation** and set **Tool name** to **ModelSim Altera**.
5. Under **NativeLink settings**, select **Compile test bench:** and then press **Test Benches**
6. In the window that pops up, press **New**
7. Pick a name for test bench name, and write **tb** for the top level module in test bench.
8. For **File Name** navigate to the provided testbench_1.v (downloaded from blackboard), press **Add** then **OK** and then **OK** again and then **OK** again.
9. In an editor, open testbench_1.v and modify it following the provided comments in the file to work as your testbench.

10. Select **Project->Add/Remove Files in Project...** and add testbench_1.v and press **OK**
11. Run **Analysis and Synthesis** (there is no need to run place and route)
12. Select **Tools->Run Simulation Tool->RTL Simulation**. A ModelSim window will open, and select wave tab to see the waveform output.

The testbench_1.v file is a template that can be used to develop more complex testbenches for later designs. It works exactly like a Verilog file that can be used to specify inputs, outputs and clocks for the module being test. (<https://verilogguide.readthedocs.io/en/latest/verilog/testbench.html>)

Add the module to the existing system

Switch back to the project containing the NIOS II. Open your system in Platform Designer and click on *New Component* in the IP Catalog window. Provide the name of your component, and in the Files tab add the vhdI or Verilog files that you have created for your component (i.e. these are the top-level vhdI or Verilog file and the vhdI or Verilog file of the lpm_mult). Click Top Level Module and select the name of the top-level module of your custom instruction logic. To set up the custom instruction interfaces, follow these steps:

1. Click on the Signals & Interfaces tab.
2. Change the Type field for this interface to Custom Instruction Slave.
3. Ensure that a single interface remains. For the design example, maintain the interface name nios_custom_instruction_slave.
4. For Clock Cycles, you need to type 0 for a variable multicycle type custom instruction, and otherwise type the number of clock cycles your custom instruction logic requires. In our case we need to type 0, but this has already been picked up by the tool.
5. In the general case, for Clock Cycle Type, type Variable for a variable multicycle type custom instruction, Multicycle for a fixed multicycle type custom instruction, or Combinatorial for a combinational type custom instruction.
6. For Operands, type the number of operands for your custom instruction.
7. For each port, change the Signal Type to the appropriate signal for that port.

If your custom instruction logic requires additional interfaces, either to the Avalon-MM fabric or outside the Platform Designer system, you can specify the additional interfaces in the Interfaces tab. Our example does not require additional interfaces.

Click Finish and Save. In the Platform Designer IP Catalog Library, under Project, select your custom module and click add to add the new instruction to the Platform Designer system. In the Connections panel, connect the new component component's nios_custom_instruction_slave interface to the cpu component's custom_instruction_master interface.

Reassign the base addresses, generate the new NIOS system, return to Quartus, add the custom instruction's directory through the **Projects -> Add/Remove Files in Project**, and then recompile the whole design in Quartus.

Check whether the new design meets timing.

Accessing the Custom Instruction from Software

Adding a custom instruction to a Nios II processor results in a significant change to the Qsys system. In this section, you create and build a new software project using the Nios II software build flow, and run the software that accesses the custom instruction.

Create a new software project using the Hello World template for your system and name it *hello_world_custom_instr*. After the file generation has been finished, click on *hello_world_custom_instr_bsp* and open the *system.h* file. Verify that a custom instruction macro has been generated as below and copy these lines into the top of your C source file after the *#include* of *system.h* and rename the custom instructions for use in your program. This is done as any changes made to the custom instructions will be lost if you regenerate the BSP.

```
#define ALT_CI_MUL_0(A,B) __builtin_custom_inii(ALT_CI_MUL_0_N,(A),(B))

#define ALT_CI_MUL_0_N 0x0
```

The second line provides the opcode for your custom instruction, and you can verify that this is the opcode assigned to your instruction by Platform Designer. The first line describes the custom instruction (input arguments and return values) and the associated custom instruction built-in function (Section 3.2 of *ug_nios2_custom_instruction.pdf*).

Without making any changes to the template, build and run the application on the actual hardware to verify its functionality.

Change the code of *hello_world.c* file as follows and verify its functionality.

```
#include <system.h>
#include <stdio.h>

#define ALT_CI_CUSTOM_MUL_0_N 0x0
#define ALT_CI_CUSTOM_MUL_0(A,B)
__builtin_custom_inii(ALT_CI_CUSTOM_MUL_0_N,(A),(B))

int main()
{
    printf("Hello from Nios II!\n");

    int a, b, c, d;
    a = 2;
    b = 4;
    c = a*b;
    printf("Multiplication result: %d\n", c);

    d = ALT_CI_CUSTOM_MUL_0(a,b);
    printf("Multiplication result from custom instr: %d", d);

    return 0;
}
```

Please note that you need to include *the system.h* file in order to access the custom instruction.

These concludes the tutorial on how you can instantiate a new hardware block in your system and create a new custom instruction to allow the NIOS processor to access it. More detailed information can be found in:



http://www.altera.com/literature/ug/ug_nios2_custom_instruction.pdf

(Chapters 1, 2 and 4).



You can find more information on Intel's support on floating point IP cores and the necessary conversions on the following documents: http://www.altera.com/literature/ug/ug_altpf_mfug.pdf, <https://www.intel.com/content/www/us/en/programmable/documentation/cru1439932898327.html>, https://www.intel.com/content/www/us/en/programmable/quartushelp/17.0/hdl/mega/mega_list_mega_lp_m_d1353e88.htm

Add custom instruction to your system

Having gone through the previous section, you should be familiar with the process of adding custom instructions to a NIOS system. The evaluation of the target function involves heavy use of floating-point addition, subtraction and multiplication, which at the moment are emulated through SW. As the target is to accelerate the evaluation of the function, the aim of this section is to map this functionality to HW.



Implement the custom logic blocks for floating-point adder, subtracter and multiplier operations in order to support hardware acceleration of the above operations. Design the HW block, verify it, and then integrate it to the rest of the system. Make sure that you select a suitable

Which type of custom instruction did you choose (i.e. Combinatorial, Multi-cycle,...)? Justify your choice.

What is the FPGA resources allocated for the new block? What is the throughput and latency of the new HW block? How the latency of your HW block impacts the overall performance of the system?

Compare the new performance results with the best performance achieved from the previous version of your system for all three test cases. Report the execution time (i.e. latency) of the function that computes $F(x)$, resource utilisation, code size, and error between the result of your system and the reference double precision Matlab implementation for each test case.

In the case where you have pipelined your design, please comment on how well the pipeline is utilised? Justify your answers.



VERIFICATION: GENERATING A SYSTEM, SYNTHESISING AND TESTING IT (A.K.A. TRIAL-AND-ERROR) IS TIME CONSUMING. YOU SHOULD VERIFY YOUR DESIGN THROUGH SIMULATION BEFORE TRYING RUNNING IT ON THE FPGA. THIS IS HOW REAL-LIFE SYSTEMS ARE DESIGNED, AND YOU SHOULD FOLLOW THIS PRACTICE THROUGHOUT THE COURSEWORK.

Hints:

- Organize your hardware blocks in a subfolder named “./IP” in your project folder;
- Create a new block diagram file and place your floating-point units there along with the necessary control logic. Remember to use labels in your connections, this will help to identify them during simulation;
- Pay attention to the interface signals of your block. They’ll be different for different types of custom instructions;
- The floating-point arithmetic units are added to your block diagram via the **IP Catalog tab**
- Use MegaWizard to create your other blocks. Add them to your design, as Platform Designer will only add the top HDL file to your design. DO NOT add your top block of your design to the project, only the sub-blocks;
- If you’re not familiar with either Verilog or VHDL, do your design using block diagram and then convert it to Verilog using **File->Create/Update->Create HDL File From Current File**. While creating a new component in Platform Designer it will ask for a VHDL or Verilog file. Remember to create a new one, and update your component, every time you update the block diagram. Platform Designer will create a copy of your HDL file (top of your block) when you create the component to a different location. Updating your HDL file won’t update your block in the system. You have to manually copy it and replace it or regenerate the component;
- Keep in mind that Intel’s CRC example is different than your floating-point add/sub/mult. You can’t just follow the steps as they are in the guide; you need to think about what needs to be changed;


- After generating the BSP, verify that you have the macros for your custom instruction in the file **system.h**. Check if the arguments and return value of **__builtin_custom_n??** agree (see manual Section 3.2). If not, create a new macro in your source file. **DO NOT EDIT system.h!**
- Replace all floating-point arithmetic operands in your application with calls to your custom application. E.g. `(float)x = (float)a * (float)b;` → `x = cust_fp_mult(a, b);`.

**Debug:**

- In case you don't read the expected value from your custom instruction, place a constant at the output of your hardware unit and verify if that value is read by the instruction.
- Whenever you introduce changes in your design, use different constant inputs so you can verify that your design is being updated. Platform Designer stores a copy of your top HDL file in a different location than your `./ip` folder. It is a good idea to have the connections correct in that design before adding it to the Platform Designer.
- Use the simulation to adjust the correct number of clock cycles required to complete the operation.
- If you fail to have any output from your instruction at all, try to implement a simple one (combinatorial) to verify that you are calling the custom instruction correctly from your software. E.g. load a constant value from it, negate one of the outputs, OR/AND/XOR your inputs, etc.

Task 7: Add Dedicated Hardware Block to compute the inner part of the arithmetic expression

You've seen that you can improve the performance of your system by implementing some of the most computationally demanding operations in hardware. In the present scenario you're going to extend your previous implementation and map the whole arithmetic expression as a custom instruction in your system.

 Please note that Tasks 7 and 8 have to be completed as individual work, which should be described in Report 3.

 Add the following custom instruction to your system:

$$y = 0.5 * x + x^2 * \cos((x - 128) / 128) \quad [2]$$

by mapping all operators to hardware including the implementation of a CORDIC block to implement `cos(.)` instead of using the software implementation from `math.h`.

Specs for Student 1

The aim is to produce a system with **maximum throughput**. As such, you dedicated hardware block that computes [2] should be designed in such way that maximises its throughput. Please note that many design choices may lead to the same maximum throughput, but out of those we are interested in the with one the smallest resource footprint.

Specs for Student 2

The aim is to produce a system with **minimum latency**. As such, you dedicated hardware block that computes [2] should be designed in such way that minimises its latency. Please note that many design choices may lead to the same minimum latency, but out of those we are interested in the one with the smallest resource footprint.

Common

Design your CORDIC block for the computation of $\cos(x)$ by selecting the number of CORDIC stages and the wordlength of your fixed point numbers, such as the **mean error e** is in the range $[-0.5 \times 10^{-6}, 0.5 \times 10^{-6}]$ with confidence level of 95%, assuming an input x is under single precision format and follows a uniform distribution in the range $[-1, 1]$ (i.e. the possible range of input given our problem).

At this point, we will decouple the development of the custom instruction from the NIOS system you have built so far.

The aim is to design and build an IP that takes as in input a single-precision floating point number x , and computes y through (2) using single-precision number format, except for the `cos()` evaluation where fixed-point will be used.


You should design your block in Quartus, use Modelsim to verify its functionality and performance (number of cycles), and check whether it meets timing after place and route. In your work, you need to design a CORDIC block based on **fixed-point format**. Please note that you should target the initial clock frequency (50MHz). When you are happy with the performance of your module, then you will need to interface it with the NIOS system.

For verification reasons, you need to implement the above custom instruction in two steps:

Step 1

Design your CORDIC architecture in accordance to your specs. Check the accuracy that is achieved when compared to a double precision SW version (you can use Matlab for this test).

(Hint: you should use the Monte Carlo simulation technique to determine the mean square error of your design. In Matlab, you can use the *Fixed-point numeric object*, "fi", to represent the fixed-point variables.)

 Please note that a look-up table-based implementation is not allowed for the implementation of the `cos (.)` function, or the use of an existing IP block that performs this function.

Comment on the architecture of your CORDIC HW block. How many CORDIC stages does it have? How did you select the number of stages? How many bits do you use for the fixed-point representation in CORDIC? How do they impact the performance of the function evaluation (i.e. accuracy and latency) for the 3 test cases?

Step 2

In the second step, you need to implement the intended custom instruction (2), and integrate your CORDIC IP with the rest of the blocks. Describe how data is passed in your new HW block. Comment on its performance vs resource utilisation when it is integrated in your NIOS system.

Report the execution time (i.e. latency) of the function that computes $F(x)$, resource utilisation, and error between the result of your system and the reference double precision Matlab implementation for each test case. Do you get the performance that you were expecting from your system?



You can find more information on Altera's support on floating point IP cores and the necessary conversions on the following document: http://www.altera.com/literature/ug/ug_alftp_mfug.pdf

Task 8: Add Dedicated Hardware Block to compute the arithmetic expression

Throughout this coursework you have been accelerating part of your software by designing dedicated hardware blocks in the hardware that accelerate part of the required computations. (Hopefully) your application has been computing the targeted arithmetic function faster through all these hardware support.



The aim of this final task is to map the whole function in hardware and reduce the execution time as much as you can. This is an open-ended task that you are free to use any possible architecture.

Some design Hints:

- You need to add a floating-point adder to perform the overall sum in hardware. In this way you can speed up part of the computations.
- Think whether you have taken full use of the pipeline capabilities of your hardware blocks. How often you can push a new value of the x vector to your system? How can you increase its throughput? Do not forget that your NIOS processor blocks after the execution of a custom instruction and waits for the assertion of the done signal to retrieve the result and being able to move to the next instruction. State any assumptions that you may have in your implementation.

Comment on the architecture of your final system and on the control and data flow of your design. Describe how and what data is passed in your new HW block. Comment on its pipeline's utilisation.

Compare the new performance results with the best performance achieved from the previous version of your system for all three test cases. Report the execution time (i.e. latency) of the function that computes $F(x)$, resource utilisation, code size, and error between the result of your system and the reference double precision Matlab implementation for each test case.



Debug hint:

- If by any chance your system fails to synthesize with an error similar to this:

```
Error (12006): Node instance "func_accel" instantiates undefined entity "first_nios2_system_func_accel"
```

Double click on the error, select the first line of that unit instantiation, and replace:

```
"first_nios2_system_func_accel" with "func_accel"
```

This happens because somewhere in the script to generate the NIOS II system, the instantiation of your hardware block got its name concatenated with the name of your system.

MARKING SCHEME

The distribution of marks to the tasks is shown below. Please note that the marking will take into consideration your design approach, your achieved results, as well as the quality of the submitted report.

Task	Mark
Tasks: 1 + 2	0 %
Task 3: Storing the Program and Data on External Memories	10 %
Task 4: Evaluate a More Complex Mathematical Expression	10 %
Task 5: Add Multiplier Support	5%
Task 6: Add Hardware Floating-Point units	5%
Task 7: Add dedicated Hardware Block to compute the inner part of the Arithmetic Expression (30% CORDIC implementation/analysis, 10% for the inner part implementation)	40%
Task 8: Add dedicated Hardware Block to compute the Arithmetic Expression	10%
Final Presentation + Interview	20%

Note: Tasks 7 and 8 and the final presentation and interview are individual assessments.

COURSEWORK SUBMISSION**Proposed work schedule and Intermediate deliverables deadlines**

You should register in a logbook all that you have accomplished including results. The logbook doesn't replace the report.

Schedule

Term Week	Tasks	Week starting on:	Deliverable deadline (end of week, Friday@20:00)
2	Task 1: NIOS II Setup Task 2: Computing a simple function	15/1	
3	Task 3: Storing the Program and Data on External Memories Task 4: Evaluate a More Complex Mathematical Expression	22/1	Report 1 (Tasks:1-2)
4	Task 5: Add Multiplier Support	29/1	
5	Task 6: Add Hardware Floating-Point Units	5/2	
6	Task 7: Add Dedicated Hardware Block to Compute the inner part of the Arithmetic Expression	12/2	Report 2 (Tasks: 3-6)
7		19/2	

8	Task 8: Add Dedicated Hardware Block to Compute the Arithmetic Expression	26/2	
9		4/3	
10		11/3	
11	Examination Week (The oral examination will take place at some time in the last week of the term).	18/3	Report 3 and code (Monday 18th @18:00) (Tasks: 7-8)

Only Reports 2 and 3 are assessed. Report 1 should be submitted for feedback. If you are late in submitting your report, the usual College penalty on late submission is applied. In the case of delaying Report 1, a 10% penalty will be applied on the final overall mark.

Reports - Marking

You need to submit three reports on your project (Report 1 and Report 2 as a group, Report 3 as individuals) according to the schedule above.

The reports should contain the following:

- a) Answers to any questions raised in the project hand-out, e.g. performance, FPGA resources, etc.;
- b) Any related design in a block diagram;
- c) A detailed justification of the design choices that you have made;
- d) Any limitations of your design;
- e) For the last report, an elaboration of what you would have done differently if you were doing the project from the beginning (for example you may have found that you took a wrong design decision but it is too late to go back and fix it. It is important to elaborate on this (why you believe it is a wrong decision and what would be a better one).

Please note that special attention will be given on the justification of your design choices and how you have approached the problem. So please provide enough details around these issues.

Also note that the report should not contain any background info like literature review on NIOS. However, the report should provide information on why you have chosen specific algorithms for the calculation of the arithmetic expression.

Below I have listed some general points and good practices on the report writing. Please note that the list below is not exhaustive.

General points

The report should be in pdf format and you should submit your code only for the final report. Provide names and group id on the first page of your report.

I would suggest to use overleaf and a double-column format.

1. Describe clearly the aim of the report and its task

2. Provide discussion on every result that you include. Does it make sense? What conclusions you can draw from the reported results?
3. Be precise when you try to justify the results. Do not just use phrases like "... good enough..", "...very slow..."
4. Avoid using screenshots that do not have any useful info.
5. Do not provide a description of the tutorial that you followed. If there is a specific step that gave you trouble or you think is important to mention, then do just that.
6. Have a conclusion section (task level/report). What did you see? (do not summarize what you did)
7. Pay attention to the structure of the report.
8. Think about adding graphs to make your points more clear.
9. Resources: Your system in the FPGA, and your Program (memory occupied)

Report 1 – Good points to include

1. Discuss your design (elements that you have included)
2. Discuss about resource utilization and timing analysis results
3. Discuss the size of your program, and the memory footprint that you expect your program to need. Do you use dynamic memory allocation? When does the process fail? Perform an offline analysis on the memory requirement of the various test cases to see whether you can fit the data in your system.
4. Discuss your results for the various test cases, and how they compare to Matlab/Python implementation.
5. Discuss the performance of the system (latency)
6. Think about the size of the cache. How does its size affects the performance of the system? Investigate the performance of the system as you change the sizes of instruction and data caches. Explain the obtained results.
7. Investigate how compiler flags can impact the performance of the system.
8. Present your results using graphs and tables. It is better to argue your point in this way.
9. Always include a performance vs resources graph in order to compare your various designs (present and past). Given that the aim is the same across the various tasks, it is interesting to see how the design of your system (moving functionality to dedicated HW) affects the performance and resource utilization of the system.
10. **page limit: 5 pages**

Report 2 - Good points to include

1. Discuss the impact of cache size. How the on-chip memory should be allocated to data cache/instruction cache/on-chip memory?
2. Look into other code optimization approaches. Consider the use of constants rather using variables, as well as expressing the code in a different way.
3. Discuss the implementation of cos function. Consider how it has been implemented in math.h library in C. Consider other versions of cos like cosf. Consider the Taylor expansion for the cos evaluation. What is the trade-off between number of terms and latency/accuracy? Consider a lookup implementation.
4. **page limit: 5 pages**

Report 3 - Good points to include

1. Comparison to previous implementations
2. High level view diagram (block diagram) of your design and clear indication on how you call your IP from NIOS (i.e. include main loop for the computation)
3. Elaboration on the selection of the latency, achieved performance, area/resources, achieved error
4. Elaboration on your CORDIC architecture and its justification
5. Elaboration on the design decisions behind the CORDIC architecture for achieving the required accuracy level.
6. Elaboration on the final adder to complete the whole design (function evaluation in HW)
7. **page limit: 5**

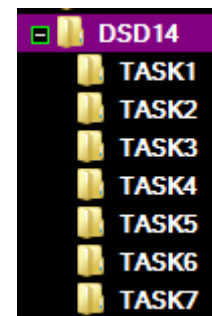
Please note that any pages beyond the page limit will not be taken into account. The page limit only refers to the body of the report (excludes the first page if it is just the title and names, and any references)

Code

Each group needs to upload the source files of their project **for the most advanced design**, at the end of the project.

The source files should be organised with subdirectories according to the coursework tasks. **You only need to submit the most advanced working design (task)**. Please include the following extensions:

.qpf - quartus project
 .qsf - quartus settings
 .sdc - timing constraints
 .sopcinfo - system info
 .qsys - system specification
 .vhd - vhdl source files
 .v - verilog source files
 .qip - megawizard component
 .tcl - script
 .bdf - block diagrams
 .bsf - symbols
 .do - modelsim macro
 .mpf - modelsim project
 .c - C source files
 .h - C include files
 .bsp - bsp settings
 .map
 .hex
 .bin
 .cproject/.project - eclipse project defs



You can follow the instructions below to make a .ZIP file with the deliverables:

1. Make a copy of your work containing only the designs/software you want to submit.
2. start command line "cmd";
3. change drive and directory to be your DSD folder e.g. "e:" "cd /dsd14/";
4. execute the following command. It will copy your sources into a zip file;

```
zip dsd -rq . -i "*.h" "*.c" "*.bsp" "*.map" "*.qsf" "*.qpf" "*.sdc" "*.sopcinfo"
  "*.qsys" "*.vhd" "*.v" "*.qip" "*.tcl" "*.bdf" "*.bsf" "*.do" "*.mpf" "*.project"
  "*.bin" "*.hex"
```

5. verify the zip file contains all the source files you want to submit for evaluation;
6. upload the file.

APPENDIX

Troubleshooting

Below there's a list of common problems and their solutions:

Problem	Solution
Unable to program the FPGA	Check whether the Programmer in Quartus has been properly set up for the device. It should be in JTAG mode through USB.
In Eclipse, you get the message: "Failed to execute: ./create-this-app -no-make"	This error may be generated by the Altera Complete Design Suite software version 10.0 and 10.0 SP1 when creating a software project by selecting Nios II Application and BSP from Template in the Nios II Software Build Tools (SBT) for Eclipse on Windows 7 using a non-administrator account. To work around this error when running on Windows 7, run the Nios II SBT for Eclipse as with administrator privileges. On the Windows Start menu, point to All Programs , point to Altera , point to Nios II EDS , right-click on Nios II Software Build Tools for Eclipse , and select Run as administrator .
Missing dependencies in Eclipse	Please add the following path in Eclipse (under Properties) in GNU C paths and symbols : C:\altera\13.0sp1\quartus\bin\cygwin\usr\include (or any the related path in your installed version of Quartus)
Project fails to compile/run Analysis & Elaboration	There's an issue with the names of paths. To solve this you need to use a local directory instead of your home (H:) directory.
No output from printf("%f")	The small C library doesn't support printf("%f") you should use gcvt(), as illustrated in the handout.
Not enough memory or no output for on-chip your application	On-chip memory is very limited. You can't use functions from includes such as math.h. Work out your algorithm to do the same using basic arithmetic operators. Change the size of your on-chip memory to 40960-49152 bytes; Edit BSP and disable: C++, clean exit, exit; enable: small C, reduced drivers.
Simulation of the accelerator is OK, but it doesn't work with NIOS	You may have to simulate the complete system (not advised). More details here: http://www.altera.com/support/examples/nios2/exm-simulating-niosii.html http://www.alterawiki.com/wiki/Simulating_Nios_II_Designs_with_Program_Memory_on_External_Flash_and_SSRAM
SDRAM settings for DE0 board	SDRAM settings: preset: custom; bits: 16; cs: 1; banks: 4; row: 12; col: 8; cas: 3; init: 2; refresh: 15.625; delay: 100; t_rfc: 70; t_rp: 20; t_rcd: 20; t_ac: 5.5; t_wr: 14;
It takes too long from generation of the system to running an application in NIOS	To accelerate the process, disable (in Platform Designer) all components that are not being used in your system (e.g. on-chip memory and led_pio). Less components means processing less time: generating the system in Qsys, compiling the design in Quartus II, generating the BSP and compiling less drivers with your application. :). Do not forget to re-generate the memory address space.
Custom Instruction	Figure on page 25: Your data are passed through dataa and datab (32 bits), not through ports a and b (5 bits).

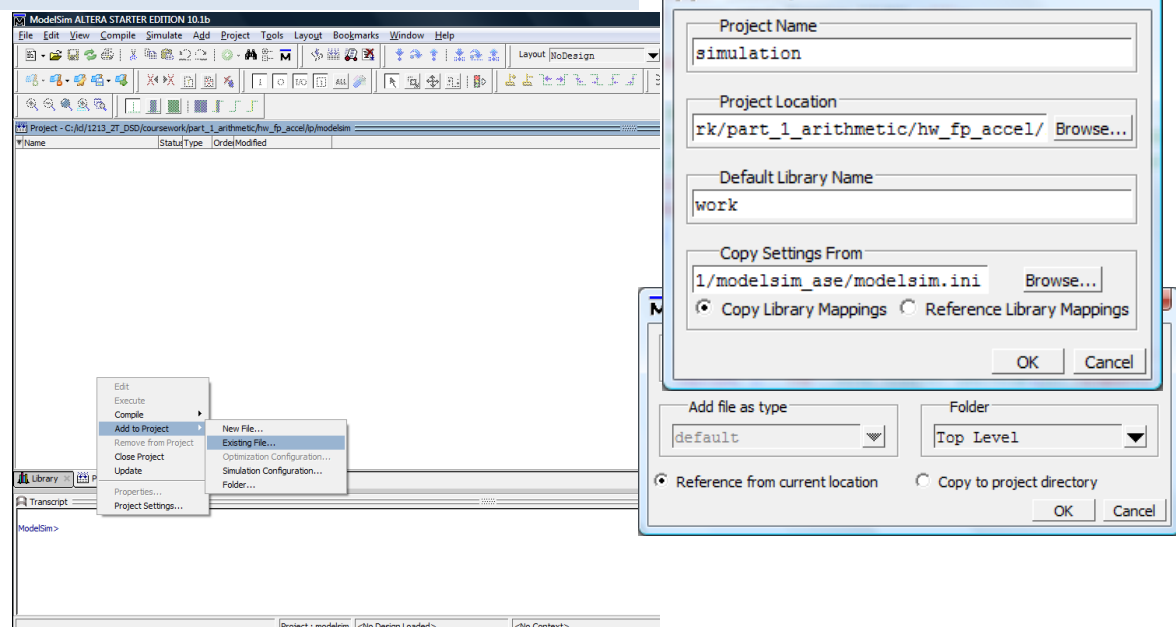
Name of Components in Qsys and Quartus	Remove "_0" from the default name given by Qsys/Quartus. Don't use "_" and a number as a suffix for the names of your units.
----------------------------------------	------------------------------------------------------------------------------------------------------------------------------

Quartus II Tutorial

Quartus is the application that maps your design to a particular FPGA device. More information on Quartus can be found in

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/intro_to_quartus2.pdf

Modelsim Tutorial



Application Profiling

In the quest to accelerate complex applications, it may not be obvious which instructions take most of the processor's time. To measure the performance of parts of your application you can make use of an external profiler or measure the time require. Altera provides an application note specific on this subject. You can find it here:



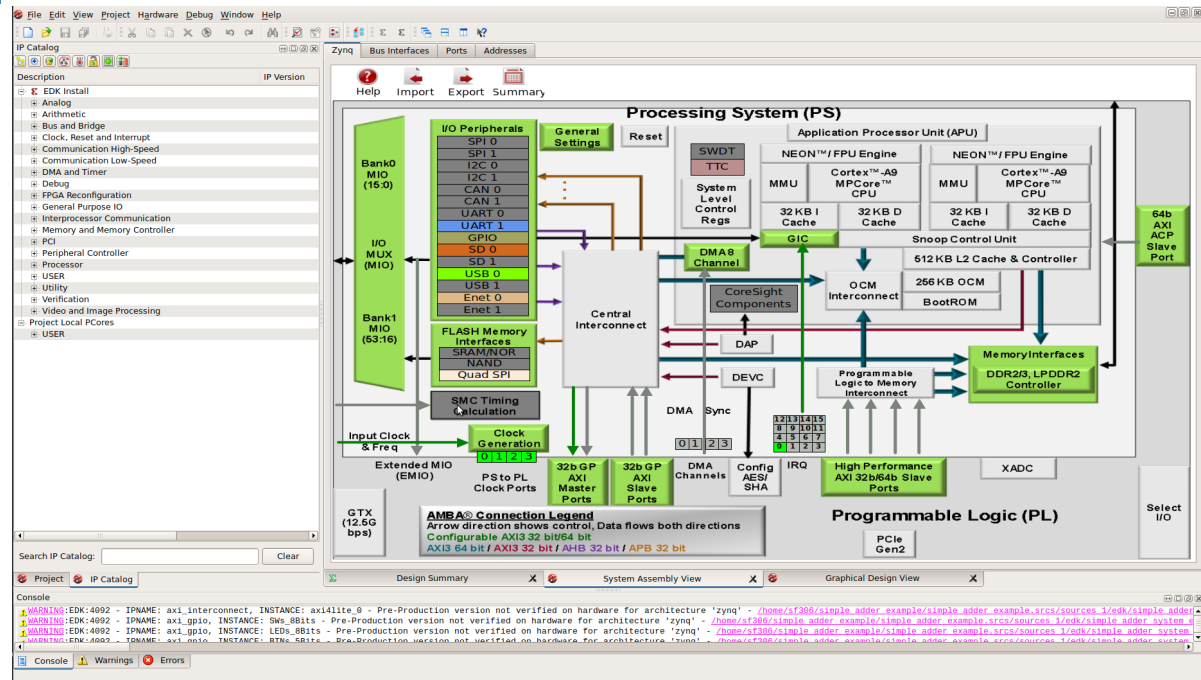
<http://www.altera.com/literature/an/an391.pdf>

Alternatives to NIOS II/Altera

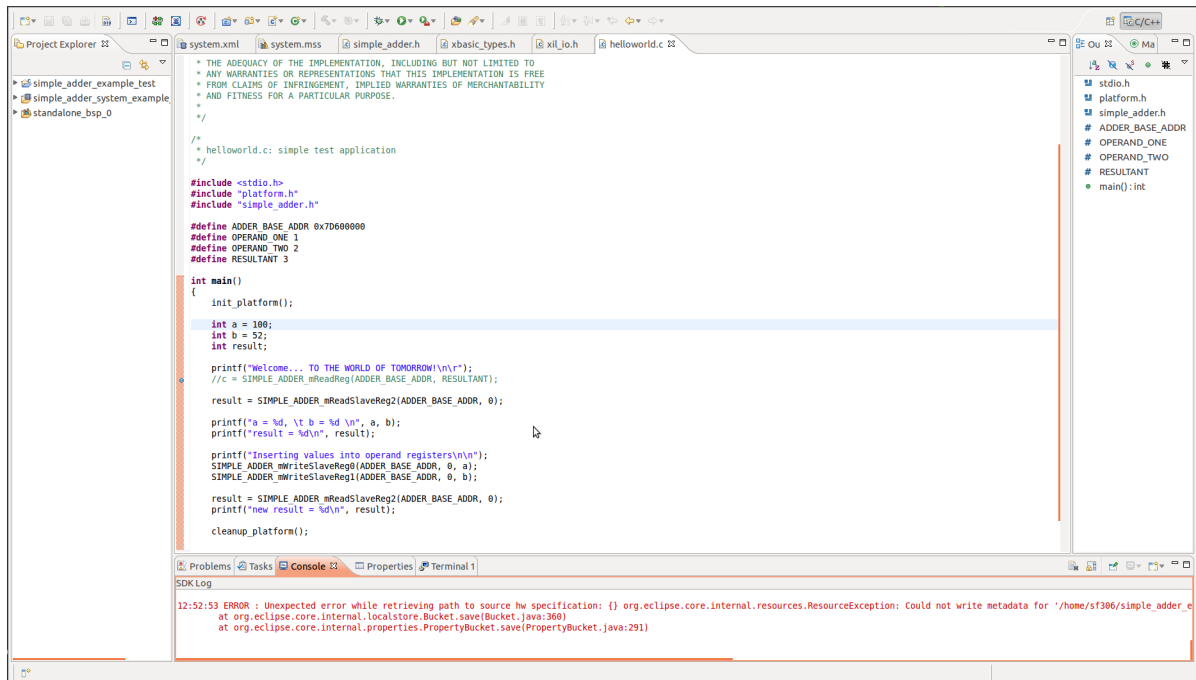
Embedded systems with soft/hard processors and reconfigurable logic are common. Similar to Altera (NIOS II) there are alternatives, namely Zynq from Xilinx. The Zynq system has a hard processor occupying a region of the device, which cannot be used for reconfigurable logic, but on the other hand the processor has enough computational power to run Ubuntu on it.

Here are screenshots of the development environments for hardware (XPS) and software (SDK). You'll find them similar to the tools you're using in this coursework.

XPS



SDK



Remote Compilation

Design compilation can require quite a few resources from your computer, and if you have a slow computer or are using a VM, you may want to compile your project remotely (for reference, both the server and Level 5 computers take roughly 5 minutes to compile designs). The teaching server, **ee-mill1**, has Quartus 18.1 installed. To access this server, follow the instructions in the link below:

<https://wiki.imperial.ac.uk/pages/viewpage.action?pageId=250302869>

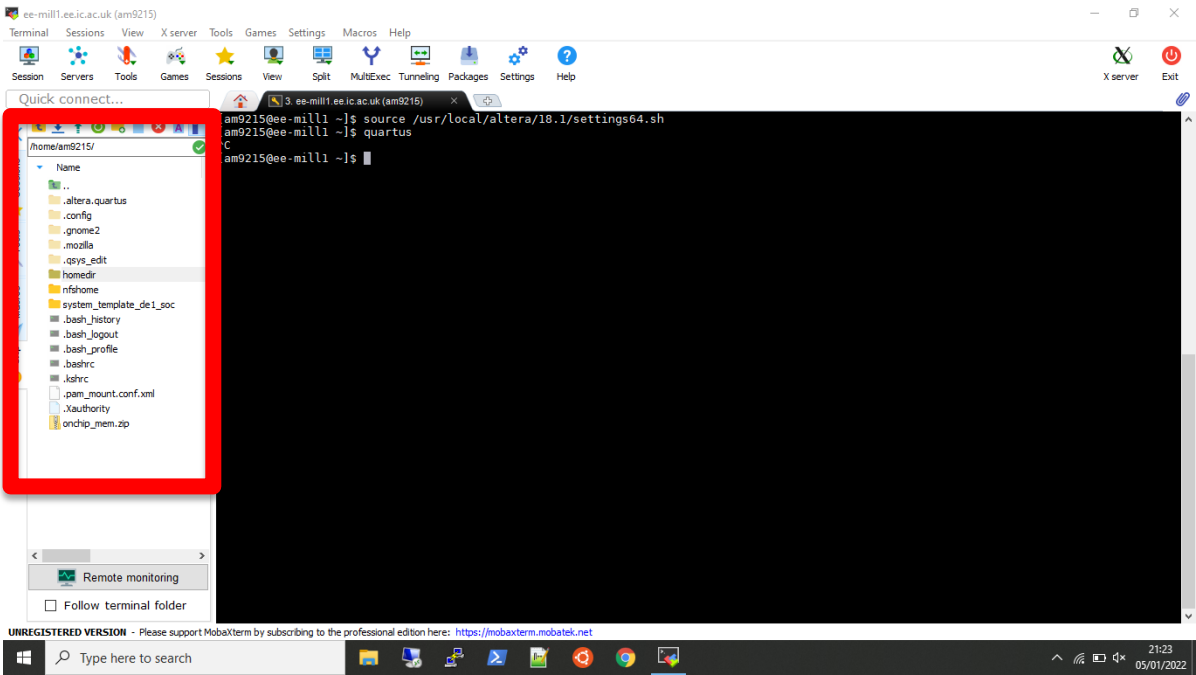
Once you have setup a connection, you need to do the following steps to run Quartus:

1. In the SSH shell command line, run: `source /usr/local/altera/18.1/settings64.sh`
2. Then to open Quartus, run: `quartus`

(You can add the first command to your .bashrc file)

This will open Quartus, which you can use to compile projects. If you plan to solely use the servers for compilation, it is recommended to keep all the project files here and only copy over the **.sof** and **.sopcinfo** files for programming the board and software development respectively. If you wish to move a whole project to the server, you are recommended to zip the project using the command in the *Code* appendix section.

To move files, if you are using MobaXterm, you can use the file explorer on the left, as shown below:



For mac and linux users, you can use the scp command, like so:

To server: scp <local-file> <username>@ee-mill1.ee.ic.ac.uk:<remote-destination>

From server: scp <username>@ee-mill1.ee.ic.ac.uk:<remote-file> <local-destination>

*** end of document ***

Version Table

Version	Date	Notes
v5.4	Nov 2023	<p>Provide further guidance to the students on how to explore the cache sizes for the system.</p> <p>Split the project after task 6 to two parts. Introduction of an individual component.</p> <p>Report 2 covers up to tasks 6 (including), where Report 3 covers tasks 7 and 8.</p>