Islamic University of Technology (IUT)
Organisation of Islamic Cooperation (OIC)

Department of Electrical and Electronic Engineering
Electronics Laboratorv. Room No.:502

Student ID. : ……………………

Date & Year: ………………… Working Table No. : ……. Section: …….. Group: ..…………

Course: EEE 4384 (Electronic Devices and Circuits Lab)

Experiment no.: 02

Name of the experiment: Study of BJT Amplifier (with Frequency Response) and Switch.

Objectives:

- To observe the operation of BJT as a switch, and to construct the DC load line.
- To observe the operation of Common Emitter (CE) and investigate the frequency response of CE amplifier.

Apparatus required:

S.NO.	NAME OF THE EQUIPMENT	TYPE	RANGE	QUANTITY (NO.S)
1.	BJT			1
2.	LED			1
3.	Resistor		10 kΩ	1
4.	Capacitor		1μF	1
5.	Oscilloscope	MC		1
6.	Standard Project Board	MC		1
7.	Function/Signal Generator	MC		1
8.	Connecting wires			Required

Task 1:

- To construct the BJT switch circuit.
- To measure the specified currents in ON and OFF states of the switch.
- To draw the DC load line using the measured values.

Theory:

BJT can be operated in three regions: cut-off region, active region and saturation region. While using a BJT for amplification purpose, we operate it in the active region. If we operate BJT in cut-off and saturation region in amplifier, clipping of waveforms will occur.

Now, when we use BJT as a switch, it is operated in cut-off and saturation regions. In saturation region, the transistor acts as ON switch. In cut-off region, it acts as OFF switch. In fact, we are operating the BJT only in two points of the DC load line while it is used as a switch.

Circuit Diagram:

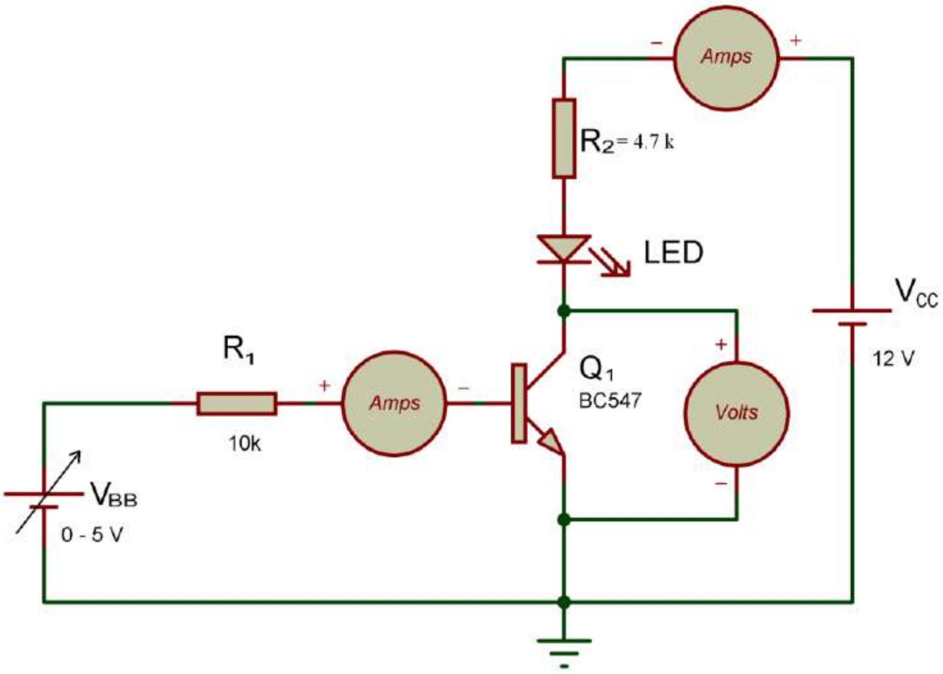


Figure-1

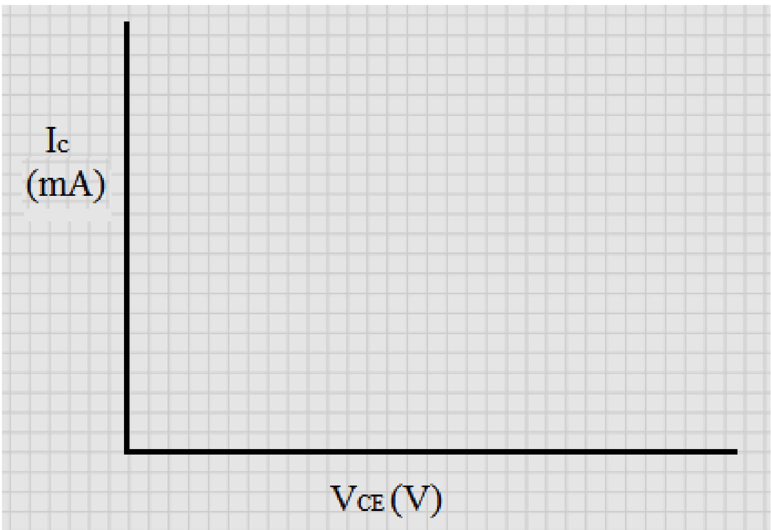
Procedure:

1. The circuit in Figure-3, keep the collector supply V_{CC} = +12 V and base supply V_{BB}= 0 V. This will make the switch OFF.
2. Measure the collector and base currents (I_C and I_B), and also the voltage between the collector and the emitter (V_{CE}). The LED is off as the BJT (switch) is OFF (operating in cut-off region).
3. Now apply +5 V to the base (V_{BB} = +5 V). This makes the BJT (switch) ON (operating in saturation). Now, notice that the LED is turned on.
4. Measure I_B, I_C and V_{CE} in this case.

Data:

- **Switch OFF (V$_{BB}$ = 0) :** I_B = ………….. I_C = ………… V_{CE} = ……………..
- **Switch ON (V$_{BB}$ = 5V) :** I_B = ………….. I_C = ………… V_{CE} = ……………..

Using data, construct the DC load line below, and mark the two operating points (ON and OFF states).



Graph: DC Load line

Task 2:

- To construct the Common Emitter (CE) amplifier circuit.
- To observe the input-output wave shapes.
- To measure the gain of amplifier at different frequencies and plot the frequency response.

Theory:

Common emitter amplifier is used to amplify weak signal. It utilizes energy from DC power supply to amplify input AC signal. Biasing of transistor is done to tie Q point at the middle of the load line. In the circuit shown, voltage divider bias is formed using resistors 10K and 2.2K. During positive half cycle of the input, forward bias voltage of base-emitter junction increase. So, the base current increases. Q point moves upward on the load line and the collector current increases β times the base current (β is current gain). As a result, collector resistor drop $I_c R_c$ increases due to increase in collector current I_c. This reduces collector voltage. Thus, during positive input cycle, we get negative output cycle. When input is in the negative half cycle, forward bias of base-emitter junction and base current reduces. Collector current reduces consequently (Q point moves downside). As a result, $I_c R_c$ reduces and collector voltage increases. Change in collector voltage is much higher than applied base voltage because less base current variation causes large collector current variation due to the current gain β. This large collector current is further multiplied by R_c, which provides large voltage output. Thus CE amplifier amplifies the input signal. Without emitter resistance, gain of amplifier is highest, but it is not stable. Emitter resistance is used to provide stability. To compensate the effect of emitter resistance, bypass capacitor is used, which provides AC ground to the emitter. This increases the gain of amplifier.

CE amplifier does not provide constant voltage gain at all frequencies. Due to emitter bypass and coupling capacitors, gain of amplifier is reduced at low frequency. Reactance of capacitor is high at low frequency; hence emitter bypass capacitor does not provide perfect AC ground (Emitter impedance is high). There is significant voltage drop across coupling capacitor at low frequency because of its high reactance. Gain of CE amplifier also reduces at very high frequency because of stray capacitances.

If we apply large signal at the input of CE amplifier, transistor is driven into saturation region during positive peak and cut-off region during negative peak (Q point reaches to saturation and cut-off points). Due to this, clipping occurs in amplified signal. So, we have to apply small signal at the input and ensure that transistor operates in active region.

Procedure:

1. The circuit in Figure-2, Set input voltage = 100 mV and frequency = 100 Hz (from signal generator).
2. Observe and measure the amplified output signal. Draw the input and output wave shapes.
3. Now, vary the input frequency between 100 Hz and 10 MHz. Observe the output and measure the voltage gain (in dB) in each case. Complete the table below with your obtained data.
4. Plot the voltage gain against frequency in the semi-log graph.

Circuit Diagram:

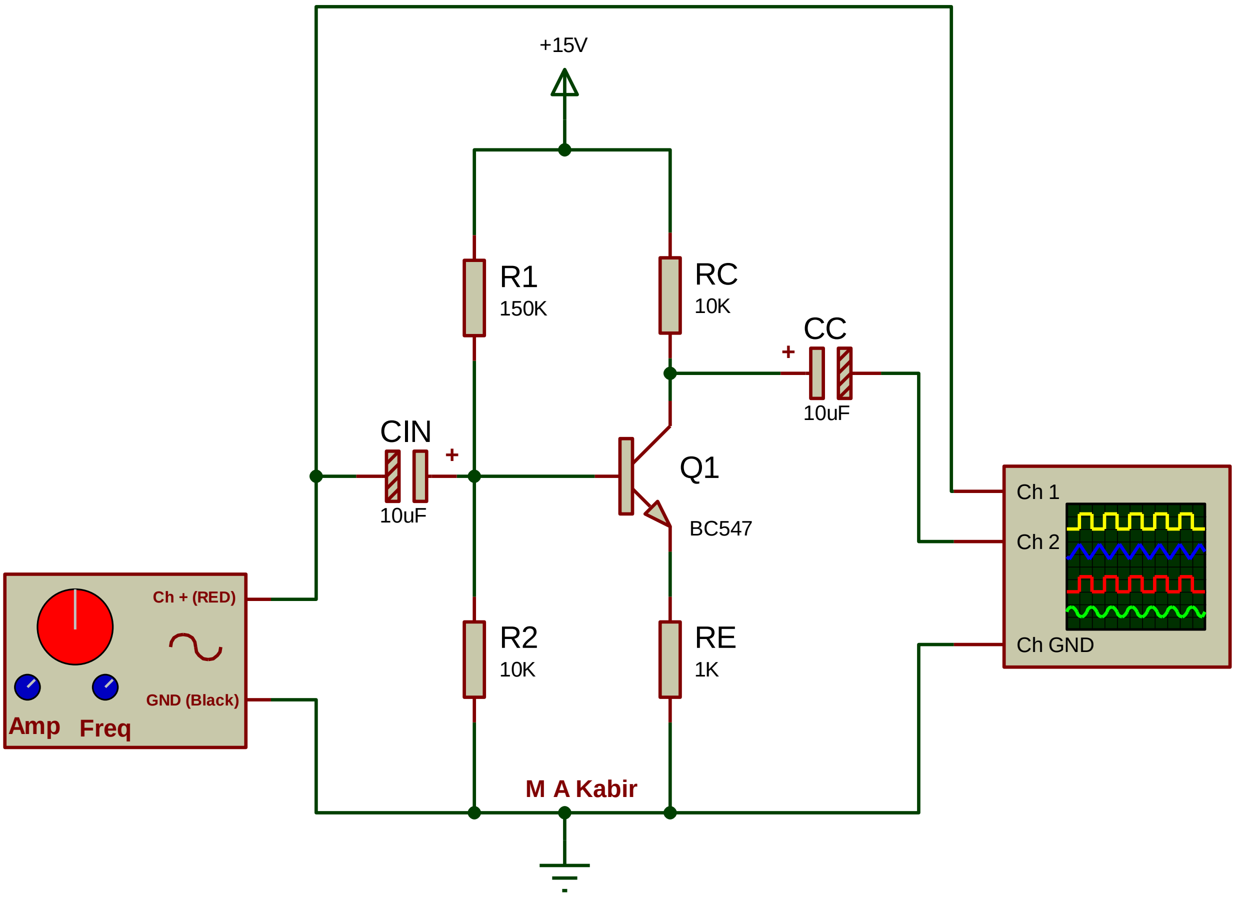


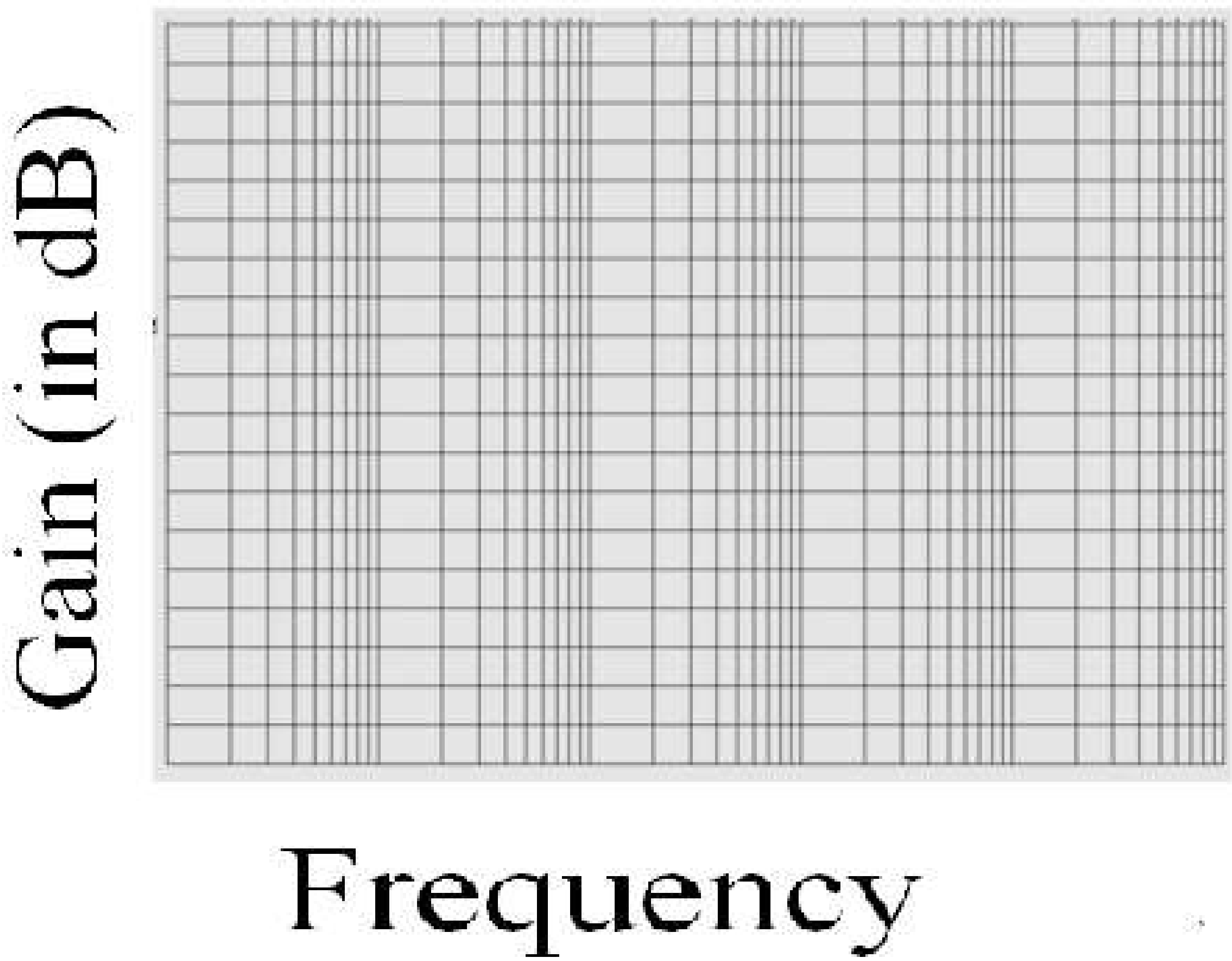
Figure-2

Figure: Input voltage at 100 Hz

Figure: Output voltage at 100 Hz

Data Table: (Vᵢ = 10 mV, Gain in dB = 20 log A)

Sl. No.	V_i Frequency	V_o Amplitude	Voltage Gain, A = V_o/V_i	Gain (dB)



Graph: Semi-log

Discussion: