San Francisco State University

Electrical Engineering

ENGR 378 Digital Systems Design

Lab 4. Downloading to FPGA

Objectives

• To learn how to prepare your Verilog design for implementation on actual hardware, an FPGA.

• To learn how to download our program to a commercial FPGA, and run it.

Prelab

In regards to task 2 of this lab, consider the following diagram as one way to organize the design for the Multi-code Converter Module.

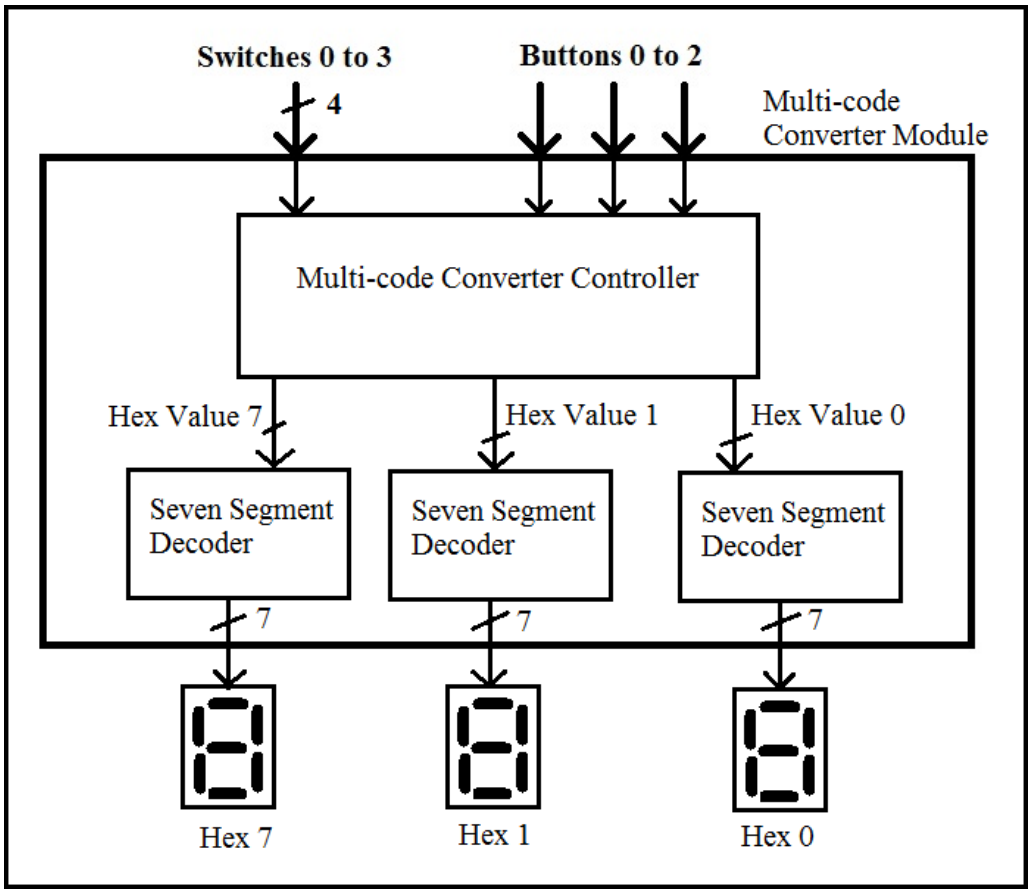

Figure 1: Multi-code Converter Module

For the prelab do **one** of the following and show to TA for prelab sign-off. Regardless of which choice you choose for the prelab, make sure you have an idea of how to write VHDL code to model it:

Choose one of the following to do for the prelab:

A**) Draw the circuit diagram** for the Multi-code Converter Controller in the Multi-Code Converter Module. Simplify where possible.

B) **Write pseudo-code** for the Multi-code Converter Controller in the Multi-Code Converter Module. Show what values are output from the Multi-code Converter Controller for the cases when button 0, button 1, and button 2 are pushed.

C) **In words**, write out how you would facilitate signals to the outputs of the multi-code converter controller given the cases of when button 0, button 1, and button 2 are pressed.

For the Seven segment decoder, write up a truth table for all possible inputs of a 4 bit seven segment decoder and its respective seven bit output that drives each seven segment display. Also notice that each seven segment LED in the display requires an active low signal. You can read the DE2_115 User Manual on how the seven segment displays are used in the "Using the 7-segment Displays" section on page 36.

Tasks

1. The first task will be to download a sample project to your FPGA in the DE2-115 Board. Open the Quartus_Intro_Tutorial_To_Verilog.pdf file from lab 1 and follow the instructions starting from page 29 "Programming and Configuring the FPGA Device" to the end of the tutorial. Resume your work from lab 1 to download the XOR gate design to the FPGA board.

Have the lab instructor sign off for the XOR gate after it is downloaded successfully to the FPGA (signoff #1).

2. Design, simulate and download your own complete application: Multi-code Converter.

a) The program will convert a four bit code into one of the following:

i. A 1-digit Hex number: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

ii. A 1-digit decimal number (BCD): 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, (Display 9 for value 10+)

iii. A 2 digits decimal number: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16

b) The 4 bit code will be entered through the 4 switches available in the board (SW0 to SW3).

c) The type of conversion will be selected by pressing one of three push buttons in the board (BTN0 to BTN2).

d) The result of the conversion should be displayed in the two **rightmost** 7-segment displays (no leading zeros).

e) The **leftmost** 7-segment display in the board must show the current type of conversion: “h” for hex, “b” for BCD, “d” for decimal.

Have the TA sign off for the Multi-code Converter after it is downloaded successfully to the FPGA (signoff #2).

Notes

• Each team should borrow (one member of the team will sign for it) the FPGA test board, including power supply and download cable, from the stock room. The team is responsible for this material and should handle it carefully in order to avoid damage. It will be returned at the end of the semester.