# PSoC® Creator™
# Project Datasheet for FiReBuG as Mic

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**Project: FiReBuG as Mic**

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# 1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through Serial Wire Debug (SWD), and Single Wire Viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Family Block Diagram

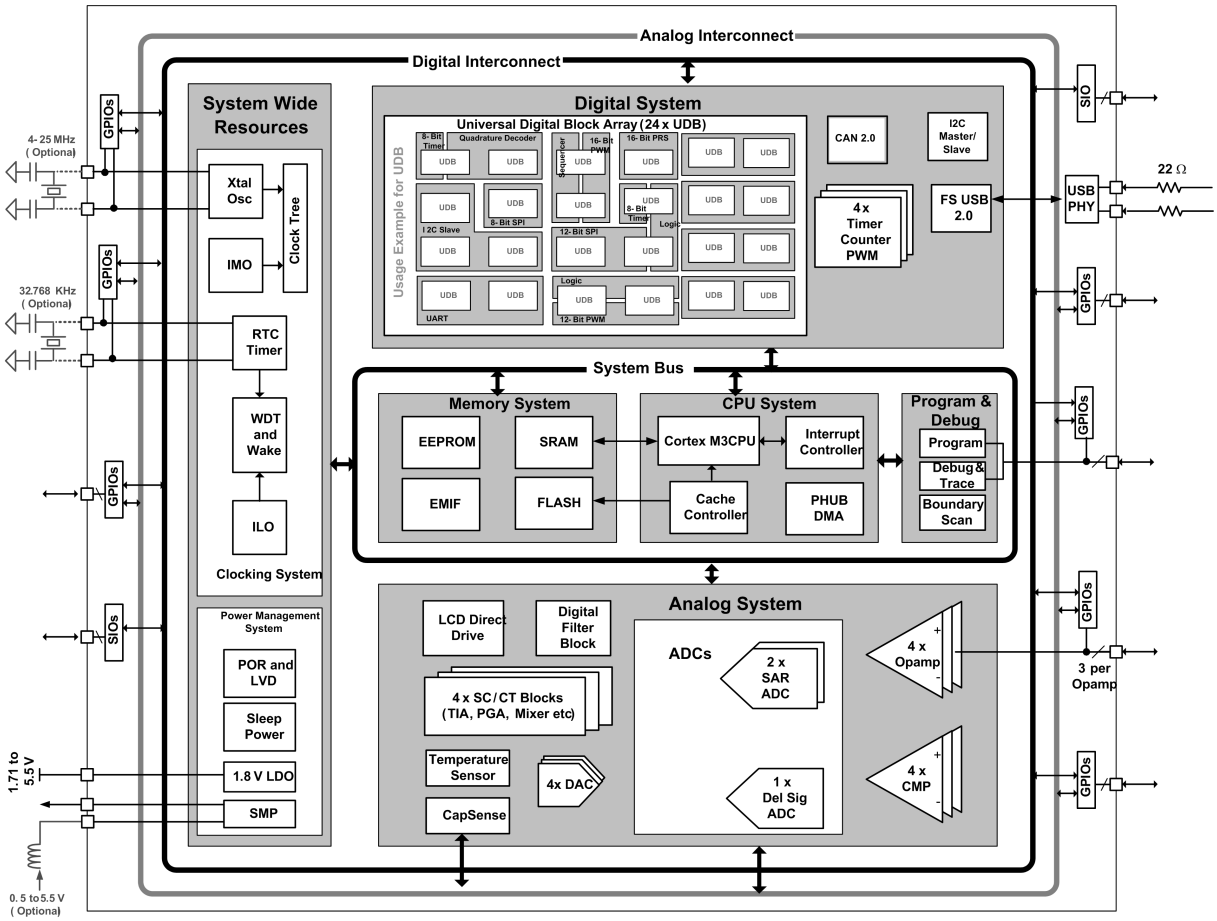


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

| Name | Value |
|---|---|
| Architecture | PSoC 5LP |
| Family | CY8C58LP |
| CPU speed (MHz) | 67 |
| Flash size (kBytes) | 256 |
| SRAM size (kBytes) | 64 |
| EEPROM size (Bytes) | 2048 |
| Trace Buffer (kBytes) | 0 |
| Vdd range (V) | 1.71 to 5.5 |
| Automotive qualified | No (Industrial Grade Only) |
| Temp range (Celcius) | -40 to 85 |
| JTAG ID | 0x2E127069 |

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by BUS_CLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

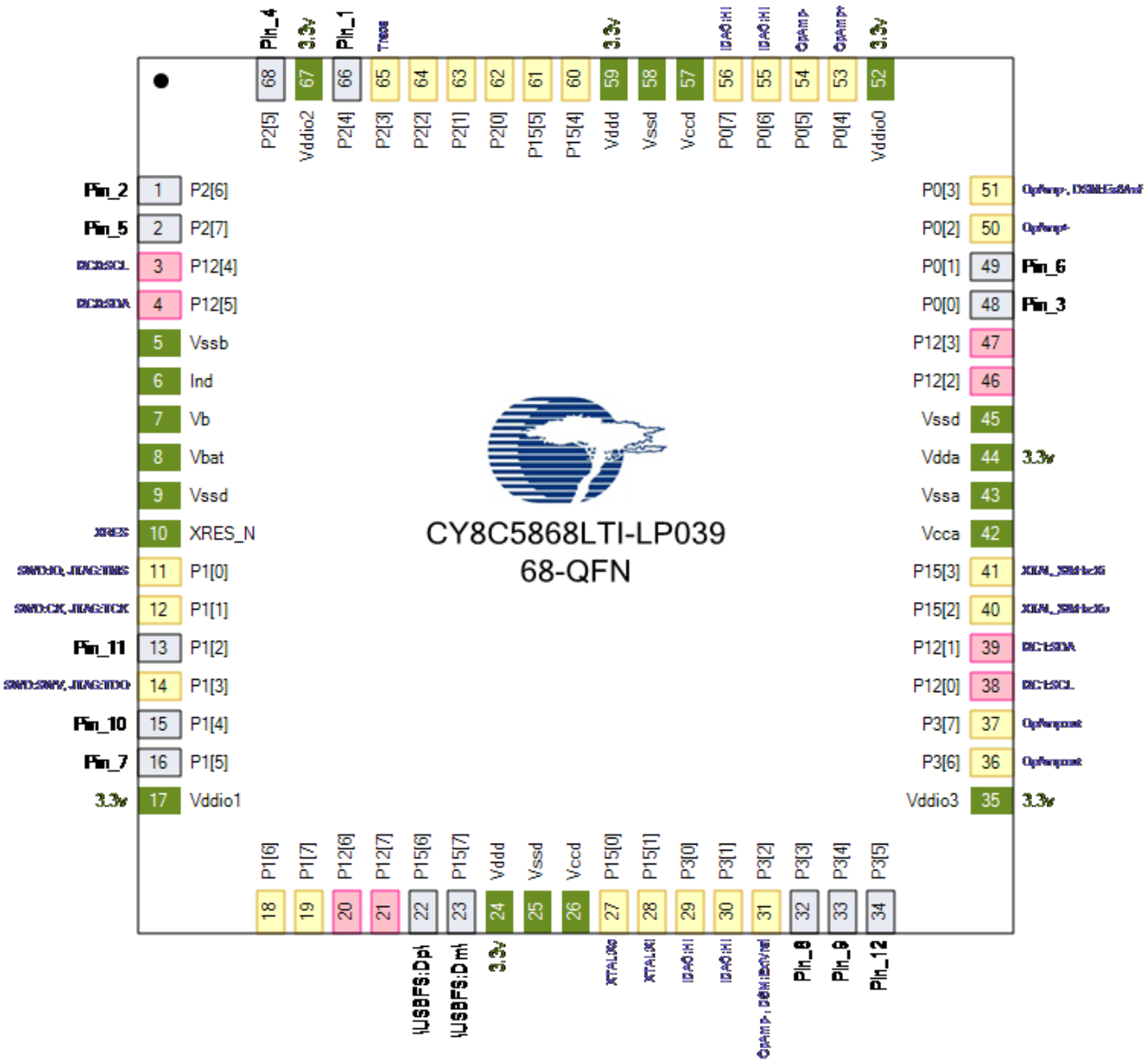
Table 2. Device Resources

| Name | Resources in Use | Total Resources Available |
|---|---|---|
| Digital clock dividers | 4 (50.0%) | 8 |
| Analog clock dividers | 0 (0.0%) | 4 |
| Pins | 14 (29.2%) | 48 |
| UDB Macrocells | 33 (17.2%) | 192 |
| UDB Unique Pterms | 60 (15.6%) | 384 |
| UDB Datapath Cells | 6 (25.0%) | 24 |
| UDB Status Cells | 1 (4.2%) | 24 |
| UDB Control Cells | 0 (0.0%) | 24 |
| DMA Channels | 6 (25.0%) | 24 |
| Interrupts | 12 (37.5%) | 32 |
| DSM Fixed Blocks | 0 (0.0%) | 1 |
| VIDAC Fixed Blocks | 0 (0.0%) | 4 |
| SC Fixed Blocks | 4 (100.0%) | 4 |
| Comparator Fixed Blocks | 4 (100.0%) | 4 |
| Opamp Fixed Blocks | 0 (0.0%) | 4 |
| CapSense Buffers | 0 (0.0%) | 2 |
| CAN Fixed Blocks | 0 (0.0%) | 1 |
| Decimator Fixed Blocks | 0 (0.0%) | 1 |
| I2C Fixed Blocks | 0 (0.0%) | 1 |
| Timer Fixed Blocks | 0 (0.0%) | 4 |
| DFB Fixed Blocks | 0 (0.0%) | 1 |
| USB Fixed Blocks | 1 (100.0%) | 1 |
| LCD Fixed Blocks | 0 (0.0%) | 1 |
| EMIF Fixed Blocks | 0 (0.0%) | 1 |
| LPF Fixed Blocks | 0 (0.0%) | 2 |
| SAR Fixed Blocks | 0 (0.0%) | 2 |

# 2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



## 2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

| Pin | Port | Name | Type | Drive Mode | Reset State |
|---|---|---|---|---|---|
| 1 | P2[6] | Pin_2 | Dgtl Out | Strong drive | HiZ Analog Unb |
| 2 | P2[7] | Pin_5 | Dgtl Out | Strong drive | HiZ Analog Unb |
| 3 | P12[4] | SIO [unused] | | | HiZ Analog Unb |
| 4 | P12[5] | SIO [unused] | | | HiZ Analog Unb |
| 5 | Vssb | Vssb | Power | | |
| 6 | Ind | Power | | | |
| 7 | Vb | Vb | Power | | |
| 8 | Vbat | Vbat | Power | | |
| 9 | Vssd | Vssd | Power | | |
| 10 | XRES_N | XRES_N | Power | | |
| 11 | P1[0] | GPIO [unused] | | | HiZ Analog Unb |
| 12 | P1[1] | GPIO [unused] | | | HiZ Analog Unb |
| 13 | P1[2] | Pin_11 | Dgtl Out | Strong drive | HiZ Analog Unb |
| 14 | P1[3] | GPIO [unused] | | | HiZ Analog Unb |
| 15 | P1[4] | Pin_10 | Analog | HiZ analog | HiZ Analog Unb |
| 16 | P1[5] | Pin_7 | Analog | HiZ analog | HiZ Analog Unb |
| 17 | Vio1 | Vio1 | Power | | |
| 18 | P1[6] | GPIO [unused] | | | HiZ Analog Unb |
| 19 | P1[7] | GPIO [unused] | | | HiZ Analog Unb |
| 20 | P12[6] | SIO [unused] | | | HiZ Analog Unb |
| 21 | P12[7] | SIO [unused] | | | HiZ Analog Unb |
| 22 | P15[6] | \USBFS:Dp\ | Analog | HiZ analog | HiZ Analog Unb |
| 23 | P15[7] | \USBFS:Dm\ | Analog | HiZ analog | HiZ Analog Unb |
| 24 | Vddd | Vddd | Power | | |
| 25 | Vssd | Vssd | Power | | |
| 26 | Vccd | Vccd | Power | | |
| 27 | P15[0] | GPIO [unused] | | | HiZ Analog Unb |
| 28 | P15[1] | GPIO [unused] | | | HiZ Analog Unb |
| 29 | P3[0] | GPIO [unused] | | | HiZ Analog Unb |
| 30 | P3[1] | GPIO [unused] | | | HiZ Analog Unb |
| 31 | P3[2] | GPIO [unused] | | | HiZ Analog Unb |
| 32 | P3[3] | Pin_8 | Dgtl Out | Strong drive | HiZ Analog Unb |
| 33 | P3[4] | Pin_9 | Analog | HiZ analog | HiZ Analog Unb |
| 34 | P3[5] | Pin_12 | Analog | HiZ analog | HiZ Analog Unb |
| 35 | Vio3 | Vio3 | Power | | |
| 36 | P3[6] | GPIO [unused] | | | HiZ Analog Unb |
| 37 | P3[7] | GPIO [unused] | | | HiZ Analog Unb |
| 38 | P12[0] | SIO [unused] | | | HiZ Analog Unb |
| 39 | P12[1] | SIO [unused] | | | HiZ Analog Unb |
| 40 | P15[2] | GPIO [unused] | | | HiZ Analog Unb |
| 41 | P15[3] | GPIO [unused] | | | HiZ Analog Unb |
| 42 | Vcca | Vcca | Power | | |
| 43 | Vssa | Vssa | Power | | |
| 44 | Vdda | Vdda | Power | | |
| 45 | Vssd | Vssd | Power | | |

| Pin | Port | Name | Type | Drive Mode | Reset State |
|---|---|---|---|---|---|
| 46 | P12[2] | SIO [unused] | | | HiZ Analog Unb |
| 47 | P12[3] | SIO [unused] | | | HiZ Analog Unb |
| 48 | P0[0] | Pin_3 | Analog | HiZ analog | HiZ Analog Unb |
| 49 | P0[1] | Pin_6 | Analog | HiZ analog | HiZ Analog Unb |
| 50 | P0[2] | GPIO [unused] | | | HiZ Analog Unb |
| 51 | P0[3] | GPIO [unused] | | | HiZ Analog Unb |
| 52 | Vio0 | Vio0 | Power | | |
| 53 | P0[4] | GPIO [unused] | | | HiZ Analog Unb |
| 54 | P0[5] | GPIO [unused] | | | HiZ Analog Unb |
| 55 | P0[6] | GPIO [unused] | | | HiZ Analog Unb |
| 56 | P0[7] | GPIO [unused] | | | HiZ Analog Unb |
| 57 | Vccd | Vccd | Power | | |
| 58 | Vssd | Vssd | Power | | |
| 59 | Vddd | Vddd | Power | | |
| 60 | P15[4] | GPIO [unused] | | | HiZ Analog Unb |
| 61 | P15[5] | GPIO [unused] | | | HiZ Analog Unb |
| 62 | P2[0] | GPIO [unused] | | | HiZ Analog Unb |
| 63 | P2[1] | GPIO [unused] | | | HiZ Analog Unb |
| 64 | P2[2] | GPIO [unused] | | | HiZ Analog Unb |
| 65 | P2[3] | GPIO [unused] | | | HiZ Analog Unb |
| 66 | P2[4] | Pin_1 | Analog | HiZ analog | HiZ Analog Unb |
| 67 | Vio2 | Vio2 | Power | | |
| 68 | P2[5] | Pin_4 | Analog | HiZ analog | HiZ Analog Unb |

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- HiZ analog = High impedance analog

## 2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

| Name | Port | Type | Reset State |
|---|---|---|---|
| \USBFS:Dm\ | P15[7] | Analog | HiZ Analog Unb |
| \USBFS:Dp\ | P15[6] | Analog | HiZ Analog Unb |
| Pin_1 | P2[4] | Analog | HiZ Analog Unb |
| Pin_10 | P1[4] | Analog | HiZ Analog Unb |
| Pin_11 | P1[2] | Dgtl Out | HiZ Analog Unb |
| Pin_12 | P3[5] | Analog | HiZ Analog Unb |
| Pin_2 | P2[6] | Dgtl Out | HiZ Analog Unb |
| Pin_3 | P0[0] | Analog | HiZ Analog Unb |
| Pin_4 | P2[5] | Analog | HiZ Analog Unb |
| Pin_5 | P2[7] | Dgtl Out | HiZ Analog Unb |
| Pin_6 | P0[1] | Analog | HiZ Analog Unb |
| Pin_7 | P1[5] | Analog | HiZ Analog Unb |
| Pin_8 | P3[3] | Dgtl Out | HiZ Analog Unb |
| Pin_9 | P3[4] | Analog | HiZ Analog Unb |
| Power | Ind | | |

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

# 3 System Settings

## 3.1 System Configuration

Table 5. System Configuration Settings

| Name | Value |
|---|---|
| Device Configuration Mode | Compressed |
| Enable Error Correcting Code (ECC) | False |
| Store Configuration Data in ECC Memory | True |
| Instruction Cache Enabled | True |
| Enable Fast IMO During Startup | True |
| Unused Bonded IO | Allow but warn |
| Heap Size (bytes) | 0x1000 |
| Stack Size (bytes) | 0x4000 |
| Include CMSIS Core Peripheral Library Files | True |

## 3.2 System Debug Settings

Table 6. System Debug Settings

| Name | Value |
|---|---|
| Debug Select | GPIO |
| Enable Device Protection | False |
| Embedded Trace (ETM) | False |
| Use Optional XRES | False |

## 3.3 System Operating Conditions

Table 7. System Operating Conditions

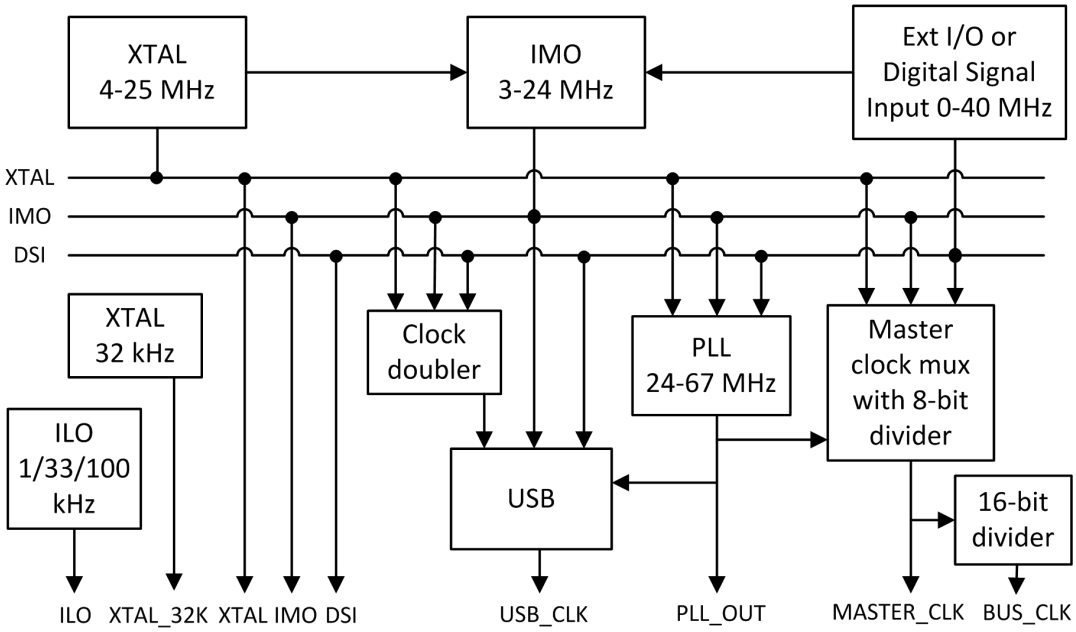
| Name | Value |
|---|---|
| Vddd (V) | 3.3 |
| Vdda (V) | 3.3 |
| Variable Vdda | False |
| Vddio0 (V) | 3.3 |
| Vddio1 (V) | 3.3 |
| Vddio2 (V) | 3.3 |
| Vddio3 (V) | 3.3 |
| Temperature Range | -40C - 85/125C |

# 4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±5% at 3 MHz
  - 1 kHz, 33 kHz, 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - USB Clock Domain, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



## 4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

| Name | Domain | Source | Desired Freq (MHz) | Nominal Freq (MHz) | Accuracy (%) | Start at Reset | Enabled |
|---|---|---|---|---|---|---|---|
| XTAL | DIGITAL | | 24 | 0 | ±0 | False | False |
| ILO | DIGITAL | | 0 | 0.1 | -55,+100 | True | True |
| PLL_OUT | DIGITAL | IMO | 45.158 | 45 | ±0.25 | True | True |
| IMO | DIGITAL | | 24 | 24 | ±0.25 | True | True |
| XTAL 32kHz | DIGITAL | | 0.0328 | 0 | ±0 | False | False |
| Digital Signal | DIGITAL | GenClock | 1.024 | 1.024 | ±0 | False | True |
| MASTER_CLK | DIGITAL | PLL_OUT | 0 | 45 | ±0.25 | True | True |
| BUS_CLK | DIGITAL | MASTER_CLK | 0 | 45 | ±0.25 | True | True |
| USB_CLK | DIGITAL | IMO | 48 | 48 | ±0.25 | False | True |

## 4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

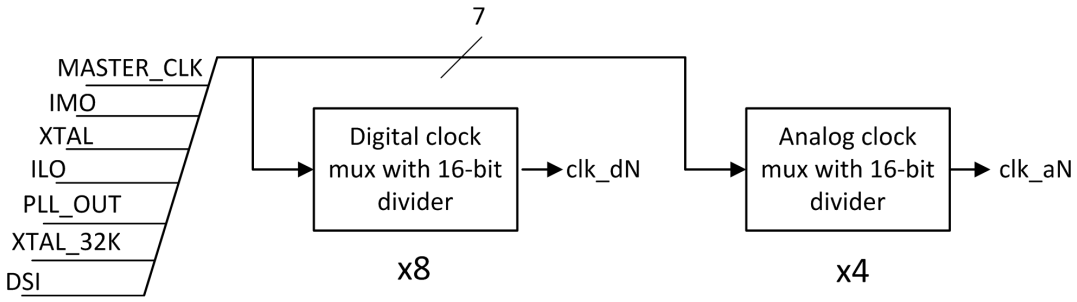



Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

| Name | Domain | Source | Desired Freq (MHz) | Nominal Freq (MHz) | Accuracy (%) | Start at Reset | Enabled |
|---|---|---|---|---|---|---|---|
| AudioClkGen_-Clock_SCK | DIGITAL | PLL_OUT | 0 | 11.25 | ±0.25 | True | True |
| AudioClkGen_-Clock_I2S | DIGITAL | PLL_OUT | 0 | 5.625 | ±0.25 | True | True |
| AudioClkGen_-Ref | DIGITAL | IMO | 0 | 24 | ±0.25 | True | True |
| ClkGenOut_Sync | DIGITAL | ILO | 0 | 0.1 | -55,+100 | True | True |
| Clock_CIC | DIGITAL | PLL_OUT | 0 | 1.875 | ±0.25 | True | True |
| USBFS_Cloc-k_vbus | DIGITAL | BUS_CLK | 0 | 45 | ±0.25 | True | True |

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

# 5 Interrupts and DMAs

## 5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 10. Interrupts

| Name | Priority | Vector |
|---|---|---|
| isr_InDMADone | 4 | 4 |
| isr_RxDMADone | 4 | 0 |
| isr_Tick | 7 | 5 |
| USBFS_arb_int | 7 | 22 |
| USBFS_bus_reset | 7 | 23 |
| USBFS_dp_int | 7 | 12 |
| USBFS_ep_0 | 7 | 24 |
| USBFS_ep_2 | 7 | 1 |
| USBFS_ep_4 | 7 | 2 |
| USBFS_ep_6 | 7 | 3 |
| USBFS_ord_int | 7 | 25 |
| USBFS_sof_int | 7 | 21 |

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

## 5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 11. DMAs

| Name | Priority | Channel Number |
|---|---|---|
| RxDMA | 0 | 0 |
| DMA_8to16 | 2 | 4 |
| USBFS_ep2 | 2 | 1 |
| USBFS_ep4 | 2 | 3 |
| USBFS_ep6 | 2 | 5 |
| USBInDMA | 3 | 2 |

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 5LP Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

# 6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

| Start Address | End Address | Protection Level |
|---|---|---|
| 0x0 | 0x3FFFF | U - Unprotected |

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

For more information on Flash memory and protection, please refer to:

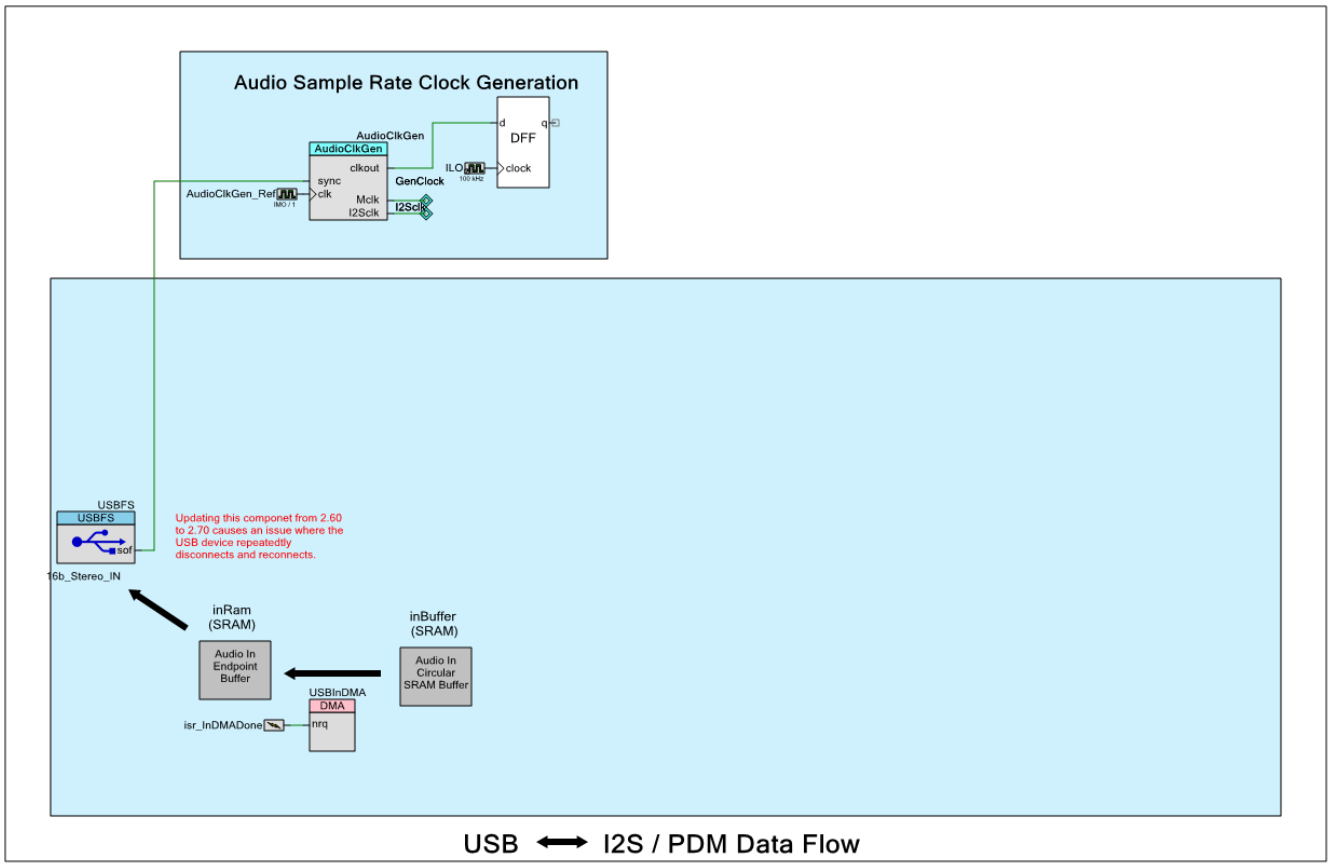
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

# 7 Design Contents

This design's schematic content consists of the following 8 schematic sheets:

## 7.1 Schematic Sheet: Digital_Audio

Figure 5. Schematic Sheet: Digital_Audio

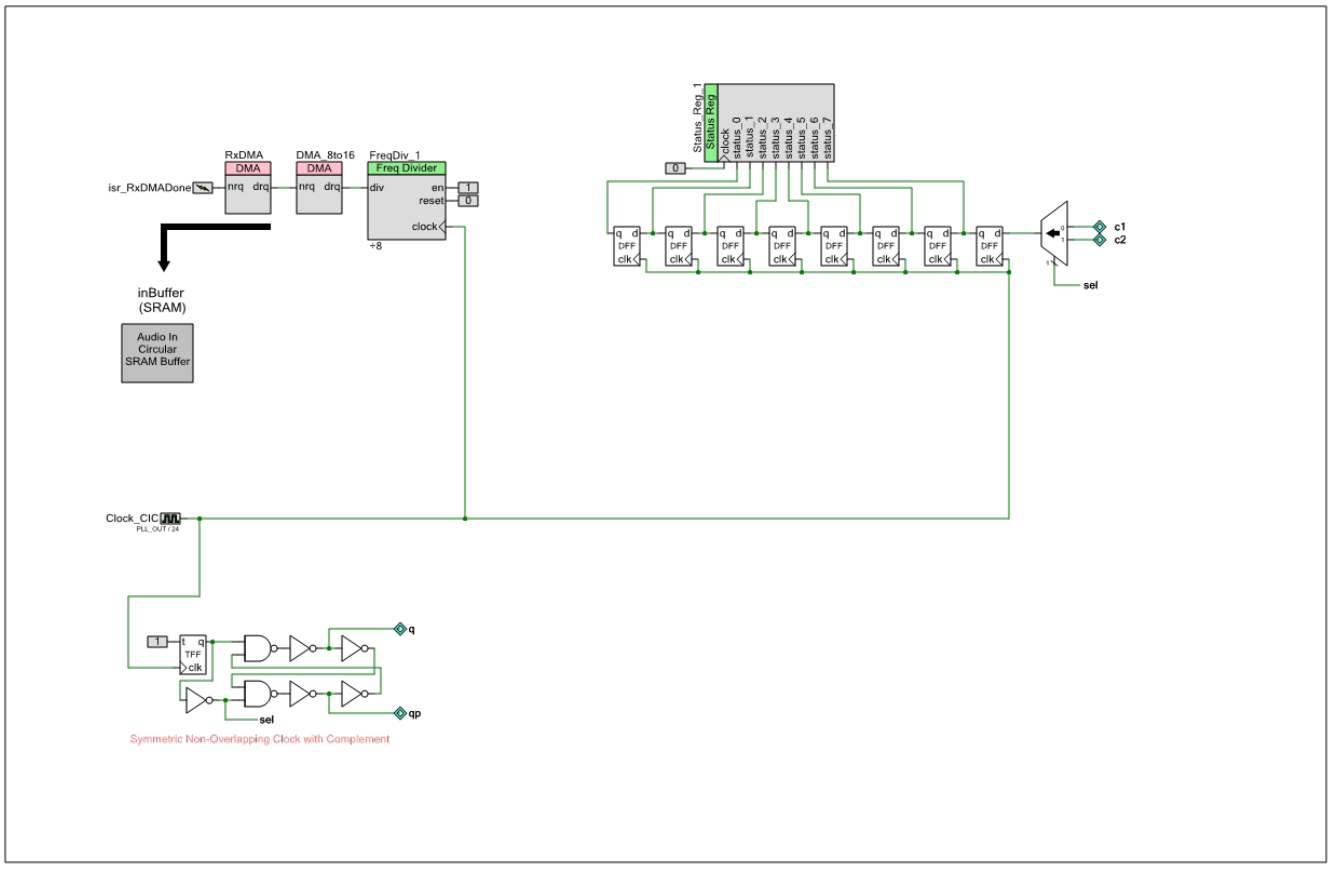



This schematic sheet contains the following component instances:

- Instance AudioClkGen (type: AudioClkGen_v0_83)
- Instance USBFS (type: USBFS_v2_60)

## 7.2 Schematic Sheet: Digital_Control

Figure 6. Schematic Sheet: Digital_Control

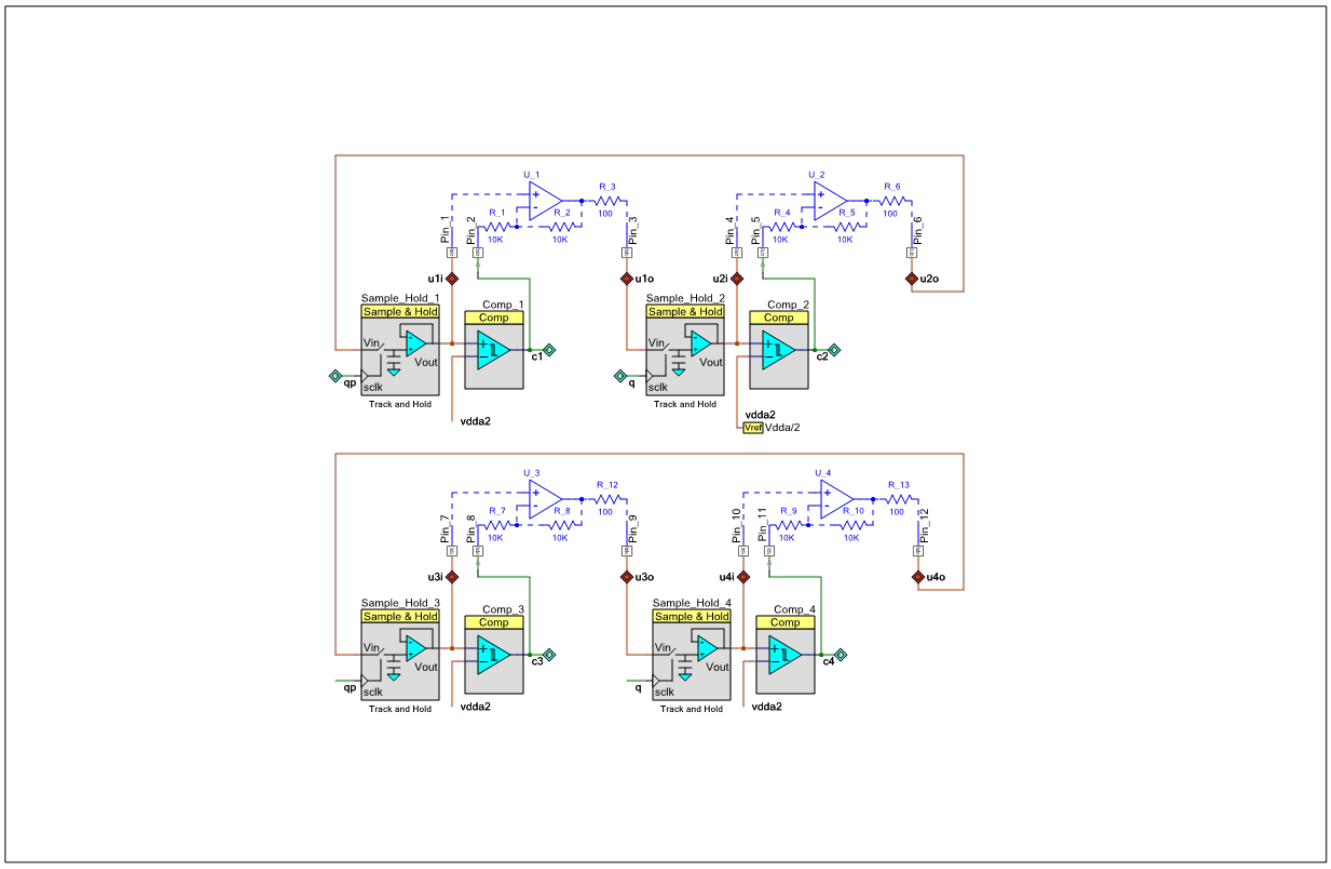



This schematic sheet contains the following component instances:

- Instance FreqDiv_1 (type: FreqDiv_v1_0)
- Instance Status_Reg_1 (type: CyStatusReg_v1_80)

## 7.3 Schematic Sheet: Analog

Figure 7. Schematic Sheet: Analog

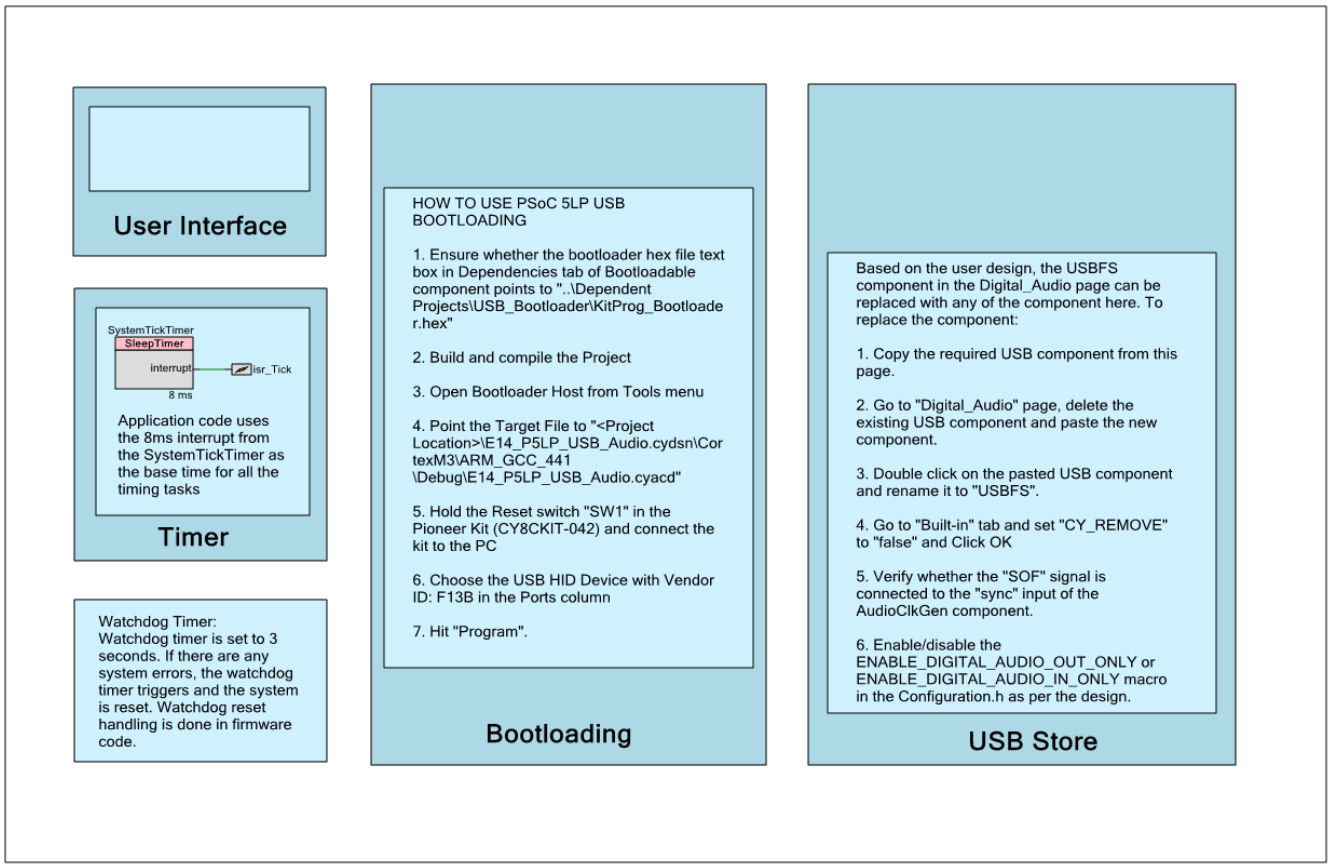



This schematic sheet contains the following component instances:

- Instance Comp_1 (type: Comp_v2_0)
- Instance Comp_2 (type: Comp_v2_0)
- Instance Comp_3 (type: Comp_v2_0)
- Instance Comp_4 (type: Comp_v2_0)
- Instance Sample_Hold_1 (type: Sample_Hold_v1_40)
- Instance Sample_Hold_2 (type: Sample_Hold_v1_40)
- Instance Sample_Hold_3 (type: Sample_Hold_v1_40)
- Instance Sample_Hold_4 (type: Sample_Hold_v1_40)

## 7.4 Schematic Sheet: Misc

Figure 8. Schematic Sheet: Misc

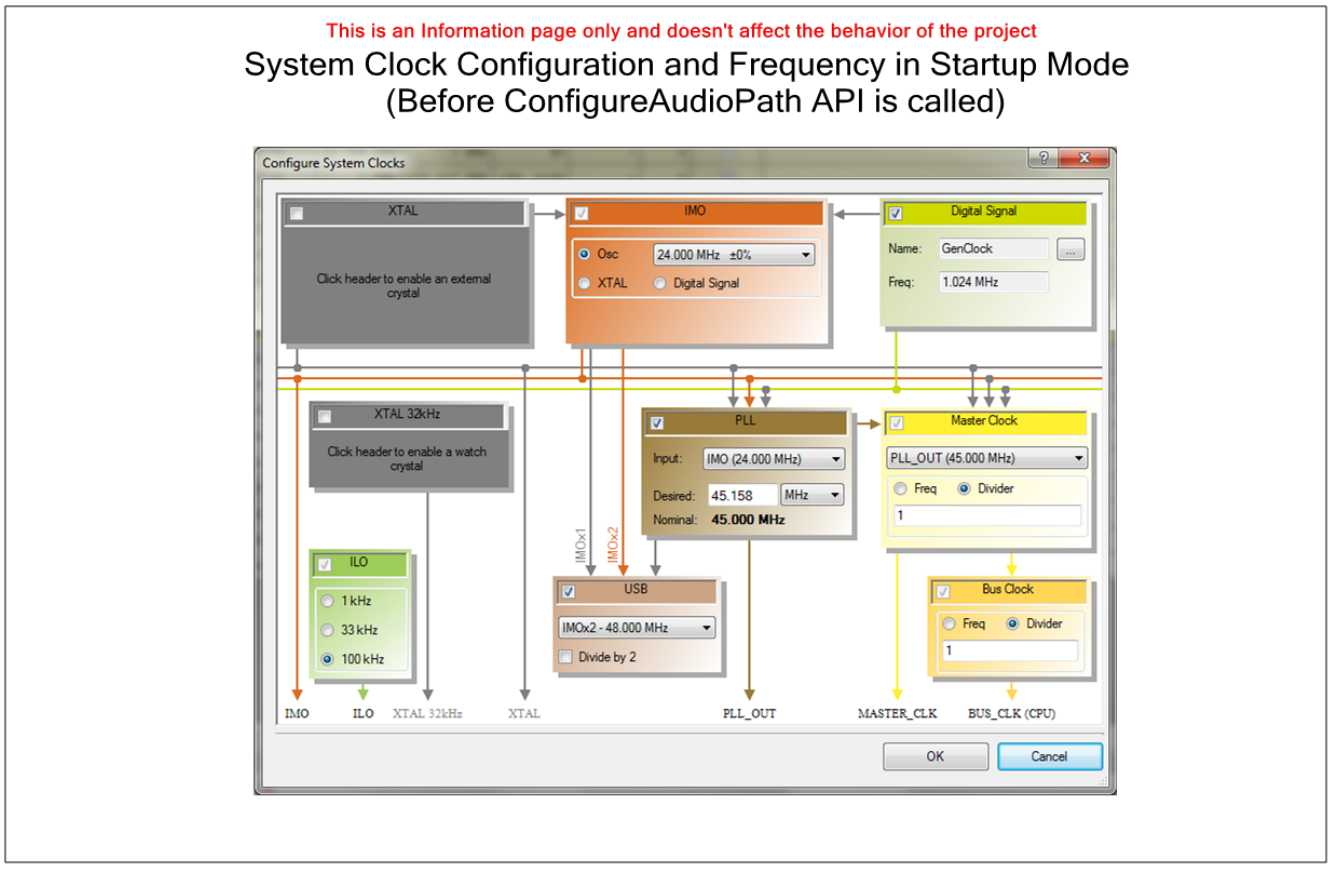



This schematic sheet contains the following component instances:

- Instance SystemTickTimer (type: SleepTimer_v3_20)

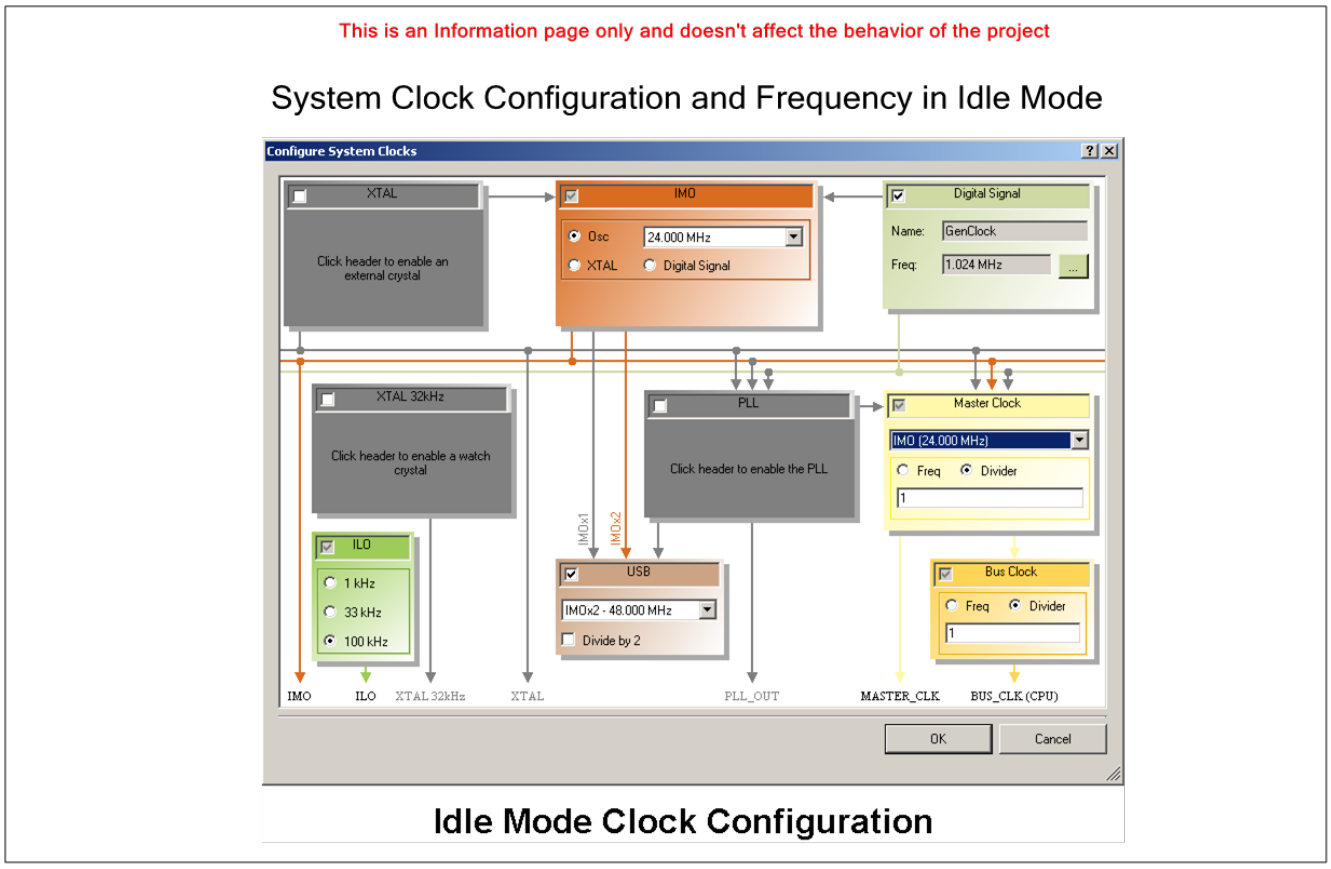
## 7.5 Schematic Sheet: Startup Mode Clock Info

Figure 9. Schematic Sheet: Startup Mode Clock Info



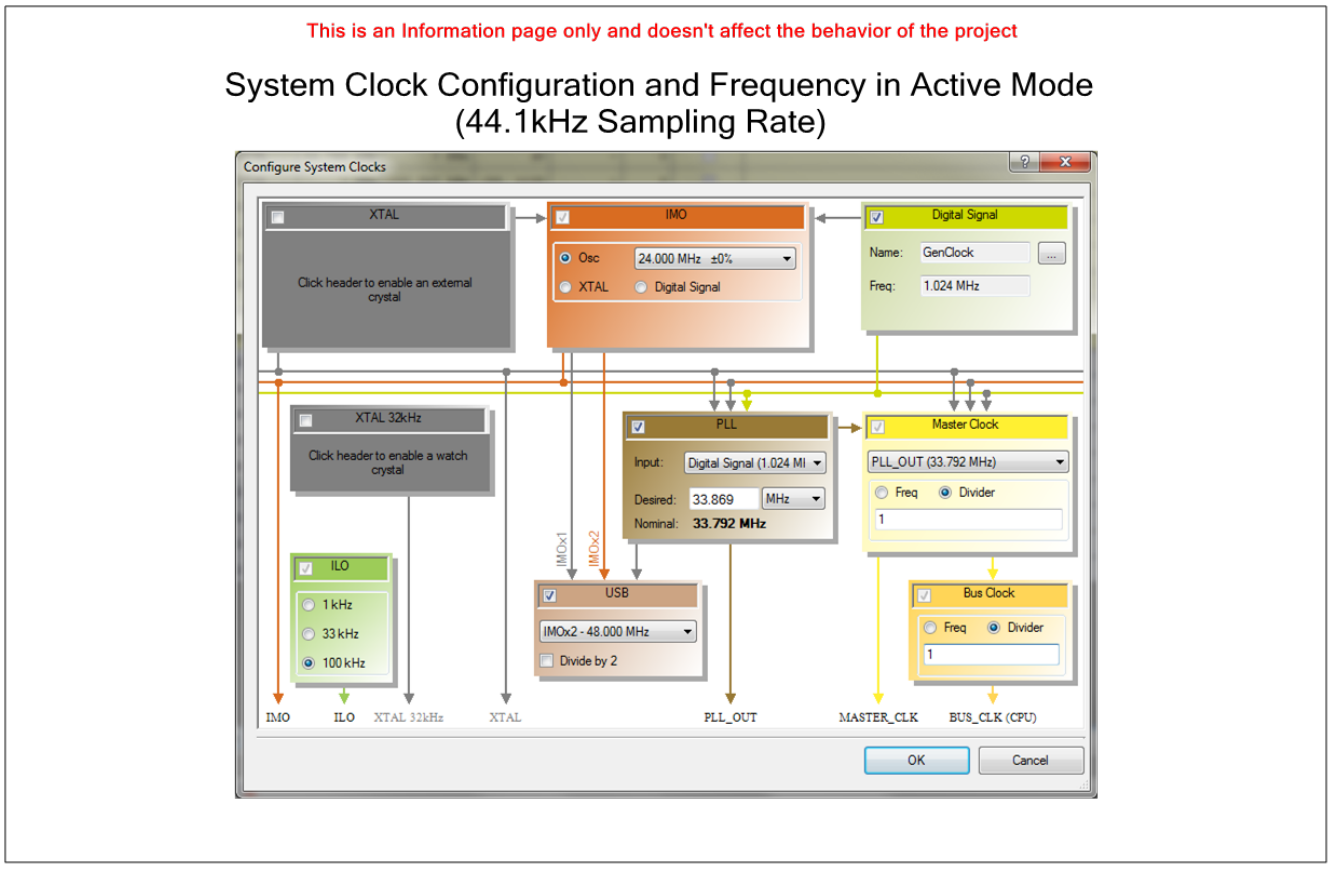
## 7.6 Schematic Sheet: Idle Mode Clock Info

Figure 10. Schematic Sheet: Idle Mode Clock Info



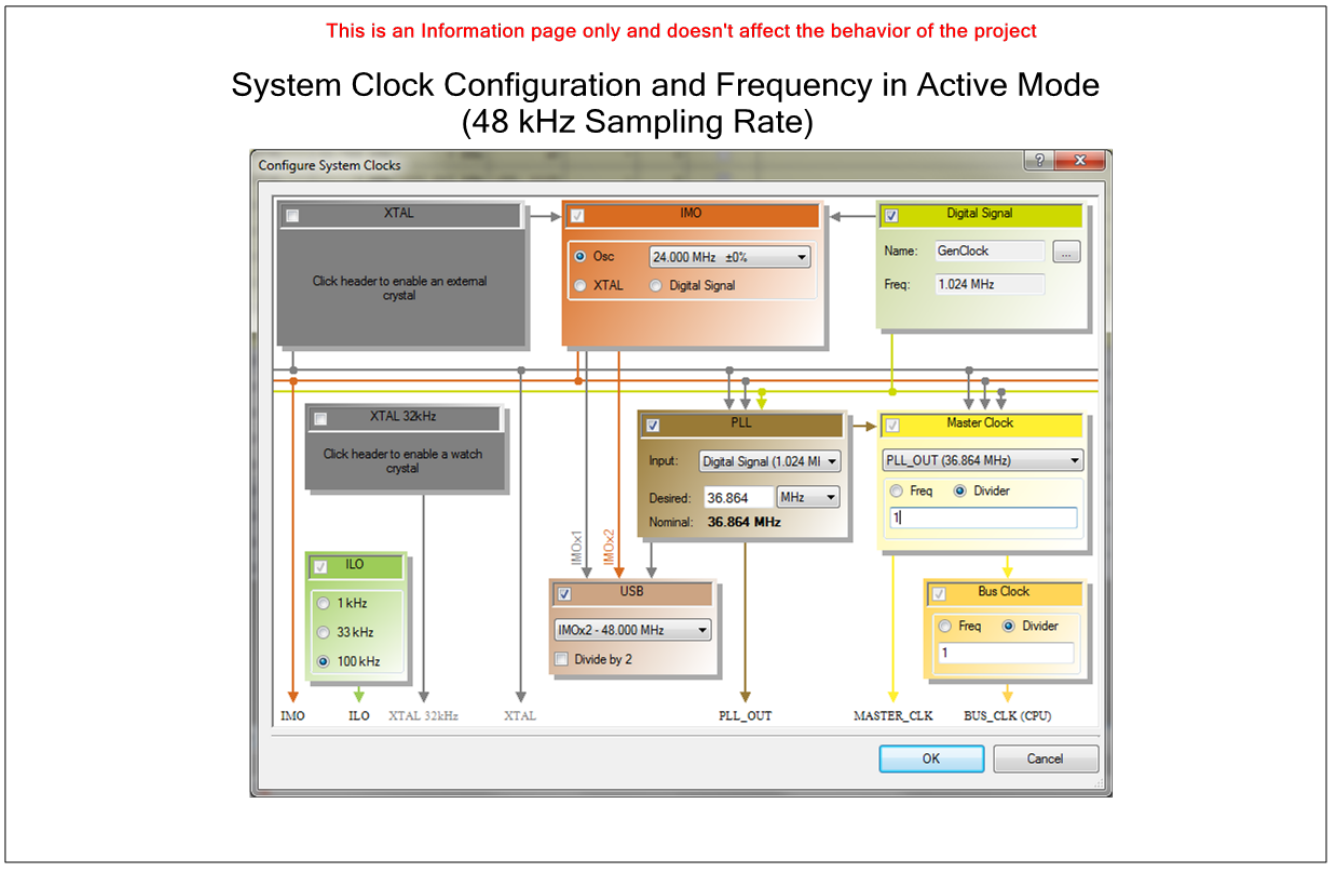
## 7.7 Schematic Sheet: Active Mode Clock 44.1kHz

Figure 11. Schematic Sheet: Active Mode Clock 44.1kHz



## 7.8 Schematic Sheet: Active Mode Clock 48kHz

Figure 12. Schematic Sheet: Active Mode Clock 48kHz



# 8 Components

## 8.1 Component type: AudioClkGen [v0.83]

### *8.1.1 Instance AudioClkGen*

**Description: (custom component)**
**Instance type: AudioClkGen [v0.83]**
**Datasheet: (not available)**

Table 13. Component Parameters for AudioClkGen

| Parameter Name | Value | Description |
|---|---|---|
| Enable_I2Sclk | true | |
| Enable_Mclk | true | |
| Enable_Sync | true | |

## 8.2 Component type: Comp [v2.0]

### *8.2.1 Instance Comp_1*

**Description: Analog voltage comparator.**
**Instance type: Comp [v2.0]**
**Datasheet: online component datasheet for Comp**

Table 14. Component Parameters for Comp_1

| Parameter Name | Value | Description |
|---|---|---|
| Hysteresis | Enable | Enable to add output hysteresis. |
| Pd_Override | Disable | Power down override to allow comparator to continue operating during sleep. |
| Polarity | Non Inverting | Allows output to be inverted. |
| Speed | Fast | Set comparator response speed. |
| Sync | Bypass | Allows synchronization with clock. |

### *8.2.2 Instance Comp_2*

**Description: Analog voltage comparator.**
**Instance type: Comp [v2.0]**
**Datasheet: online component datasheet for Comp**

Table 15. Component Parameters for Comp_2

| Parameter Name | Value | Description |
|---|---|---|
| Hysteresis | Enable | Enable to add output hysteresis. |
| Pd_Override | Disable | Power down override to allow comparator to continue operating during sleep. |
| Polarity | Non Inverting | Allows output to be inverted. |
| Speed | Fast | Set comparator response speed. |

| Parameter Name | Value | Description |
|---|---|---|
| Sync | Bypass | Allows synchronization with clock. |

### *8.2.3 Instance Comp_3*

**Description: Analog voltage comparator.**
**Instance type: Comp [v2.0]**
**Datasheet: online component datasheet for Comp**

Table 16. Component Parameters for Comp_3

| Parameter Name | Value | Description |
|---|---|---|
| Hysteresis | Enable | Enable to add output hysteresis. |
| Pd_Override | Disable | Power down override to allow comparator to continue operating during sleep. |
| Polarity | Non Inverting | Allows output to be inverted. |
| Speed | Fast | Set comparator response speed. |
| Sync | Bypass | Allows synchronization with clock. |

### *8.2.4 Instance Comp_4*

**Description: Analog voltage comparator.**
**Instance type: Comp [v2.0]**
**Datasheet: online component datasheet for Comp**

Table 17. Component Parameters for Comp_4

| Parameter Name | Value | Description |
|---|---|---|
| Hysteresis | Enable | Enable to add output hysteresis. |
| Pd_Override | Disable | Power down override to allow comparator to continue operating during sleep. |
| Polarity | Non Inverting | Allows output to be inverted. |
| Speed | Fast | Set comparator response speed. |
| Sync | Bypass | Allows synchronization with clock. |

## 8.3 Component type: CyStatusReg [v1.80]

### *8.3.1 Instance Status_Reg_1*

**Description: The Status Register allows the firmware to read values from digital signals.**
**Instance type: CyStatusReg [v1.80]**
**Datasheet: online component datasheet for CyStatusReg**

Table 18. Component Parameters for Status_Reg_1

| Parameter Name | Value | Description |
|---|---|---|
| Bit0Mode | Transparent | Bit Mode for Bit 0 of the Status Register |
| Bit1Mode | Transparent | Bit Mode for Bit 1 of the Status Register |
| Bit2Mode | Transparent | Bit Mode for Bit 2 of the Status Register |
| Bit3Mode | Transparent | Bit Mode for Bit 3 of the Status Register |
| Bit4Mode | Transparent | Bit Mode for Bit 4 of the Status Register |
| Bit5Mode | Transparent | Bit Mode for Bit 5 of the Status Register |
| Bit6Mode | Transparent | Bit Mode for Bit 6 of the Status Register |
| Bit7Mode | Transparent | Bit Mode for Bit 7 of the Status Register |
| BusDisplay | false | Displays the input terminals as bus |
| Interrupt | false | Shows the interrupt terminal |
| MaskValue | 0 | Defines the value of the interrupt mask |
| NumInputs | 8 | Defines the number of status inputs (1-8) |

## 8.4 Component type: FreqDiv [v1.0]

### *8.4.1 Instance FreqDiv_1*

**Description: Frequency Divider**
**Instance type: FreqDiv [v1.0]**
**Datasheet: online component datasheet for FreqDiv**

Table 19. Component Parameters for FreqDiv_1

| Parameter Name | Value | Description |
|---|---|---|
| Divider | 8 | The divider used to generate the div output from the clock input. |
| HighPulseTime | 2 | Number of clock cycles each clock period that the div output is high. 0 indicates 50% duty cycle. |

## 8.5 Component type: Sample_Hold [v1.40]

### *8.5.1 Instance Sample_Hold_1*

**Description: Sample/Track and Hold Amplifier**
**Instance type: Sample_Hold [v1.40]**
**Datasheet: online component datasheet for Sample_Hold**

Table 20. Component Parameters for Sample_Hold_1

| Parameter Name | Value | Description |
|---|---|---|
| Power | High Power | To select the device power |
| Sample_Clock_Edge | Negative | To select the clock edge |

| Parameter Name | Value | Description |
|---|---|---|
| Sample_Mode | Track and Hold | To select the mode of the device |
| Vref_Type | External | To select the Vref for Sample_Hold mode |

### *8.5.2 Instance Sample_Hold_2*

**Description: Sample/Track and Hold Amplifier**
**Instance type: Sample_Hold [v1.40]**
**Datasheet: online component datasheet for Sample_Hold**

Table 21. Component Parameters for Sample_Hold_2

| Parameter Name | Value | Description |
|---|---|---|
| Power | High Power | To select the device power |
| Sample_Clock_Edge | Negative | To select the clock edge |
| Sample_Mode | Track and Hold | To select the mode of the device |
| Vref_Type | External | To select the Vref for Sample_Hold mode |

### *8.5.3 Instance Sample_Hold_3*

**Description: Sample/Track and Hold Amplifier**
**Instance type: Sample_Hold [v1.40]**
**Datasheet: online component datasheet for Sample_Hold**

Table 22. Component Parameters for Sample_Hold_3

| Parameter Name | Value | Description |
|---|---|---|
| Power | High Power | To select the device power |
| Sample_Clock_Edge | Negative | To select the clock edge |
| Sample_Mode | Track and Hold | To select the mode of the device |
| Vref_Type | External | To select the Vref for Sample_Hold mode |

### *8.5.4 Instance Sample_Hold_4*

**Description: Sample/Track and Hold Amplifier**
**Instance type: Sample_Hold [v1.40]**
**Datasheet: online component datasheet for Sample_Hold**

Table 23. Component Parameters for Sample_Hold_4

| Parameter Name | Value | Description |
|---|---|---|
| Power | High Power | To select the device power |
| Sample_Clock_Edge | Negative | To select the clock edge |
| Sample_Mode | Track and Hold | To select the mode of the device |
| Vref_Type | External | To select the Vref for Sample_Hold mode |

## 8.6 Component type: SleepTimer [v3.20]

### *8.6.1 Instance SystemTickTimer*

**Description: The Sleep Timer component**
**Instance type: SleepTimer [v3.20]**
**Datasheet: online component datasheet for SleepTimer**

Table 24. Component Parameters for SystemTickTimer

| Parameter Name | Value | Description |
|---|---|---|
| EnableInt | true | Determines whether the sleep timer interrupt is enabled or disabled. |
| Interval | CTW_8_MS | Parameter that defines the wake up interval in milliseconds. |

## 8.7 Component type: USBFS [v2.60]

### *8.7.1 Instance USBFS*

**Description: USB 2.0 Full Speed Device Framework**
**Instance type: USBFS [v2.60]**
**Datasheet: online component datasheet for USBFS**

Table 25. Component Parameters for USBFS

| Parameter Name | Value | Description |
|---|---|---|
| EnableCDCApi | false | Enables additional high level API's that allow the CDC device to be used similar to a UART device. |
| EnableMidiApi | false | Enables additional high level MIDI API's. |
| endpointMA | MA_Static | Endpoint memory allocation |
| endpointMM | EP_DMAauto | Endpoint memory management |
| extern_cls | false | This parameter allows for user or other component to implement his own handler for Class requests. USBFS_DispatchClassRqst() function should be implemented if this parameter enabled. |
| extern_vbus | false | This parameter enables external VBUSDET input. |
| extern_vnd | false | This parameter allows for user or other component to implement his own handler for Vendor specific requests. USBFS_HandleVendorRqst() function should be implemented if this parameter enabled. |
| extJackCount | 0 | Max number of External MIDI IN Jack or OUT Jack descriptors |
| max_interfaces_num | 3 | Defines maximum interfaces number |

| Parameter Name | Value | Description |
|---|---|---|
| Mode | false | Specifies whether the implementation will create API for interfacing to UART component(s) for a corresponding set of external MIDI connections. |
| mon_vbus | false | The mon_vbus parameter adds a single VBUS monitor pin to the design. This pin must be connected to VBUS and must be assigned in the pin editor. |
| out_sof | true | The out_sof parameter enables Start-of-Frame output. |
| Pid | F232 | Product ID |
| Vid | 04B4 | Vendor ID |

# 9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine