RV32IC Pipelined implementation

Computer Architecture

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### **Project Description:**

The femtoRV32 project involves implementing a pipelined RISC-V processor (RV32I) in Verilog for the Nexys A7 FPGA. It supports all 42 user-level RV32I instructions, excluding ECALL, EBREAK, PAUSE, FENCE, and FENCE.TSO, with ECALL treated as a halting instruction and the others as no-ops. The processor uses a single-ported memory for both instructions and data, with a 2-cycle instruction issue to handle memory access hazards. The project includes hazard handling, test cases, and bonus features like compressed instruction support and a test program generator. The final deliverables include Verilog code, test programs, and this report detailing the design and testing process.

#### **Problems and solutions:**

The single memory was the most challenging part to implement since it takes distinct data and instructions and puts them in the same port, we just had to differentiate them by fetching one at a positive edge and the other at a negative edge. It also forced us to accept the trade off and make our program has an average CPI of 2 to handle the structural hazards that came with this. Changing from our code that was implemented in the lab was also a bit challenging since there was different hazards and stages handled in the lab that we no longer needed such as forwarding from the MEM/WB stage.

#### **Test Cases:**

### Testing all I instructions

addi x1,x0,-32

addi x2,x0,44

addi x31,x0,2

addi x25,x0,2

add x2,x2,x1

sub x2,x1,x2

xor x3,x2,x1

or x4,x3,x1

and x5,x4,x1

sll x5,x5,x25

srl x6,x5, x25

sra x7,x6,x25

slt x8,x7,x25

sltu x9,x8,x25

addi x10,x9,5

xori x11, x10,5

ori x12,x11,2

andi x13,x12,2

slli x14,x13,2

srli x15,x14,2

srai x16,x15,2

slti x17,x16,2

sltiu x18,x17,2 Waveform Output:

				460.166 ns			
Name	Value		440.000 ns	460.000 ns	<sup>480.000 ns</sup>	500.000 ns	520.000
<b>¼</b> ssdClk	0						
∨ 💖 regfile[31:0][31:0]	2,0,0,0,0,0,2,0,0,0,0	2,0,0,0,0,0,2,0,0,0,0,0,0,	1,1,0,2,8,2,3,	3,6,1,0,26843	5448,107374179	2,-12	
> 😽 [31][31:0]	2		2			<del></del>	
> 😽 [30][31:0]	0		0				
> 🐶 [29][31:0]	0		0				
> 😽 [28][31:0]	0		0			<del></del>	
> 🛂 [27][31:0]	0		0				
> 💖 [26][31:0]	0		0				
> 💖 [25][31:0]	2		2			<del></del>	
> 🐶 [24][31:0]	0		0				
> 💖 [23][31:0]	0		0				
> 🐶 [22][31:0]	0		0				
> 😽 [21][31:0]	0		0			<del></del>	
> 😽 [20][31:0]	0		0				
> 🕨 [19][31:0]	0		0				
> 🐶 [18][31:0]	1		1				
> 🕨 [17][31:0]	1		1				
> 🕨 [16][31:0]	0		0				
> 😽 [15][31:0]	2		2				
> 🕨 [14][31:0]	8		8				
> 🐶 [13][31:0]	2		2				
> 🚺 [12][31:0]	3		3				
> 🕨 [11][31:0]	3		3				
> 🕨 [10][31:0]	6		6				
> 🚺 [9][31:0]	1		1			<b></b>	
> 🚺 [8][31:0]	0		0			<del></del>	
> 🛂 [7][31:0]	268435448		2684354	48		<del></del>	
> 6 [6][31:0]	1073741792		1073741	92		$\longrightarrow$	
> 🚺 [5][31:0]	-128		-128			$\blacksquare$	
> 🕨 [4][31:0]	-12		-12			<del></del>	
> 🕨 [3][31:0]	52		52			<del></del>	
> 🐶 [2][31:0]	-44		-44				
> ♥ [1][31:0]	-32		-32				
> ▼ [0][31:0]	0		0				
* * /							

# **Benchmark Output**

Init Value	Register	Decimal	Hex	Binary
0	x0 (zero)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeeee
0	x1 (ra)	-32	0xffffffe0	0b11111111111111111111111111100000
0	x2 (sp)	-44	0xffffffd4	0b1111111111111111111111111111010100
0	x3 (gp)	52	0x00000034	0b0000000000000000000000000000000000000
0	x4 (tp)	-12	0xfffffff4	0b1111111111111111111111111111110100
0	x5 (t0)	-128	0xffffff80	0b1111111111111111111111110000000
0	x6 (t1)	1073741792	0x3fffffe0	0b001111111111111111111111111100000
0	x7 (t2)	268435448	0x0ffffff8	0b00001111111111111111111111111000
0	x8 (s0/fp)	0	0x00000000	000000000000000000000000000000000000000
0	X9 (S1)	1	0x00000001	000000000000000000000000000000000000000
0	x10 (a0)	6	0x00000006	050000000000000000000000000000000000000
0	X11 (a1)	3	0x00000003	0b0000000000000000000000000000000000000
0	x12 (a2)	3	0x00000003	000000000000000000000000000000000000000
0	x13 (a3)	2	0x00000002	000000000000000000000000000000000000000
0	x14 (a4)	8	0x00000008	000000000000000000000000000000000000000
0	x15 (a5)	2	0x00000002	000000000000000000000000000000000000000
0	x16 (a6)	0	0x00000000	000000000000000000000000000000000000000
0	x17 (a7)	1	0x00000001	000000000000000000000000000000000000000
0	X18 (S2)	1	0x00000001	000000000000000000000000000000000000000
0	X19 (S3)	0	0x00000000	000000000000000000000000000000000000000
0	X20 (S4)	0	0x00000000	050000000000000000000000000000000000000
0	X21 (S5)	0	0x00000000	000000000000000000000000000000000000000
0	X22 (S6)	0	0x00000000	050000000000000000000000000000000000000
0	X23 (S7)	0	0x00000000	000000000000000000000000000000000000000
0	X24 (S8)	0	0x00000000	000000000000000000000000000000000000000
0	X25 (S9)	2	0x00000002	000000000000000000000000000000000000000
0	X26 (S10)	0	0x00000000	000000000000000000000000000000000000000
0	X27 (S11)	0	0x00000000	050000000000000000000000000000000000000
0	x28 (t3)	0	0x00000000	050000000000000000000000000000000000000
0	x29 (t4)	0	0x00000000	050000000000000000000000000000000000000
0	x30 (t5)	0	0x00000000	050000000000000000000000000000000000000
0	x31 (t6)	2	0x00000002	000000000000000000000000000000000000000

## Testing store and load instructions

li x1,0x7f7f4f2

li x2,0x7f1

li x9,4

sw x1,0(x0)

sw x2,0(x9)

lw x5,4(x0)

 $1b \times 6,6(x0)$ 

Ibu x7,5(x0)

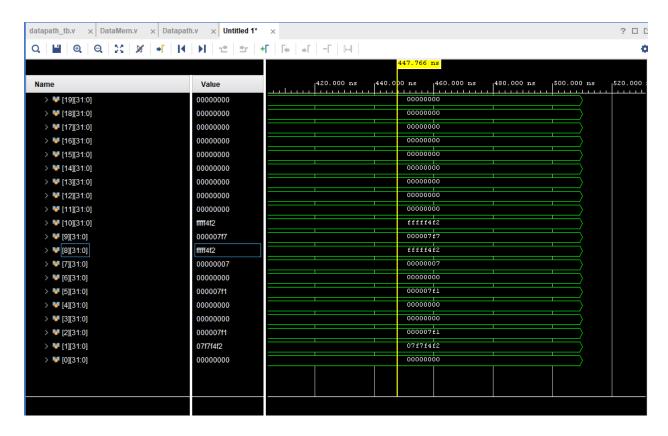
Ih x8,0(x0)

lhu x9,2(x0)

sh x1, 2(x0)

lh x10, 2(x0)

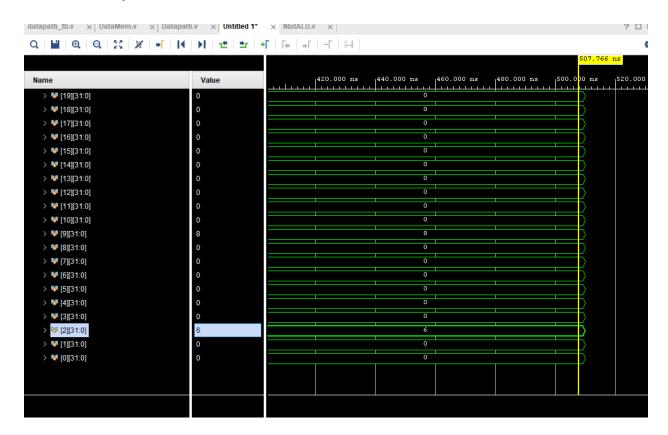
## **Waveform Output:**



# **Testing Branch instructions**

beq x0,x1,8 addi x1,x1,4 blt x1,x2,8 addi x2,x2,6 bge x2,x1,8 addi x3,x3,5 bne x2,x3,8 addi x10,x10,10 addi x9,x9,8

#### **Waveform Output:**

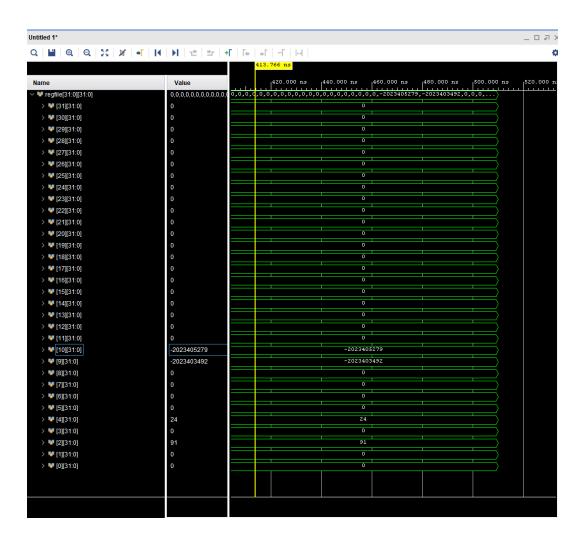


# **Benchmark Output:**

Init Value	Dogistor	Desimal	Llav	Dinant
Init Value	Register	Decimal	Hex	Binary
9	x0 (zero)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeeeee
0	x1 (ra)	0	0x00000000	@b@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
0	x2 (sp)	6	0x00000006	050000000000000000000000000000000000000
0	x3 (gp)	0	0x00000000	000000000000000000000000000000000000000
0	x4 (tp)	0	0x00000000	ebeeeeeeeeeeeeeee
0	x5 (t0)	0	0x00000000	ebeeeeeeeeeeeeeeeeee
0	x6 (t1)	0	0x00000000	ebeeeeeeeeeeeeeee
0	x7 (t2)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeeee
0	x8 (s0/fp)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeee
0	x9 (s1)	8	0x00000008	0b000000000000000000000000000000000000
0	x10 (a0)	0	0x00000000	000000000000000000000000000000000000000
0	x11 (a1)	0	0x00000000	@beeeeeeeeeeeeeeeeeeeee
0	x12 (a2)	0	0x00000000	@b@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
0	x13 (a3)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeeeeee
0	x14 (a4)	0	0x00000000	@beeeeeeeeeeeeeeeeeeeeeeeee
0	x15 (a5)	0	0x00000000	©beeeeeeeeeeeeeeeee
0	x16 (a6)	0	0x00000000	@beeeeeeeeeeeeeeeeeeeeeeeee
0	x17 (a7)	0	0x00000000	©beeeeeeeeeeeeeeeee
0	X18 (S2)	0	0x00000000	©beeeeeeeeeeeeeeeeeee
0	x19 (s3)	0	0x00000000	6peeeeeeeeeeeeeeeeeeeeeee
0	X20 (S4)	0	0x00000000	ebeeeeeeeeeeeeeeee
0	X21 (S5)	0	0x00000000	ebeeeeeeeeeeeeee
0	X22 (S6)	0	0x00000000	ebeeeeeeeeeeeeee
0	X23 (S7)	0	0x00000000	0b000000000000000000000000000000000000
0	X24 (58)	0	0x00000000	0b000000000000000000000000000000000000
0	X25 (S9)	0	0x00000000	0b000000000000000000000000000000000000
0	X26 (S10)	0	0x00000000	0b000000000000000000000000000000000000
0	X27 (S11)	0	0x00000000	ebeeeeeeeeeeeeeee
0	x28 (t3)	0	0x00000000	0b000000000000000000000000000000000000
0	x29 (t4)	0	0x00000000	ebeeeeeeeeeeeeeeee
0	x30 (t5)	0	0x00000000	ebeeeeeeeeeeeeeeeeee
0	x31 (t6)	0	0x00000000	@heeeeeeeeeeeeeeeeeeeeeeeeeeeee

# **Testing JAL, JALR, AUIPC, LUI**

lui x10,0x87655 addi x10,x10,10 jal x0,8 addi x10,x0,53 addi x2,x0,91 jalr x4,x0,28 addi x5,x0,20 auipc x9,0x87655



# Benchmark:

Init Value	Register	Decimal	Hex	Binary
0	x0 (zero)	0	0x00000000	000000000000000000000000000000000000000
0	x1 (ra)	0	0x00000000	000000000000000000000000000000000000000
0	x2 (sp)	91	0x0000005b	0b0000000000000000000000000000000000000
0	x3 (gp)	0	0x00000000	000000000000000000000000000000000000000
0	x4 (tp)	24	0x00000018	0b0000000000000000000000000000000000000
0	x5 (t0)	0	0x00000000	000000000000000000000000000000000000000
0	x6 (t1)	0	0x00000000	000000000000000000000000000000000000000
0	x7 (t2)	0	0x00000000	000000000000000000000000000000000000000
0	x8 (s0/fp)	0	0x00000000	000000000000000000000000000000000000000
0	X9 (S1)	-2023403492	0x8765501c	0b10000111011001010101000000011100
0	x10 (a0)	-2023403510	0x8765500a	0b10000111011001010101000000001010
0	X11 (a1)	0	0x00000000	000000000000000000000000000000000000000
0	X12 (a2)	0	0x00000000	000000000000000000000000000000000000000
0	x13 (a3)	0	0x00000000	000000000000000000000000000000000000000
0	X14 (a4)	0	0x00000000	000000000000000000000000000000000000000
0	x15 (a5)	0	0x00000000	000000000000000000000000000000000000000
0	x16 (a6)	0	0x00000000	000000000000000000000000000000000000000
0	X17 (a7)	0	0x00000000	000000000000000000000000000000000000000
0	X18 (S2)	0	0x00000000	000000000000000000000000000000000000000
0	X19 (S3)	0	0x00000000	000000000000000000000000000000000000000
0	X20 (S4)	0	0x00000000	000000000000000000000000000000000000000
0	X21 (S5)	0	0x00000000	000000000000000000000000000000000000000
0	X22 (S6)	0	0x00000000	000000000000000000000000000000000000000
0	X23 (S7)	0	0x00000000	000000000000000000000000000000000000000
0	X24 (S8)	0	0x00000000	000000000000000000000000000000000000000
0	X25 (S9)	0	0x00000000	000000000000000000000000000000000000000
0	X26 (S10)	0	0x00000000	000000000000000000000000000000000000000
0	X27 (S11)	0	0x00000000	000000000000000000000000000000000000000
0	x28 (t3)	0	0x00000000	000000000000000000000000000000000000000
0	x29 (t4)	0	0x00000000	000000000000000000000000000000000000000
0	x30 (t5)	0	0x00000000	ebeeeeeeeeeeeeeeeeeeee

# Datapath:

Notes: All necessary shifts have been made in the imm ge

