Memory

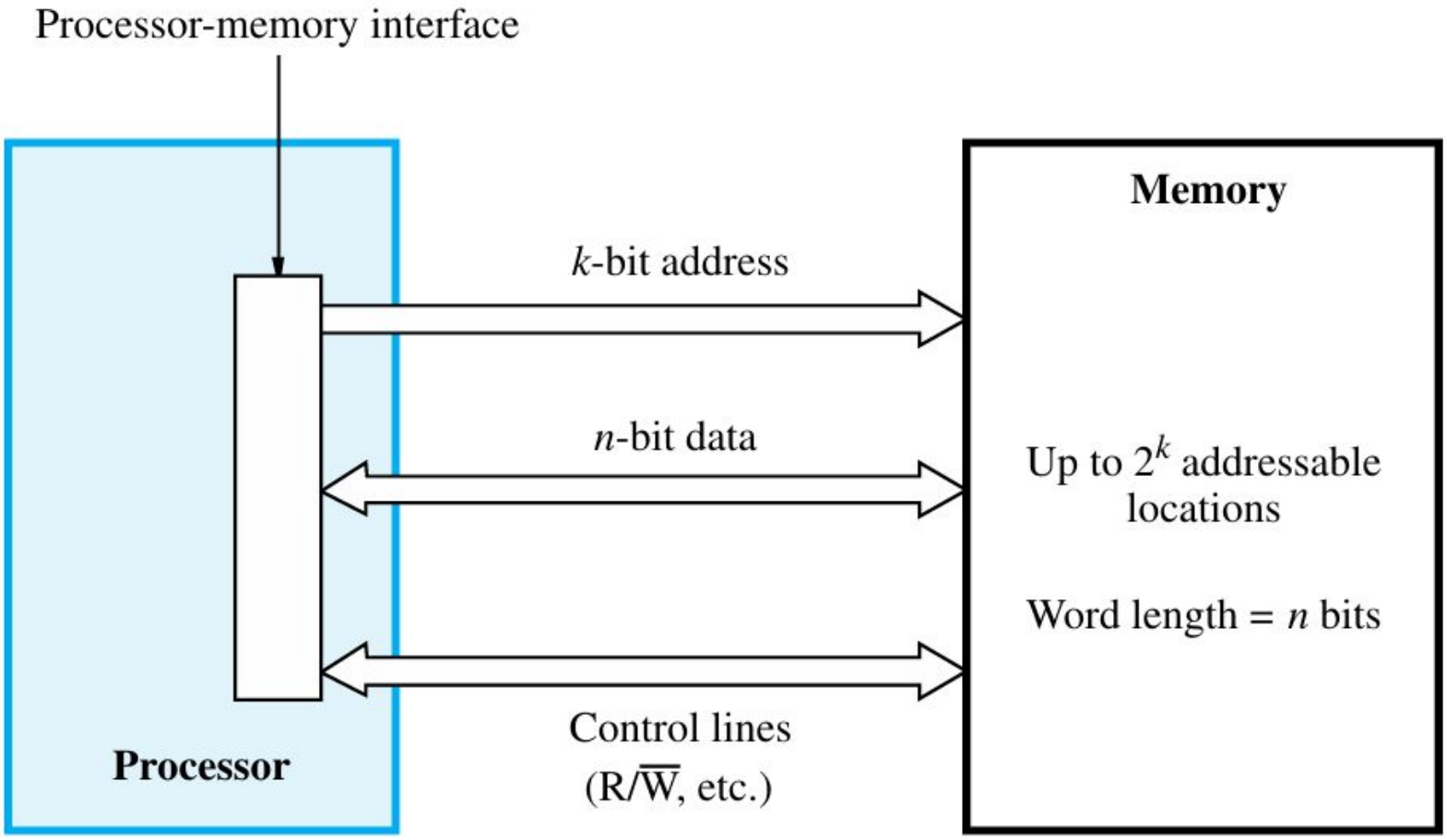

Figure 8.1 Connection of the memory to the processor.

Some basic concepts

- **memory access time-** between the initiation of an operation to transfer a word of data and the completion of that operation. This is referred to as the
- **memory cycle time**, which is the minimum time delay required between the initiation of two successive memory operations, for example, the time between two successive Read operations.
- A memory unit is called a **random-access memory** (RAM) if the access time to any location is the same, independent of the location's address. Main memory is RAM.
- Cache memory: The processor of a computer can usually process instructions and data faster than they can be fetched from the main memory. Hence, the memory access time is the bottleneck in the system. One way to reduce the memory access time is to use a cache memory. This is a small, fast memory inserted between the larger, slower main memory and the processor. It holds the currently active portions of a program and their data.

- An important design issue is to provide a computer system with as large and fast a memory as possible, within a given cost target.

- Several techniques to increase the effective size and speed of the memory:
  - Cache memory (to increase the effective speed).
  - Virtual memory (to increase the effective size).

Organization of memory cells in a ***16 x 8*** memory chip

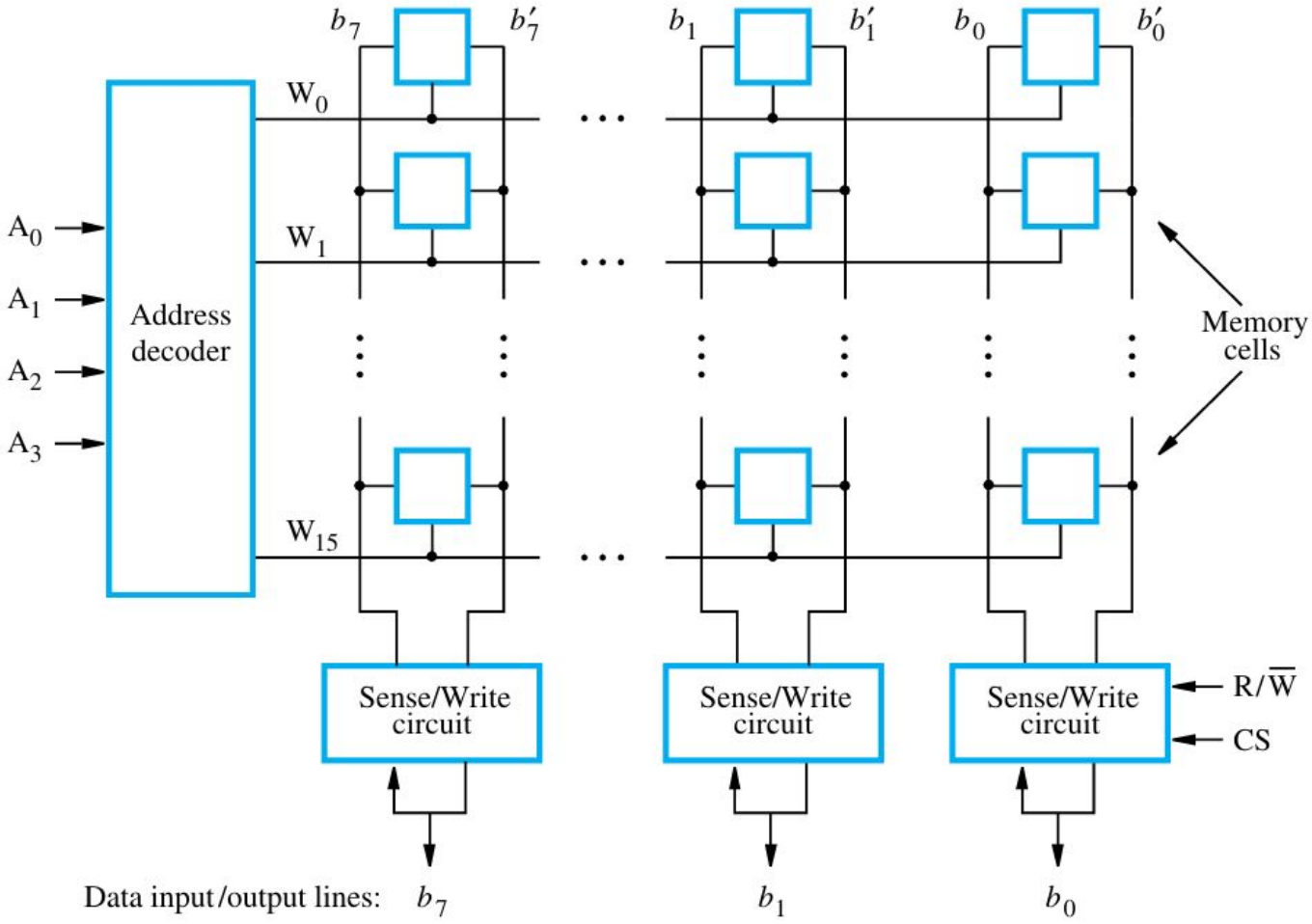

Figure 8.2 Organization of bit cells in a memory chip.

Internal organization of memory cells

- Each memory cell can hold 1 bit of information
- Memory cells are organized in the form of an array
- One row is one memory word
- All cells of a row are connected to a common line, known as the word line
- Word line is connected to the address decoder
- Sense/write circuits are connected to the data input/output lines of the memory chip.

No. of external pins required to connect a memory chip

For 16x8 chip:

- 4 address lines
- 8 data lines
- 2 control lines (R/W’, CS)
- 2 power lines (Power supply, ground)
- Total lines: 16

Organization of memory cells in 1Kx1 memory chip

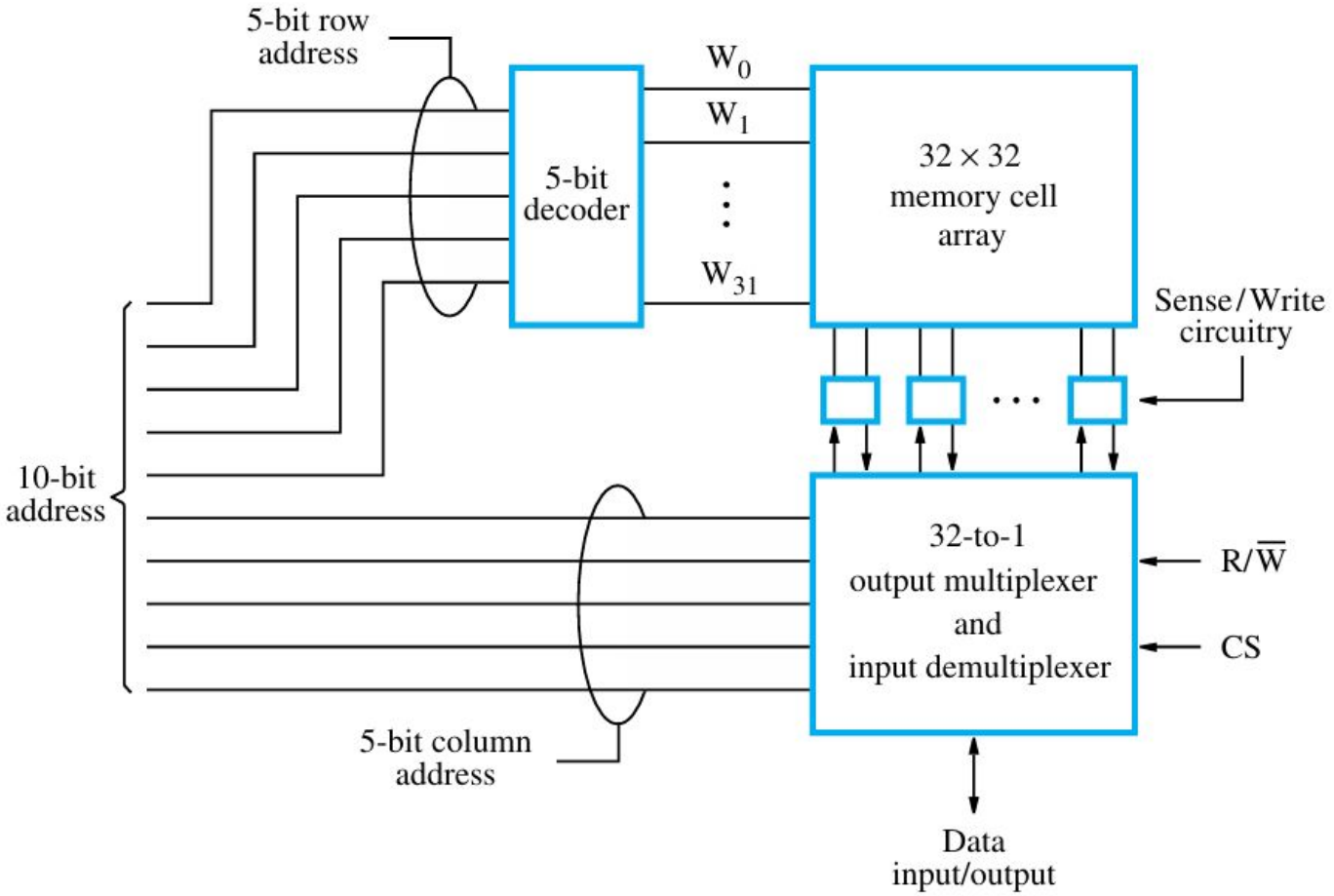

Figure 8.3 Organization of a 1K × 1 memory chip.

SRAM – Static Random Access Memory

- Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.

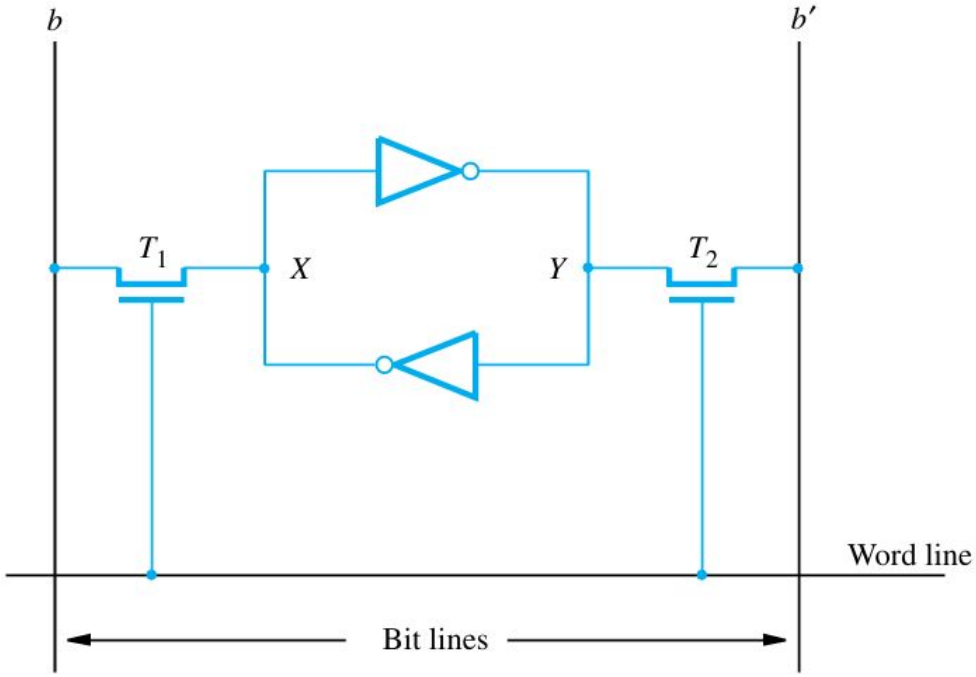

Figure 8.4 A static RAM cell.

- Two inverters are cross-connected to form the basic storage element 'latch'.
- The latch is connected to two bit lines *b and b'* and one word line by transistors T1 and T2.
- These transistors can be opened or closed under control of the word line. When the word line is at ground level, the transistors are turned off and the latch retains its state.

- Cross-coupled inverters in SRAM cells are used **to create a stable, latch-like structure that holds the stored data (0 or 1) reliably, even without constant power or refreshing**, due to the positive feedback between the two inverters.

Here's a more detailed explanation:

Data Storage:

- The core of an SRAM cell consists of two cross-coupled inverters, which act as a latch.

Positive Feedback:

- **The output of each inverter is connected to the input of the other, creating a positive feedback loop. This feedback ensures that once a stable state (0 or 1) is established, it will be maintained.**

Stability:

- This latch-like behavior allows SRAM to store data without the need for constant refreshing, unlike DRAM.

Read operation at SRAM cell

- The Sense/Write circuit at the end of the two bit lines monitors the state of b and b’ and set the output accordingly.
- In order to read the state of the SRAM cell, the word line is activated to close switches T1 and T2.
- If the cell is in state 1, the signal on bit line b is high and the signal on bit line b’ is low. The opposite is true if the cell is in state 0. Thus, b and b are always complements of each other.

Write operation at SRAM cell

- The state of the cell is set by placing the appropriate value on bit line b and its complement on b’, and then activating the word line
- This forces the cell into the corresponding state.
- The cell will retain its state when the word line is deactivated.

DRAM – Dynamic RAM

- DRAM: slow, cheap and dense memory
- Typical choice for main memory
- Cell consists of: 1 transistor and 1 capacitor
- Bits are stored as charge on capacitor. The charge can be retained for only tens of milliseconds
- To retain the information for a longer time: **periodically refreshes the capacitor by restoring the capacitor charge** to its full value

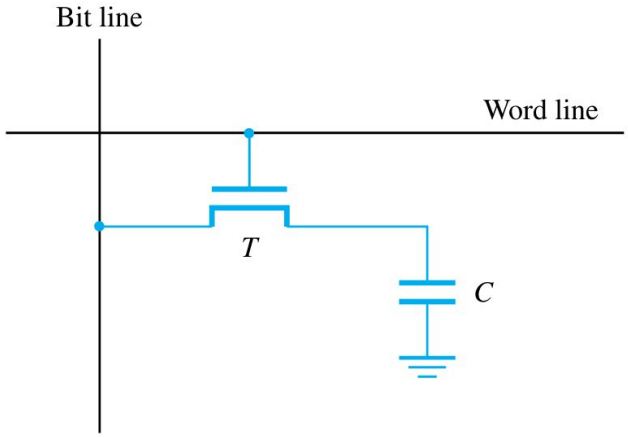

Figure 8.6 A single-transistor dynamic memory cell.

Periodic refreshing is required, bcos after the transistor is turned off, capacitor begins to discharge, due to

- 1. capacitors own leakage resistance
- 2. The transistor conduct a tiny amount of current measured in picoamperes, after it is turned off.

How periodic refresh operation is performed?

- During **a read operation**, the transistor in a selected cell is turned on.
- A sense amplifier connected to the bit line detects whether the charge stored on the capacitor is above the threshold value
- If so, it drives the bit line to a full voltage that represents logic value 1. This voltage recharges the capacitor to the full charge that corresponds to logic value 1.
- If the sense amplifier detects that the charge on the capacitor is below the threshold value, it pulls the bit line to ground level, which ensures that the capacitor will have no chrge, representing logic value 0.
- Hence, reading the contents of the cell automatically refreshes its contents.

Write Operation

1. Activate the word line
2. Transistor in selected cell is turned ON
3. Capacitor gets charged to the voltage supplied to bit line

Read Operation

1. Activate the word line
2. Transistor in selected cell is turned ON
3. Cell and bit line share charges
   - Capacitor > threshold voltage, bit line = 1
   - Capacitor < threshold voltage, bit line = 0

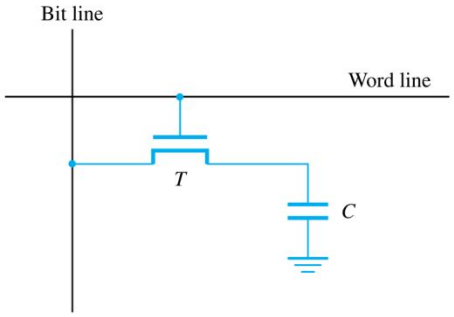

Figure 8.6 A single-transistor dynamic memory cell.

SRAM vs DRAM

	SRAM	DRAM
1	Transistors are used to store information in SRAM	Capacitors are used to store information
2	SRAM does not need periodic refreshment to maintain the logic state	DRAM needs periodic refreshment to maintain the logic state
3	SRAM is faster than DRAM	DRAM is slower than SRAM
4	Less storage capacity – low density devices	It has large storage capacity – high density devices
5	More expensive than DRAM	Cheaper than SRAM
6	Power consumption is more	Power consumption is less
7	Used in cache memory	Used in main memory

Asynchronous DRAM and Synchronous DRAM

- Synchronous DRAM uses the system clock to coordinate the memory access while asynchronous DRAM does not use the system clock to coordinate the memory access.

Designing 16Megabit Asynchronous DRAM as 2M x 8

- Configure **16Megabit** as 2Mx8 memory
- Cells are organized as 4K x 4K array.
- There are 4096 rows. Each row consists of 4096 cells. This are divided into 512 groups of 8 bits each. ie, a row will have 512 bytes.
- To select a row, 12 address bits are required. To select a byte in the row, 9 address bits are required. Thus 21 address bits are required to specify a byte.
- Higher order 12 bits specify row, lower order 9 bits specify byte

- First apply the row address RAS signal latches the row address. Then apply the column address, CAS signal latches the address.
- Timing of the memory unit is controlled by a specialized unit which generates RAS and CAS.
- This is asynchronous DRAM.

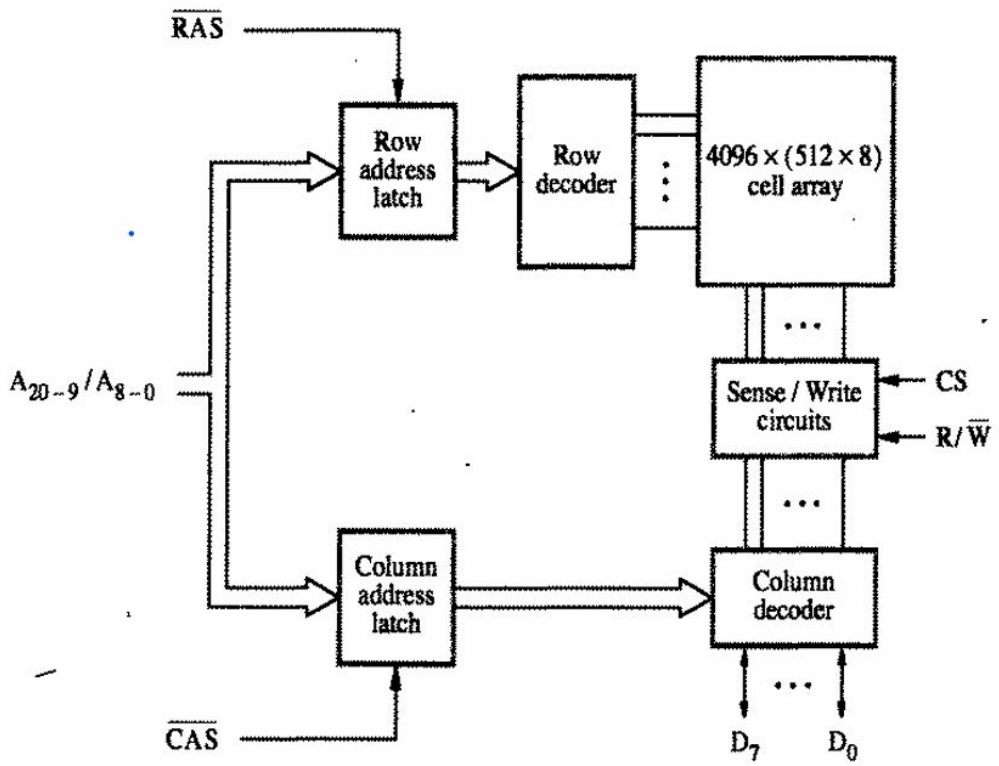

Figure 5.7 Internal organization of a 2M × 8 dynamic memory chip.

Designing 16Megabit Asynchronous DRAM as 2M x 8

Synchronous DRAM