CSEN402: Computer Organization
Project milestone 2
Team 42

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note: every signal is shifted by one as we assumed it is possible to have indirect addressing every T4 will be decremented to T3 , T5 to T4 , etc.

Register Transfer Language:

- T0 : AR ← PC
- T1 : IR ← M[AR] , PC ← PC + 1
- T2 : D0,.....,D7 ← Decode IR(12-14), AR ← IR(0-11) , I ← IR(15)

for AND:

- D0T4 : DR ← M[AR]
- D0T5 : AC ← AC ^ DR , SC ← 0

for ADD:

- D1T4 : DR ← M[AR]
- D1T5 : AC ← AC + DR , SC ← 0

for LDA:

- D2T4 : DR ← M[AR]
- D2T5 : AC ← DR , SC ← 0

for STA:

- D3T4 : M[AR] ← AC , SC ← 0

for SUB:

- D5T4 : DR ← M[AR]
- D5T5 : AC ← DR , DR ← AC
- D5T6: AC ← DR - AC , SC ← 0

for INC:

- D7I'T3B5 : AC ← DR , DR ← AC
- D7I'T4B5 : AC ← DR + 1, DR ← AC, SC ← 0

for BUN:

- D4T4 : PC ← AR, SC ← 0

for SZA:

- B2D7I'T3 : If (AC = 0) then (PC ← PC + 1 , SC ← 0)

Bus Selection Lines:

Priority encoder has been used to generate the selection line inputs of the multiplexer for the bus by taking the input lines from x0 to x7 and generating the output accordingly.

- x0(Memory) : T1 + D0T4 + D1T4 + D2T4 + D5T4
- x1(AR) : D4T4
- x2(TR) : X
- x3(DR) : X
- x4(AC) : D3T4 + D5T5 + D7I'T3B5 + D7I'T4B5
- x5(PC) : T0
- x6(IR) : T2
- x7(nothing) : X

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Register Loads:

- AR: T0 + T2
- TR: X
- DR: D0T4 + D1T4 + D2T4 +D5T4 + D5T5 + D7I'T3B5 + D7I'T4B5
- AC: D0T5 + D1T5 + D2T5 + D5T5 + D5T6 + D7I'T3B5 + D7I'T4B5
- PC: D4T4
- IR: T1
- I : T2

Increment PC : T1 + (AC == 0) ^ B2T3D7I'
Memory Read : T1 + D0T4 + D1T4 + D2T4 + D5T4
Memory Write : D3T4

ALU Control:

Priority encoder has been used to generate the selection line inputs of the multiplexer for the ALU by taking the input lines from x0 to x7 and generating the output accordingly.

- x0(nothing) : X
- x1 (DR + AC) : D1T5
- x2 (DR - AC) : D5T6
- x3(Transfer DR) : D5T5 + D2T5 + D7I'T3B5
- x4(DR ^ AC) : D0T5
- x5(DR ∨ AC) : X
- x6(DR XOR AC) : X
- x7(DR + 1) : D7I'T4B5

SC Clear:

- D7I'T3B2 + D1T5 + D2T5 + D5T6 + D0T5 + B5T4D7I' + D3T4 + D4T4.