



CSU32M10/CSU32M11

User Manual

8-bit RISC MTP MCU with 12-bit ADC

REV 1.4

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1 Product Overview

1.1 Functional Description

CSU32M10/CSU32M11 is an 8-bit CMOS single-chip RISC MCU with 12-bit ADC, built-in 2Kx16-bit MTP program memory and 104 bytes SRAM.

1.2 Main Features

High-performance RISC CPU

- ÿ 8-bit MCU ÿ Built-in 2Kx16-bit program memory MTP ÿ Built-in 128-byte EEPROM
- ÿ 104-byte data memory (SRAM) ÿ Only 43 single-word instructions ÿ 8-level PC storage stack, 8-level PUSH and POP stack

Oscillator

- ÿ Built-in 32/16/8/4/2MHz oscillator, accuracy is ±1%@5V, 25ÿ

Peripheral Features

- ÿ 14 bidirectional I/O ports ÿ 2 buzzer outputs, 2 PWM outputs, PWM2 can output from one of the PT5.0, PT1.5, PT1.4, PT3.0 ports
- ÿ Timer 3 supports 2 pairs of complementary PWM outputs and supports large drive output
- ÿ 5 internal interrupts: ADC, Timer 0, Timer/Counter 2, Timer/Counter 3 ÿ 2 external interrupts: INT0, INT1, 11 external interrupt inputs
- Entrance
ÿ 11 input ports with wake-up function ÿ 7+3 12-bit ADC
 - 6 reference voltage options: internal 1.4V, internal 2.0V, internal 3.0V, internal 4.0V, VDD, external input
 - With digital comparator
- ÿ Short circuit protection comparator, the comparison voltage supports four configurations: VDD or PT3.4 minus 80/200/320/480mv.
- ÿ Constant current source output, PT3.2 port outputs constant current source 50mA ÿ Provides a 1.4V, 2V, 3V, 4V reference voltage output, accuracy ±1.5%
- ÿ Low voltage detection (LVD) pin, internally provides 2.4V, 3.6V voltage comparator ÿ 4 open-drain output ports

— PT5.0, PT5.1, PT1.1, PT1.3 open drain

ÿ PT5.0 and PT5.1 output current can be configured as

IOL=53mA@5V, IOH=25mA@5V; ÿ

PT1.0, PT3.5 output current can be configured as IOL =30mA@5V, IOH=20mA@5V

ÿ Configurable input logic level threshold ÿ

5*8 LCD driver, 1/4 duty, 1/2 bias ÿ Support online simulation (ICD)

Features of Dedicated Microcontrollers

ÿ Power-on reset (POR) ÿ

Power-on reset and hardware reset delay timer (98ms) ÿ Built-in low voltage reset (LVR) ÿ Timer 0 — 8-bit timer/counter with

8-bit prescaler ÿ Timer/Counter 2 — 12-bit prescaler with 12-bit divider ÿ Timer/Counter 3 — 12-bit prescaler with 12-bit divider

ÿ Extended Watchdog Timer (32K WDT) — Programmable

time range ÿ Window Watchdog (CPU clock) — 7-bit down counter, cannot be disabled once enabled

Working conditions

ÿ Voltage operating range

— VDD 2.35V~5.5V ÿ Operating temperature range —
-40~85 °C

Low power consumption

ÿ MCU operating current

— Normal mode 2.5mA@16MHz,5V —
Current in sleep mode is less than 1ÿA

Encapsulation

ÿ MSOP10, SOP16, QFN16

Application

ÿ Mobile power

ÿ Electronic cigarette

1.3 Selection table

Table 1-1 Selection table

model	ROM	RAM	heap Stack	Certainty hour Device	PWM/ Buzz er	mutual repair PW M	IT	big drive move	Wake -up Pinout number	Heng flow source	Compa rison Device	LCD	ADC (CH*Bi t)	Encapsulation
CSU32M10-MSOP10 2K*16 104 8			3 2			1	8	2	7	1	1	- 4*12		MSOP10
CSU32M10-SOP16 2K*16 104 8			3 2			2	14 4 11			1	1 5*8	7*12		SOP16
CSU32M11-SOP16 2K*16 104 8			3 2			2	14 4 11			1	1 5*8	7*12 1 5*8 7*12		SOP16
CSU32M10-QFN16 2K*16 104 8			3 2			2	14 4 11			1				QFN16

1.4 PIN Configuration

1.4.1 MSOP10 PIN Configuration

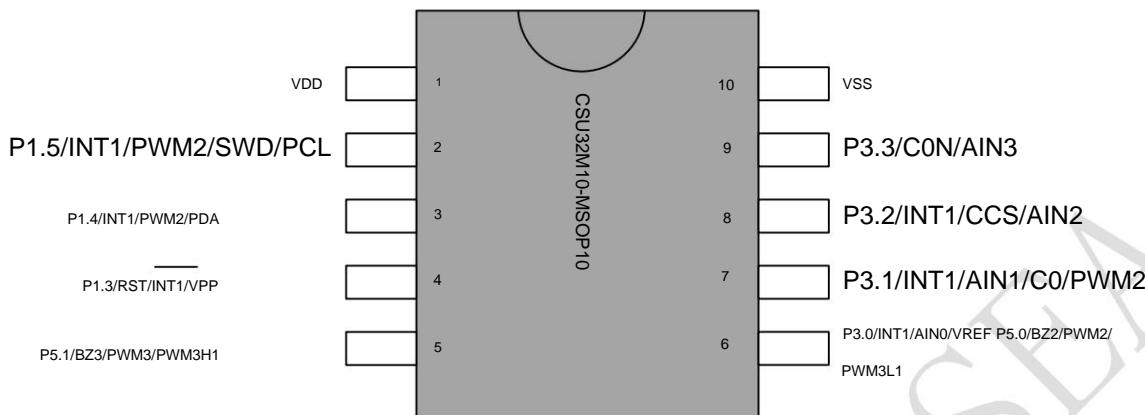


Figure 1-1 MSOP10 pin diagram

Note: When the PT5.0 port of MSOP10 is used as output, the PT3.0 port needs to be configured as input or analog port; similarly, when the PT3.0 port is used as output, the PT5.0 port needs to be configured as input port.

1.4.2 SOP16-1 PIN Configuration

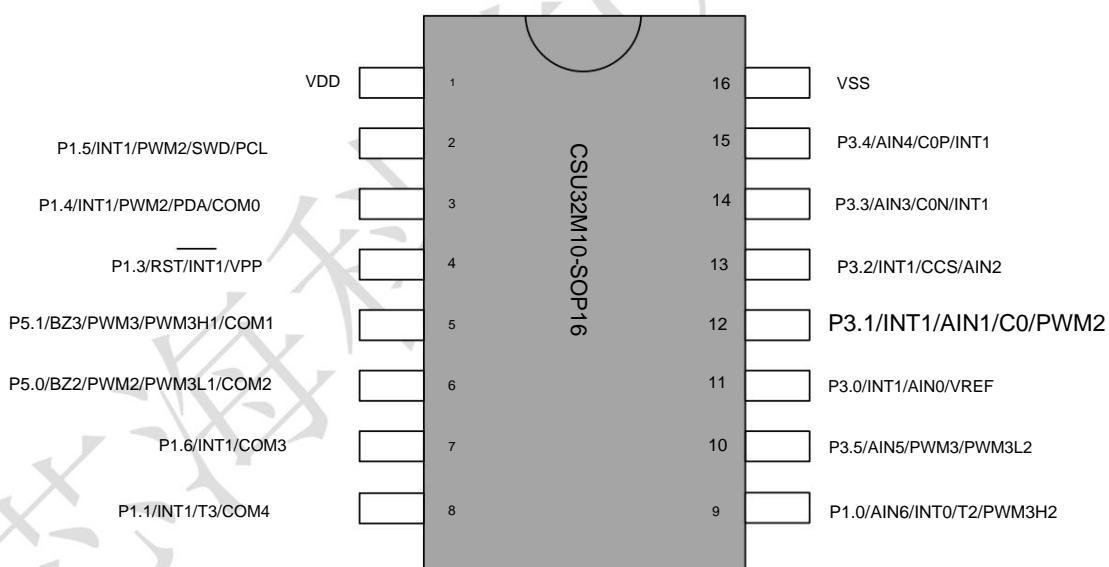


Figure 1-2 SOP16-1 pin diagram

1.4.3 SOP16-2 PIN Configuration

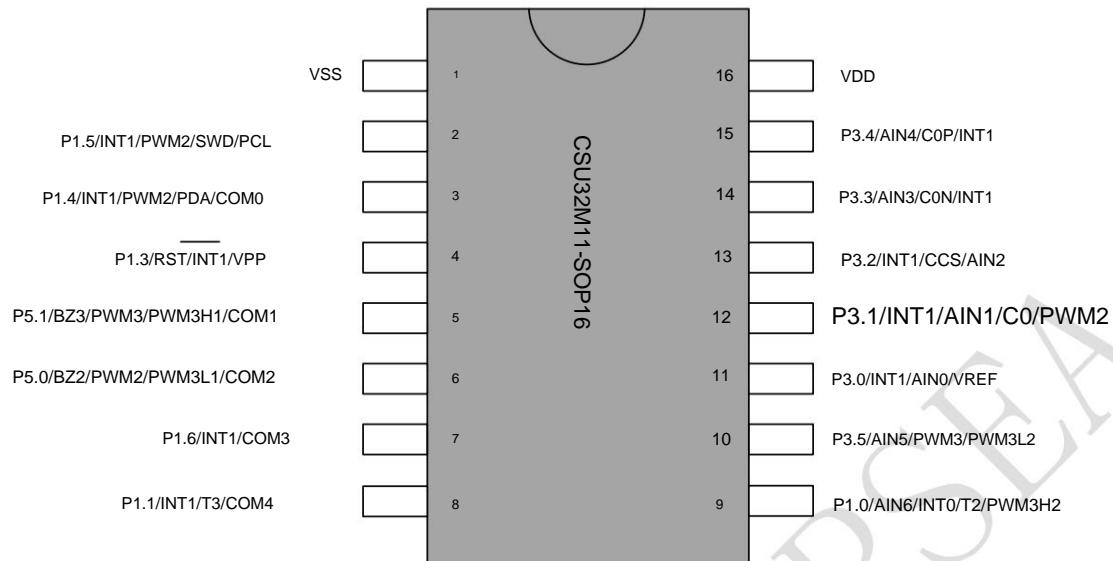


Figure 1-3 SOP16-2 pin diagram

1.4.4 QFN16 PIN Configuration

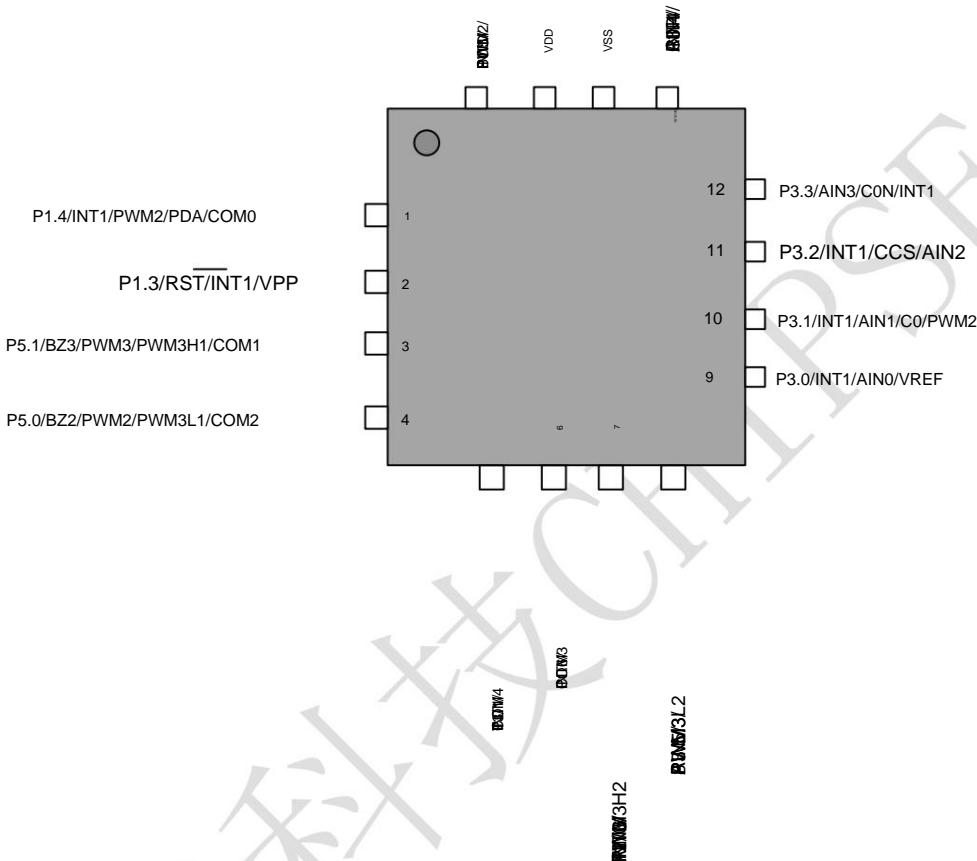


Figure 1-4 QFN16 PIN configuration diagram

Note: The metal pad under the CSU32M10-QFN16 package is not VSS. The package does not connect the metal pad to VSS. Please pay special attention.

1.5 Pin Description

Table 1-2 Pin Description

Pin Name	enter /lose out	SOP16- 1 pin Serial number	SOP16 -2 tubes Foot number	QFN16 Pin sequence Number	MSOP10 Pin sequence No.	describe
VSS	P	16	1	14	10	
P1.5/INT1/PWM2/ SWD/PCL	I/O	2	2	16	2	IO; external interrupt 1 input, with wake-up function; PWM2 output port; ICD debugging communication port; when burning Bell mouth
P1.4/INT1/PWM2/ PDA/COM0	I/O	3	3	1	3	IO; external interrupt 1 input, with wake-up function; PWM2 output port; burning input data port; COM port
P1.3/ RST /INT1/ VPP	I	4	4	2	4	IO, pure open drain output; reset input, low level Effective; External interrupt 1 input, with wake-up function; Burning voltage
P5.1/BZ3/PWM3/P WM3H1 /COM1	I/O	5	5	3	5	IO, with open-drain output; buzzer 3 output; PWM3 Output; Complementary PWM3H1 output; COM port
P5.0/BZ2/PWM2/P WM3L1/COM2	I/O	6	6	4	6	IO, with open-drain output; buzzer 2 output; PWM2 Output; complementary PWM3L1 output; COM port
P1.6/INT1/COM3 I/O P1.1/INT1	T3/CO	7	7	6		IO; external interrupt 1 input; COM port
M4	I/O	8	8	5		IO, with open-drain output; external interrupt 1 input; with With wake-up function; Timer/Counter 3 external input; COM Port
P1.0/AIN6/INT0/ T2/PWM3H2	I/O	9	9	7		IO; ADC input channel 6; external interrupt 0 input; With wake-up function; Timer/Counter 2 External Input Input; complementary PWM3H2 output;
P3.5/AIN5/PWM3/ PWM3L2	I/O	10	10	8		IO; ADC input channel 5; PWM3 output; complementary PWM3L2 output;
P3.0/ INT1/AIN0/VREF	I/O	11	11	9	6	IO; external interrupt 1 input, with wake-up function; ADC input channel 0; ADC reference voltage input
P3.1/INT1/ AIN1/CO/PW M2	I/O	12	12	10	7	IO; external interrupt 1 input, with wake-up function; ADC input channel 1; comparator result output; PWM2 Output
P3.2/INT1/ CCS/AIN2	I/O	13	13	11	8	IO; external interrupt 1 input, with wake-up function; 50mA constant current source output; ADC input channel 2;
P3.3/AIN3/CON/I NT1/T3	I/O	14	14	12	9	IO; ADC input channel 3; comparator negative input; External interrupt 1 input, with wake-up function; timing/ Counter 3 external input;
P3.4/AIN4/C0P/I NT1/T2	I/O	15	15	13		IO; ADC input channel 4; comparator positive input; External interrupt 1 input, with wake-up function; timing/ Counter 2 external input;
VDD	P	1	16	15	1	power supply

1.6 Resource Differences between CSU32M10/CSU32M11 and CSU8RP3119B/3117B/3115B, CSU32P20

Table 1-3

Differences	CSU8RP3119B/3117B/3115B	CSU32P20	CSU32M10/CSU32M11
Program Memory	1Kx14	2Kx16	2Kx16
SRAM	64 bytes 11	104 bytes 104 bytes	
I/O	bidirectional ports, 1 input mouth	13 bidirectional ports, 1 input port 14 bidirectional ports	
Timer	3 1-	3 2-	3
complementary	channel complementary	way complementary	2 complementary PWM
PWM large drive port	PWM PT5.0, PT5.1 port power supply Current 80mA@5V	PWM 1, PT5.0 and PT5.1 outputs Streams can be configured as IOL=53mA@5V IOH=25mA@5V 2. PT1.0, PT3.5 can be input The output current can be configured as IOL = 30mA@5V. IOH=20mA@5V	1. PT5.0 and PT5.1 input The output current can be configured as IOL=53mA@5V IOH=25mA@5V 2. PT1.0, PT3.5 can be input The output current can be configured as IOL = 30mA@5V. IOH=20mA@5V
Open drain output	PT1.1~PT5.0~PT5.1 PT1.1~PT5.0~PT5.1	PT1.3	PT1.1~PT5.0~ PT5.1~PT1.3
LCD Driver	No	5x8 software LCD	5x8 Software LCD
Window Watchdog (WWDT)			have
Instruction Cycle	2.35V~5.5V Support 4MHz 2.2V~5.5V supports 2MHz	with 2.35V~5.5V supports 4MHz	2.35V~5.5V supports 4MHz
External crystal or ERC not supported		No support	Not supported
UART			none
Analog Comparator	None		have Support for short-term measures against e-cigarettes Road protection function
Constant current source	none	none	Support 50mA constant current source output

2 Standard features

2.1 CPU Core

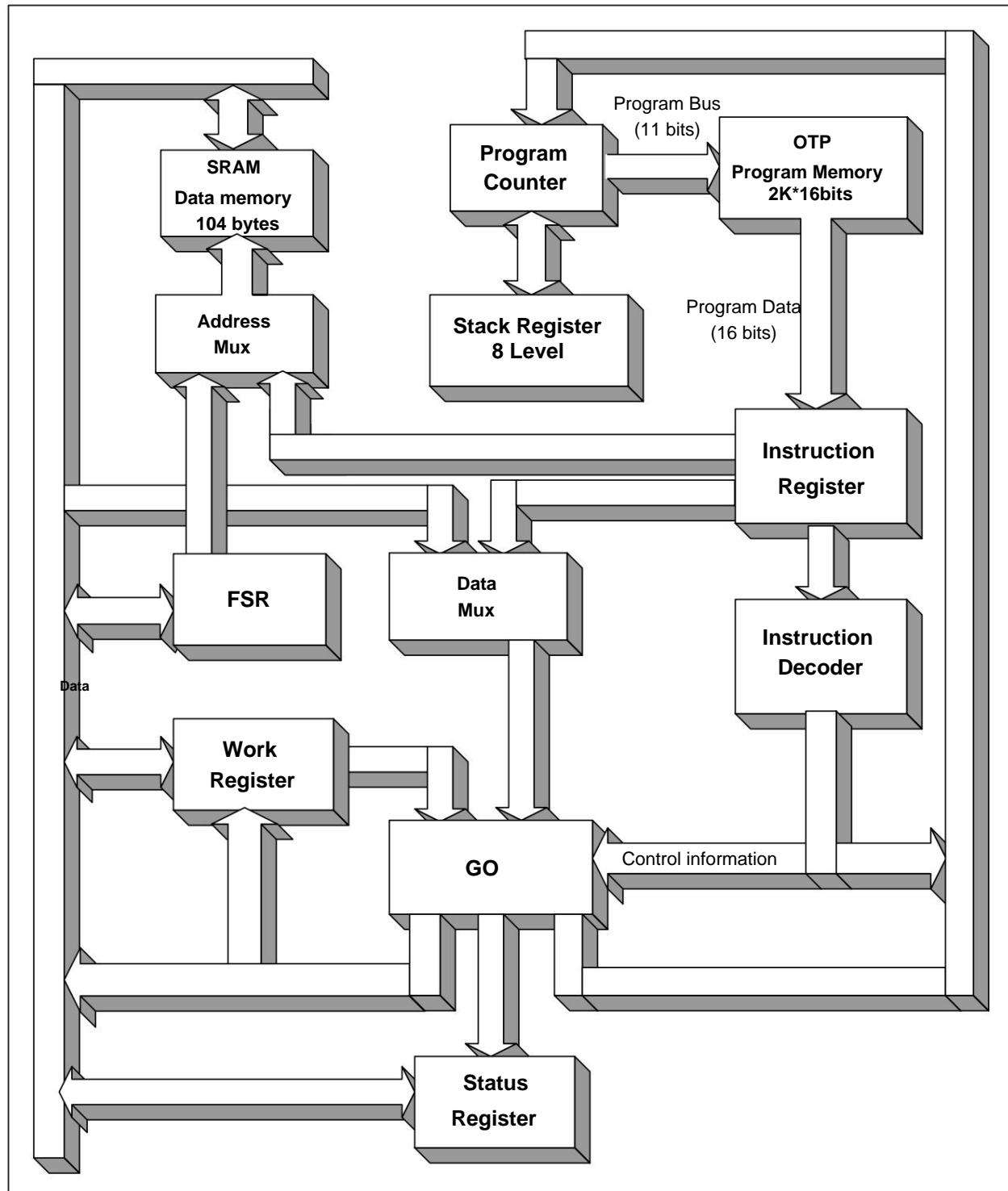


Figure 2-1 Functional module diagram of CSU32M10/CSU32M11 CPU core

From the functional module diagram of the CPU core, we can see that it mainly consists of 7 main registers and 2 memory units.

Table 2-1 MCU architecture description

Module Name	
Program Counter	Description This register plays an important role during the CPU's working cycle. It records the CPU's processing program in each cycle. In one CPU cycle, the program counter changes the address of the program memory to (11 bits), the instruction pointer is pushed to the program memory and then automatically incremented by 1 for the next cycle.
Stack registers	The stack register is used to record the instruction pointer to which the program returns. The instruction pointer is pushed to the stack register. After the function is executed, the stack register will push the instruction pointer to the stack register. Returns the program counter to continue the original program processing.
Instruction Register	The program counter pushes the instruction pointer (program memory address) to the program memory, which The data (16 bits) from the sequence memory are pushed to the instruction register. The instructions of CSU32M10/CSU32M11 are 16 bits, including 3 types of information: direct address, immediate value and control information. Direct address (8 bits): The address of the data memory. The CPU can use this address to store data. device to operate. Immediate data (8 bits): The CPU uses this data to operate on the working register through the ALU. Control information: It records the operation information of ALU.
Instruction decoder	The instruction register pushes the control information to the instruction decoder for decoding, and then the decoder sends the decoded information to the instruction decoder. The information is sent to the relevant registers.
The arithmetic logic unit can not only perform arithmetic calculations such as addition, subtraction, addition 1, subtraction 1, etc. of 8-bit binary, but also Bit variables can perform logical operations such as logical AND, OR, XOR, circular shift, complement, and clear.	
Working Register	The working registers are used to cache data and immediate values in the data memory.
Status Register	When the CPU uses the ALU to process register data, the following states will change in the following order: PD, TO _Y DC _Y C _Y Z _Y
In the instruction set of CSU32M10/CSU32M11, the file select register FSR is used for indirect data processing (i.e., to implement indirect search).	The user can use FSR to store a register address in the data memory, and then use the indirect The address register (IND) handles this register.
Program Memory	CSU32M10/CSU32M11 has 2Kx16-bit MTP as program memory. (OPCODE) is 16 bits, and the user can only program 2K instructions at most. The address bus of the program memory is 11 bits, the data bus is 16 bits.
Data storage	CSU32M10/CSU32M11 has 104 bytes of SRAM as data memory. The address bus is 7 bits and the data bus is 8 bits.

2.1.1 Memory

2.1.1.1 Program Memory

The program memory is mainly used to store instructions. In CSU32M10/CSU32M11, the program memory is 2K*16bit program MTP, for programmers, this memory is read-only and cannot be written. The system reset address is 000H, and the interrupt entry address is 004H, it should be noted that all interrupts share the same interrupt entry address.

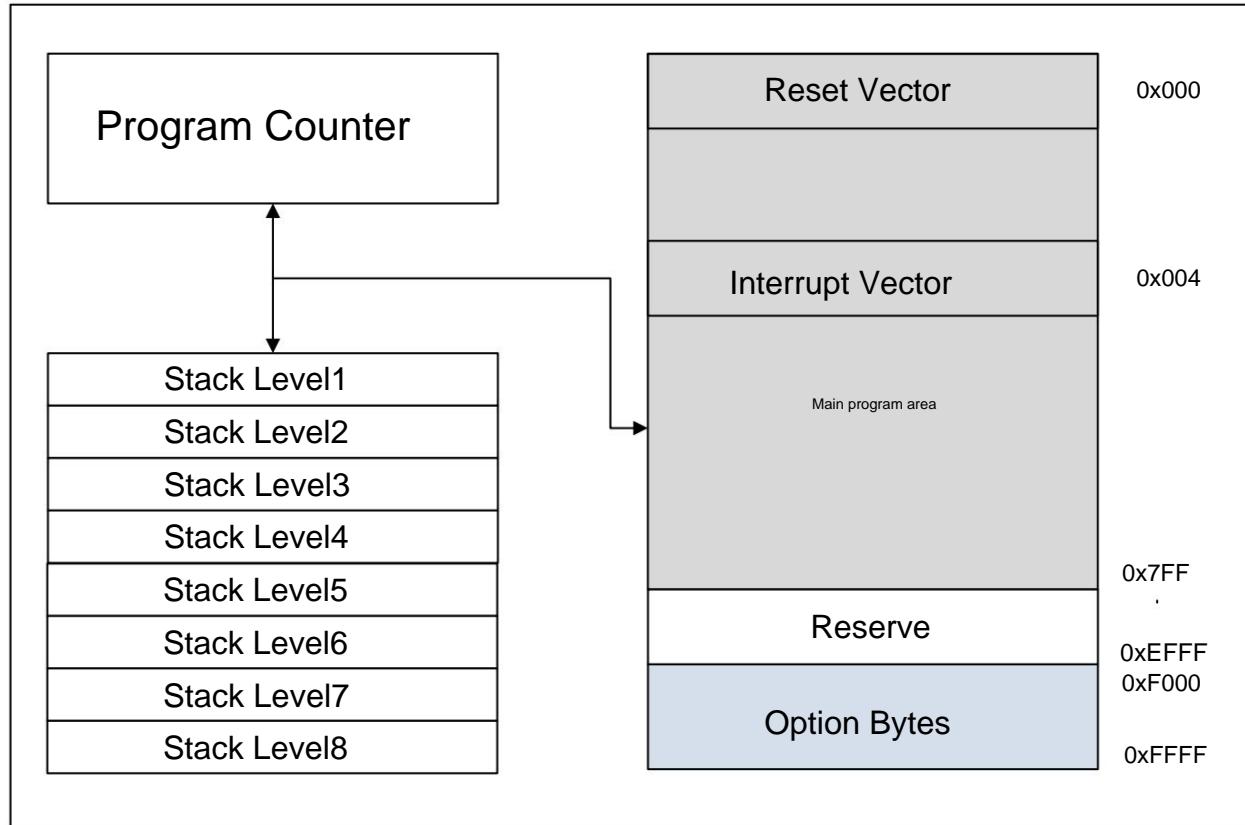


Figure 2-2 Program memory

2.1.1.2 EEPROM

EEPROM is mainly used to store data that needs to be retained after power failure. In CSU32M10/CSU32M11, the EEPROM size is 128 bytes, the address range is 0x2000~0x207F.

CSU32M10/CSU32M11 has a built-in 128-byte EEPROM memory with an erase and write endurance of 10,000 times and a write operation voltage range of 2.5V~5.5V. The program cannot directly access the EEPROM, and can only read and write the EEPROM through MOVP and TBLP instructions. The memory address is 0x2000~0x207F. To write to the EEPROM, the write protection must be unlocked.

2.1.1.3 Data Storage

The data memory is mainly used to store global variables and intermediate variables during program execution. The memory is divided into three parts. The 00H to 08H addresses are system special function registers, such as indirect address, indirect address pointer, status register, working register, interrupt flag, interrupt control register. Address 09H to 7FH corresponds to peripheral special function registers, such as IO ports, timers. The system special function registers and peripheral special function registers are implemented by registers, while the general data memory is implemented by RAM, which is readable and writable.

Table 2-2 Data memory address allocation

Data Memory	Starting address	End address
System Special Function Registers	00H	08H
Peripheral Special Function Registers	09H	7FH

General purpose data storage	80H	E7H
------------------------------	-----	-----

The data memory and special function registers can be accessed indirectly through the IND0 and FSR0 registers.

When the address register (IND0) reads data, the MCU actually uses the value in FSR0 as the address to access the data memory to obtain the data.

When writing data to the indirect register (IND0), the MCU actually uses the value in FSR0 as the address to access the data memory.

And store the value at the address. The access method is shown in the figure below.

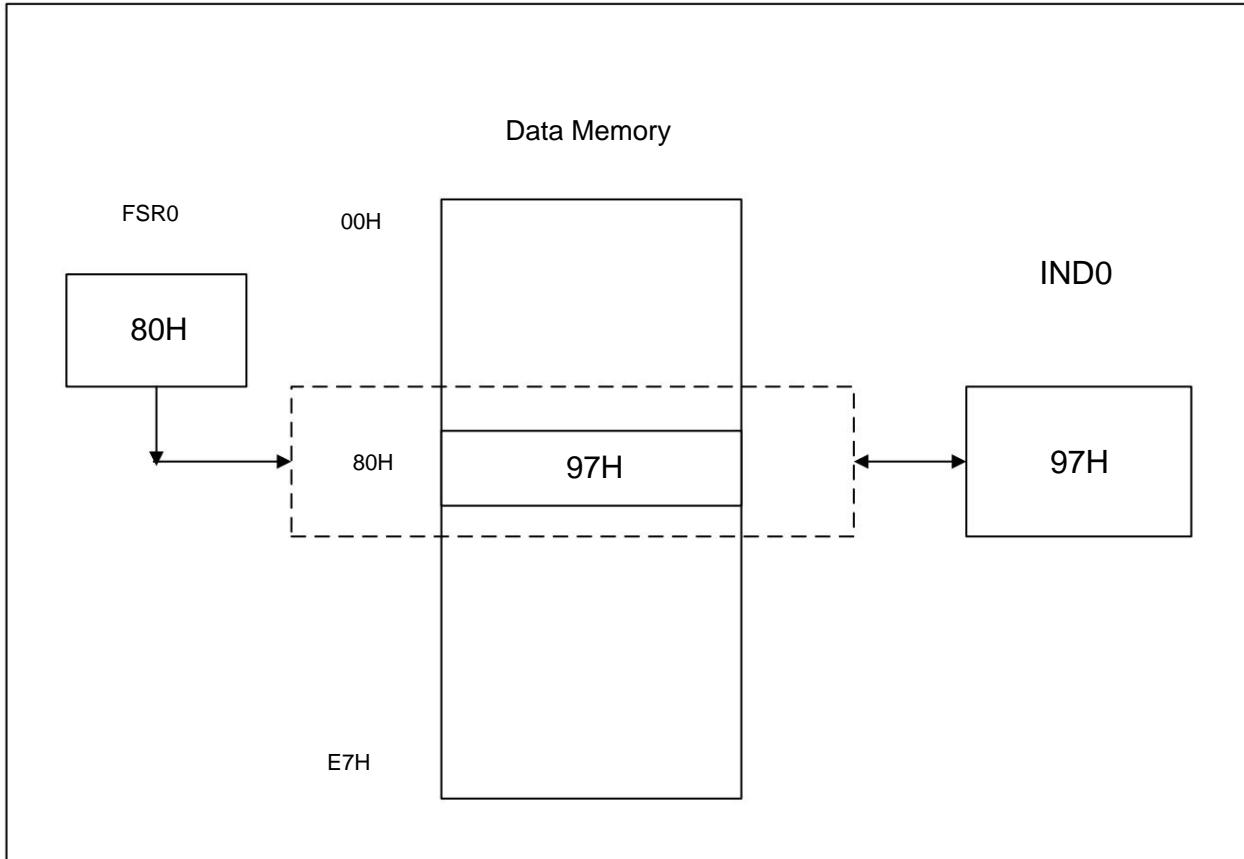


Figure 2-3 Indirect address access

2.1.2 Status Register

The status register contains the arithmetic status and reset status of the ALU. The status register, like other registers, can be used as a destination register for an instruction that affects the Z, DC, or C bits. If the status register is the destination register for an instruction that affects the Z, DC, or C bits, then the status register is set to zero for all three bits. Writing to the TO and PD bits is invalid. These bits are set or cleared by the device logic. The TO and PD bits are not writable.

2.1.2.1 STATUS Status Register (Address 04h)

Table 2-3

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics RX		U-0	U-0	R-0	R-0	R/W-0	R/W-0	R/W-0
STATUS	LVD24			PD	TO	DC	C	RESERVED

Table 2-4

Bit address identifier		Function
7	LVD24	2.4V LVD operating voltage flag, only valid when code option LVD_SEL is 2'b01 1: The system operating voltage is lower than 2.4V, indicating that the low voltage detector is in monitoring state 0: The system operating voltage exceeds 2.4V and the low voltage detector does not work.
6~5 RESERVE		reserve
4	PD	Power-off flag, set this bit after sleep 1: After executing the SLEEP instruction 0: After power-on reset or hardware reset or CLRWDT instruction
3	TO	Watchdog timer overflow flag, watchdog timer overflow sets this bit 1: Watchdog timer overflow occurs 0: After power-on reset or hardware reset or CLRWDT instruction or SLEEP instruction
2	DC	Half-byte carry flag/borrow flag When used for carry 1: A carry overflow occurs at the 4th bit of the result 0: No carry overflow occurred at the 4th bit of the result When used for borrow, the polarity is opposite 0: The 4th bit of the result has a borrow overflow 1: No borrow overflow occurs at the 4th bit of the result
1	C	Carry flag/borrow flag When used for carry 1: A carry overflow occurs in the most significant bit (MSB) of the result 0: The MSB of the result does not overflow. When used for borrow, the polarity is opposite 0: The MSB of the result has a borrow overflow 1: The MSB of the result does not overflow with borrow
0	RESERVED	Zero Flag 1: The result of an arithmetic or logical operation is 0 0: The result of an arithmetic or logical operation is not 0

Property:

R = readable bit

W = Writable bit

U = invalid bit

18M40 value after power-on reset '1' = bit is set '0' = bit is cleared X = undefined bit

CS-QR-YF-054A02

2.1.3 SFR

The Special Function Registers (SFRs) contain system-specific registers and auxiliary-specific registers.

System-specific registers are used to complete the functions of the CPU core, including indirect address, indirect address pointer, status register, working register Device, interrupt flag and interrupt control register.

Auxiliary special registers are designed for auxiliary functions, such as I/O ports, timers, and peripheral control registers.

Table 2-5 Register list

Index	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset value						
Address		The address pointer of the data indirect data memory in the data														
00h INDO		memory with the content of FSR0 as the address 0														
02h FSR0 04h	LVD24			PD	TO	DC	C			xuu00000						
STATUS 05h WORK		Working Register														
06h INTF		TM2IF		TM0IF SRADIF		E1IF	E0IF u0u000000									
07h NOT	GO	TM2IE		TM0IE SRADIE		E1IE	E0IE 00u000000									
09h RSTSR					EMCF	ILOPF	WWDTF uuuuuu000									
0Ah EADRH		EADR[15:8]														
0Mh EADRL		EADR[7:0]														
0Ch EDATH		EDIT[7:0]														
0Dh WDTCON	WDTEN					WTS[2:0]				0uuuu000						
0Eh WDTIN		WDTIN[7:0]														
0Fh TM0CON	TOEN	T0RATE[2:0]			T0RSTB	T0SEL[1:0]				0000u100						
10h TM0IN		TM0IN[7:0]														
11h TM0CNT		TM0CNT[7:0]														
16h MCC			CST_WDT							uu1uuuu						
17h TM2CON	T2EN	T2RATE[2:0]			T2CKS T2RSTB	T2OUT	PWM2OUT			0000100						
18h TM2IN		TM2IN[7:0]														
19h TM2CNT		TM2CNT[7:0]														
1Ah TM2R		TM2R[7:0]														
1Bh TM3CON	T3EN	T3RATE[2:0]			T3CKS T3RSTB	T3OUT	PWM3OUT			0000100						
1Ch TM3IN		TM3IN[7:0]														
1Dh TM3CNT		TM3CNT[7:0]														
1Eh TM3R		TM3R[7:0]														
1Fh TM3INH					TM3INH[11:8]											
20h PT1		PT1[6:3]					PT1[1:0]			uxxxxuxx						
21h PT1EN		PT1EN[6:3]					PT1EN[1:0]			u0000u00						
22h PT1PU		PT1PU[6:3]					PT1PU[1:0]			u0000u00						
23h PT1CON	PT11OD	PT1W[3:0]				E1M	E0M[1:0]			00000000						
24h TM2INH					TM2IN[11:8]											
25h TM2CNTH					TM2CNT[11:8]											
26h TM2RH					TM2R[11:8]											
27h TM3CNTH					TM3CNT[11:8]											
28h PT3		PT3[5:0]														
29h PT3EN		PT3EN[5:0]														
2Ah PT3PU		PT3PU[5:0]														
2Bh PT3CON		PT3CON[5:0]														
2Ch TM3RH					TM3R[11:8]											
2Dh TM3CON2	DT3CK[1:0]	DT3CNT[2:0]				DT3_EN P3H_OEN P3L_OEN	00000000									

2Eh	METCH1	P3HINV P3LINV		PT1W[6:4]	PWM2PO	PWM2PO1		0000000u
2Fh	METCH	VTHSEL		REF_SEL[2:0]	PWMIS	T3RATE[3]]	T2RATE[3] P14_CUR 00000000	
30h	PT5						PT5[1:0]	uuuuuuuxx
31h	PT5EN						PT5EN[1:0]	uuuuuu00
32h	PT5PU						PT5PU[1:0]	uuuuuu00
33h	PT5CON						PT51OD	PT50OD uuuuuu00
34h	SRADCON0			SRADACKS[1:0]			SRADCKS[1:0]	uu00uu00
35h	HEARTCON1	SRADEN SRADS OFTEN CALIF			ENOV		VREFS[1:0]	00000u00
36h	SRADCON2		CHS[3:0]					0000uuuu
37h	SRADL			SRAD[7:0]				00000000
38h	STREET						SRAD[11:8]	uuuu0000
39h	SROFTL			ROUGH[7:0]				00000000
3Ah	SROFTH						SROFT[11:8]	uuuu0000
3Ch	INTF2	CMPIF		TM3IF				0uu0uuuu
3Dh	INTE2	CMPIE		TM3IE				0uu0uuuu
40h	INTCFG	LVD36 LVD24					INTCFG[2:0]	xxuuu000
41h	PT1CON1						PT1CON0 uuuuuu0	
42h	PT1PD			PT1PD[6:3]			PT1PD[1:0]	uu0000u00
43h	PT3PD				PT3PD[5:0]			uu000000
44h	PT5PD						PT5PD[1:0]	uuuuuu00
45h	TM3CON3	PWM3PO			P3H2INV P3L2INV P3H2OEN P3L2OEN 0uuu0000			
46h	LCDCOM				LCDCOM[4:0]			uuu00000
47h	WWDTCR	WWDTEN			TR[6:0]			01111111
48h	WWDTWR				WD[6:0]			u1111111
60h	ISPCON1	CHKRSLT						0uuuuuuuuu
63h	WRPRT							WRPRTF 00000000
6Ah	CMPCON0	CMPEN		HYSN CMP_PSE L		CMP_NSEL[2:0]	CMPOUT0 0000000	
6Bh	CMPCON1	CMPOEN CMPVTHEN CMPVTHS[1:0] VTHOEN				CMP_FLT[2:0]		00000000
6Ch	CMPCON2	CMPENS[1:0]	CMPINTS[1:0]				TM3STP	TM2STP 000uuu00
6Dh	CCSCON							CCSOEN uuuuuuu0
79h	METCH2					METCH2[3:0]		uuuu0000

Note: When performing a read operation, the invalid bit is read as 0

Property:

R = readable

W = Writable bit

U = invalid bit

bit -n = value after power-on reset '1' = bit is set '0' = bit is cleared X = undefined bit

2.2 Clock system

2.2.1 Overview

The chip clock system includes a built-in 32/16/8/4/2MHz RC oscillator clock (HIRC), a built-in low-speed 32KHz WDT clock, and a built-in 32KHz WDT clock. CSU32M10/CSU32M11 only has built-in high-speed RC oscillator clock (HIRC) that can be used as the system clock source Fosc. Fcpu is the CPU clock. The fastest instruction cycle supported by CSU32M10/CSU32M11 is 4MHz. When the 32MHz built-in RC oscillator is selected, 4-minute The maximum frequency division is 8.

Normal mode (high-speed clock): $F_{CPU} = F_{OSC}/N$, $N=4, 8, 16, 32$

2.2.2 Clock Block Diagram

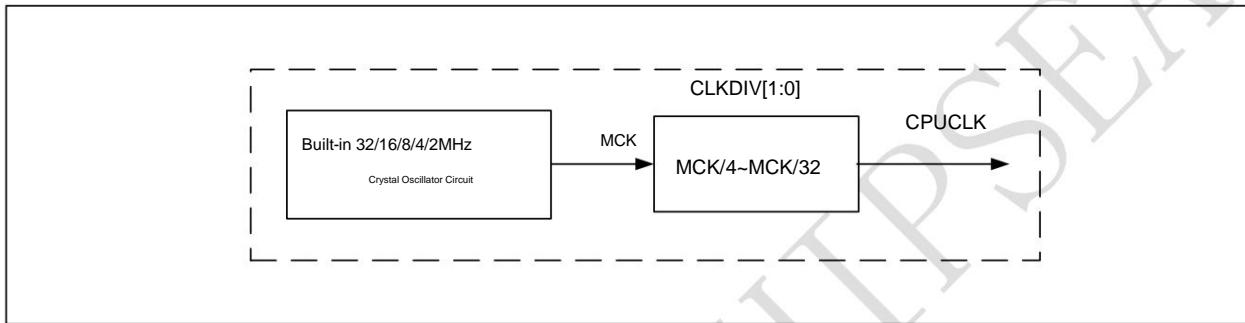


Figure 2-4 CSU32M10/CSU32M11 oscillator state diagram

2.2.3 Registers

Table 2-6 CSU32M10/CSU32M11 clock system register list

Address	Name	Bit7	Bits6	Bit5	Bits4	Bit3	Bits2	Bit1	Bit0	Power-On Reset value
16h	MCK				CST_WDT					uu1uuuu

2.2.3.1 MCK register (address 16h)

Table 2-7

Bit number	Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0			U-0	R/W-1	U-0	U-0	U-0	U-0	U-0
MCK				CST_WDT					

Table 2-8

Bit address identifier		
5	CST_WDT	Function Internal 32K low speed oscillator start switch, when code option WDT_CFG is configured as internal 32K When the low-speed oscillator is fixed on, this bit is invalid. 1: Internal 32K low speed oscillator is turned off 0: Internal 32K low speed oscillator is turned on

When writing to the MCK register, it is recommended to use the BCF or BSF instruction.

2.2.4 Internal high speed RC clock

Internal high-speed RC clock (32/16/8/4/2MHz), the system can only use the internal high-speed RC clock as the main clock of the system.

2.2.5 Internal low speed wdt clock

The internal low-speed wdt clock (32kHz) can be configured through WDT_CFG. When WDT_CFG is 0, the internal 32K low-speed oscillator is fixed on, software cannot turn it off. When WDT_CFG is 1, the switch is enabled through register CST_WDT. The internal WDT clock cannot be used as the system main clock and can only be used as the WDT and Timer 0 clock.

2.3 Reset System

CSU32M10/CSU32M11 can be reset in the following ways:

- 1) Power-on reset
- 2) RST hardware reset (normal operation)
- 3) RST hardware reset (from Sleep mode)
- 4) WDT reset (normal operation)
- 5) WDT reset (from Sleep mode)
- 6) Low Voltage Reset (LVR)
- 7) WWDT reset
- 8) Illegal instruction reset
- 9) EMC reset

When any of the above resets occurs, all system registers return to their default states (except the TO and PD flags when WDT is reset).

The program stops running and the program counter PC is cleared. After the reset is completed, the system address restarts from 000H.

The reset register flags are shown in the following table.

Table 2-9 Relationship between reset signal and status register

	TO	PD	WWDTF	EMCF	ILOPF
Conditional Power-On Reset	0	0	0	0	0
RST Hardware reset (normal operation)	0	0	0	0	0
RST Hardware reset (from Sleep mode) 0		0	0	0	0
WDT Reset (Normal Operation)	1	constant	Unchanged,	unchanged	constant
WDT reset (from Sleep mode) Low voltage reset	1	1	unchanged,	unchanged	constant
	0	0	unchanged	unchanged	constant
WWDT reset illegal	Unchanged,	Unchanged,	1	unchanged	constant
instruction reset	unchanged,	unchanged,	constant	unchanged	1
The schematic	unchanged	unchanged	0	1	0

Diagram of the EMC reset circuit is shown below.

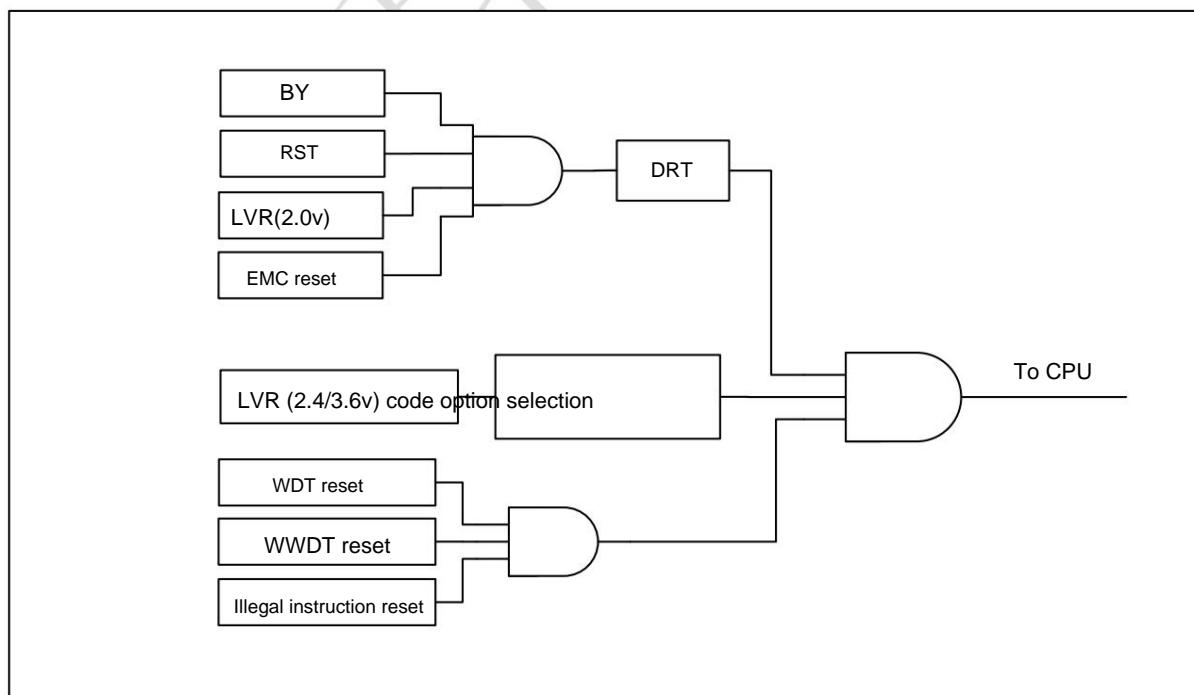


Figure 2-5 Reset circuit schematic

Any reset situation requires a certain response time. The system provides a complete reset process to ensure the smooth progress of the reset action.

Different types of oscillators have different start-up times, so the time to complete the reset is also different. Users should reserve

Wait for a certain period of time for the system to stabilize. When using the terminal, users should pay attention to the host's requirements for power-on reset.

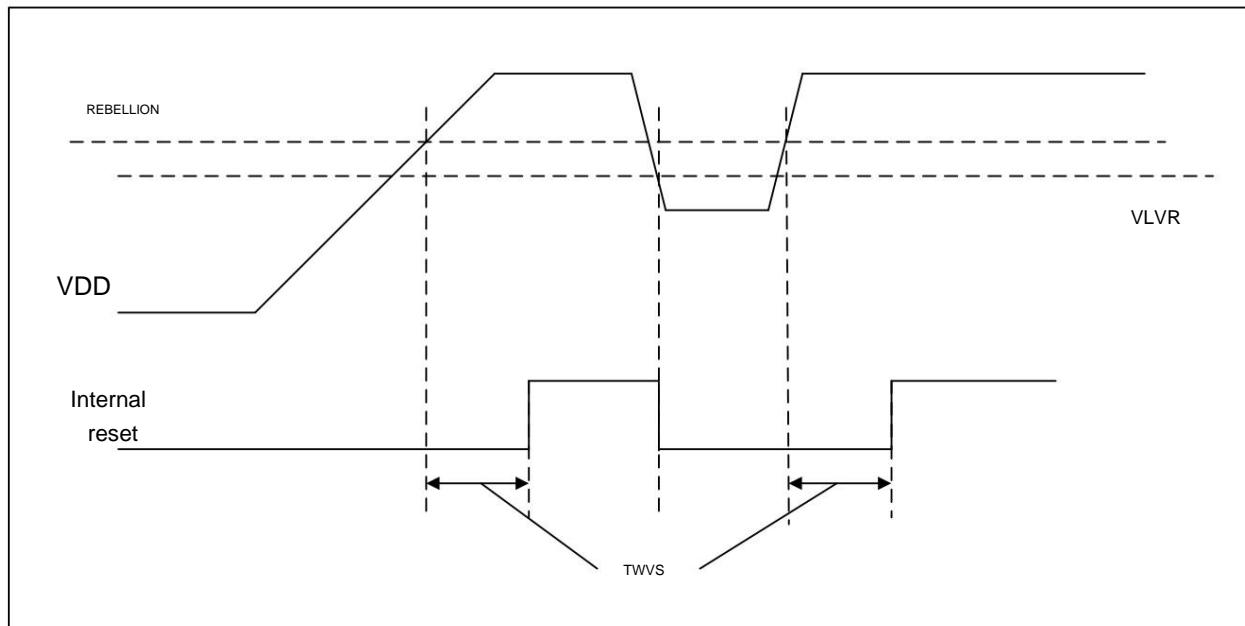


Figure 2-6 Example of power-on reset circuit and power-on process

Table 2-10

parameter	Minimum	Typical Value	Maximum
REBELLION	1.7V	2.0V	2.3V
VLVR	1.7V	2.0V	2.3V
TWVS (Test conditions: VDD=5V, T=25°C)	78.4ms	98ms	117.6ms

VPOR: Power-on reset

VLVR: Power-off reset

TWVS : Waiting time for voltage stabilization

2.3.1 Power-On Reset

The system power-on voltage shows a gradually rising curve, and it takes a certain amount of time to reach the normal working voltage (for different indicators).

The operating voltage required for each command cycle is different. The faster the command cycle, the higher the required operating voltage (see 6.2 DC characteristics).

2.3.2 Watchdog reset

Watchdog reset is a system protection setting. Under normal conditions, the program will clear the watchdog timer. If an error occurs, the system will be in

Unknown state, in this case, use the watchdog reset. After the watchdog reset, the system returns to the normal state.

The watchdog reset can wake up the SLEEP mode and HALT mode, reset the chip, and the system re-enters the normal state.

2.3.3 Window Watchdog Reset

The window watchdog is mainly used to detect software errors caused by external interfaces or unpredictable logic errors.

With the program running, WWDT can generate a reset to reset the MCU.

The WWDT will stop counting in SLEEP mode, so it cannot wake up from SLEEP mode.

The behavior of the WWDT in HALT mode can be configured by code options to continue counting in HALT mode or

If the chip continues to count in HALT mode, it can be woken up by resetting.

2.3.4 Power-off reset

The power-off reset is for externally caused power supply voltage drop, such as interference or load change. Power failure may cause

The system is not working properly or the program is executing incorrectly.

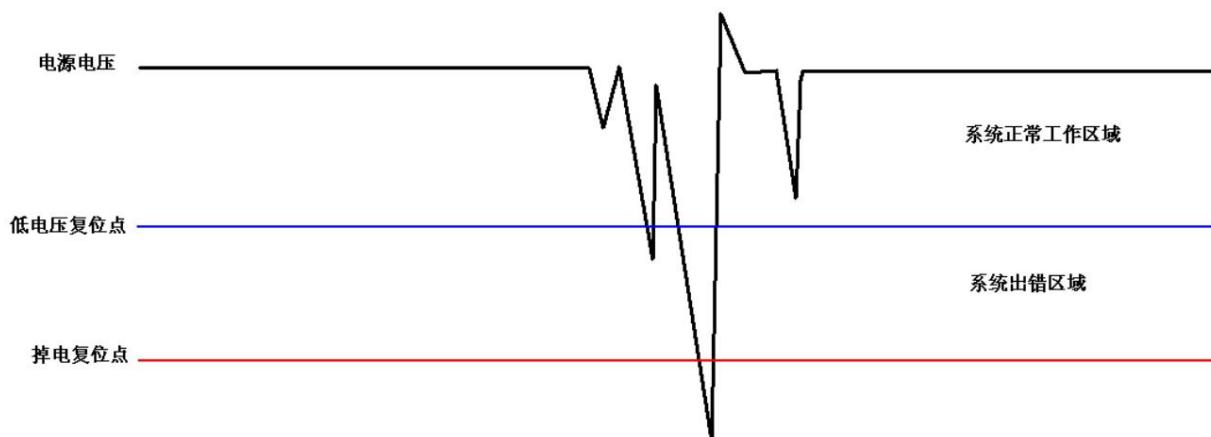


Figure 2-7 System power-off reset diagram

The power supply voltage drop may cause the chip to enter the system dead zone. The system dead zone means that the power supply voltage cannot meet the minimum operating voltage requirement of the system. The system power-off reset diagram is shown in the figure above. The power-off reset point of the chip is 2.0V, and the low voltage reset point of the chip can be set to 2.4/3.6V through the code option.

To avoid entering the system dead zone, it is recommended to use the low voltage reset (LVR) function, especially when the instruction cycle is a high-speed application. The system error area of different instruction cycles is different, depending on the instruction cycle operating voltage range, see 6.2. The improvement of power-off reset performance can be achieved through the following points: 1) Low voltage reset (LVR) 2) Watchdog reset 3) Reduce the system instruction cycle 4) Use an external reset circuit (Zener diode reset circuit; voltage offset reset circuit; external IC reset)

2.3.5 External Hardware Reset

The external reset is controlled by the code option RESET_PIN, see 3.12. By setting this code option, the external hardware reset function can be enabled. The external hardware reset pin is a Schmitt trigger structure, and the low level is valid. When the hardware reset pin is high, the system works normally; when the hardware reset pin is low, the system is reset. After the chip code option enables the external hardware reset function, it should be noted that: after the system is powered on, the external reset needs to be input high level, otherwise, the system will reset until the external hardware reset ends. External hardware reset can use system reset during power-on. A good external reset circuit can protect the system from entering the system dead zone.

2.3.6 Illegal instruction reset

In order to enhance the chip's anti-interference ability, the chip will automatically detect illegal system instructions. If an illegal instruction is detected, it will automatically generate an MCU reset signal to reset the chip. This reset has no enable bit and cannot be turned off.

Illegal instructions include the following: 1. Other instruction codes outside the instruction set and pseudo-instructions of this document.

2. Accessing addresses beyond 104 bytes of SRAM (0x80~0xE7) and stack addresses (0xE8~0xFF), i.e., greater than 0xFF

The address of.

3. Accessing addresses outside the 2K MTP space, that is, addresses greater than 0x7FF.

4. Set the GIE bit to 1 in the interrupt service routine.

2.3.7 EMC reset

In order to prevent the chip registers from being rewritten due to strong interference such as ESD and EFT, CSU32M10/CSU32M11 adds

Shadow registers have an inverse relationship with each other. When the system detects that the inverse relationship between them is not established, a reset signal is generated to reset the chip.

Chip reset.

The shadow registers added in CSU32M10/CSU32M11 include the following registers for verification:

1. WDT module enable bit
2. WWDT module enable bit
3. WDT clock enable bit
4. Code options
5. SLEEP register

The value of the shadow register cannot be read by the user and is only used for verification.

2.3.8 Register Description

Table 2-11 Reset system register list

land site	NameBit7		Bits6	Bit5	Bits4	Bit3	Bits2	Bit1	Bit0	Power-On Reset value
09h RSTSR							EMCF	ILOPF	WWDTF	uuuuu000
40h INTCFG	LVD36	LVD24								xxxxuuuu

2.3.8.1 RSTSR Register (Address 09h)

Table 2-12

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
RSTSR						EMCF	ILOPF	WWDTF

Table 2-13

Bit address identifier		Function
2	EMCF	<p>EMC reset flag</p> <p>This bit is set to 1 by hardware and cleared to 0 by software.</p> <p>0: No EMC reset occurred 1: EMC reset occurred</p>
1	ILOPF	<p>Illegal instruction reset flag</p> <p>This bit is set to 1 by hardware and cleared to 0 by software.</p> <p>0: No illegal instruction reset occurred 1: An illegal instruction reset occurred</p>
0	WWDTF	<p>WWDT reset flag</p> <p>This bit is set to 1 by hardware and cleared to 0 by software.</p>

		0: No WWDT reset occurred 1: A WWDT reset occurred When a WWDT reset occurs in HALT mode, this flag cannot be reset normally.
--	--	---

2.3.8.2 INTCFG register (address 40h)

Table 2-14

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	RX	R-X	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
INTCFG	LVD36	LVD24						INTCFG[2:0]

Table 2-15

Bit address identifier		Function
7	LVD36	3.6V LVD operating voltage flag, only valid when code option LVD_SEL is 2'b10 1: The system operating voltage is lower than 3.6V, indicating that the low voltage detector is in monitoring state 0: The system operating voltage exceeds 3.6V and the low voltage detector does not work.
6	LVD24	2.4V LVD operating voltage flag, only valid when code option LVD_SEL is 2'b01 1: The system operating voltage is lower than 2.4V, indicating that the low voltage detector is in monitoring state 0: The system operating voltage exceeds 2.4V and the low voltage detector does not work.

2.4 Interrupts

2.4.1 Interrupt Overview

CSU32M10/CSU32M11 has 7 interrupt sources and only 1 interrupt entry address 004H. Interrupt-related SFRs: interrupt enable control register INTE and interrupt flag register INTF. Each of these 7 interrupt sources has an interrupt enable and shares a common interrupt enable bit GIE. Their flags are set by hardware and cleared by software.

When the chip responds to an interrupt request, it will save the current PC value on the stack and set the PC to 004H, while clearing the general enable bit GIE.

0, after executing the interrupt service routine, use the RETFIE instruction to return to the previous main program and set GIE to 1.

The CSU32M10/CSU32M11 interrupt system does not support interrupt nesting and has no interrupt priority. Therefore, it is forbidden to set the GIE bit to 1 in the interrupt service routine. If the GIE bit is set to 1 in the interrupt service routine, the hardware will automatically generate a reset request to reset the chip. After the reset is generated, the hardware will automatically set the ILOPF bit of the RSTS register to 1, which needs to be cleared by software.

The interrupt logic block diagram is as follows

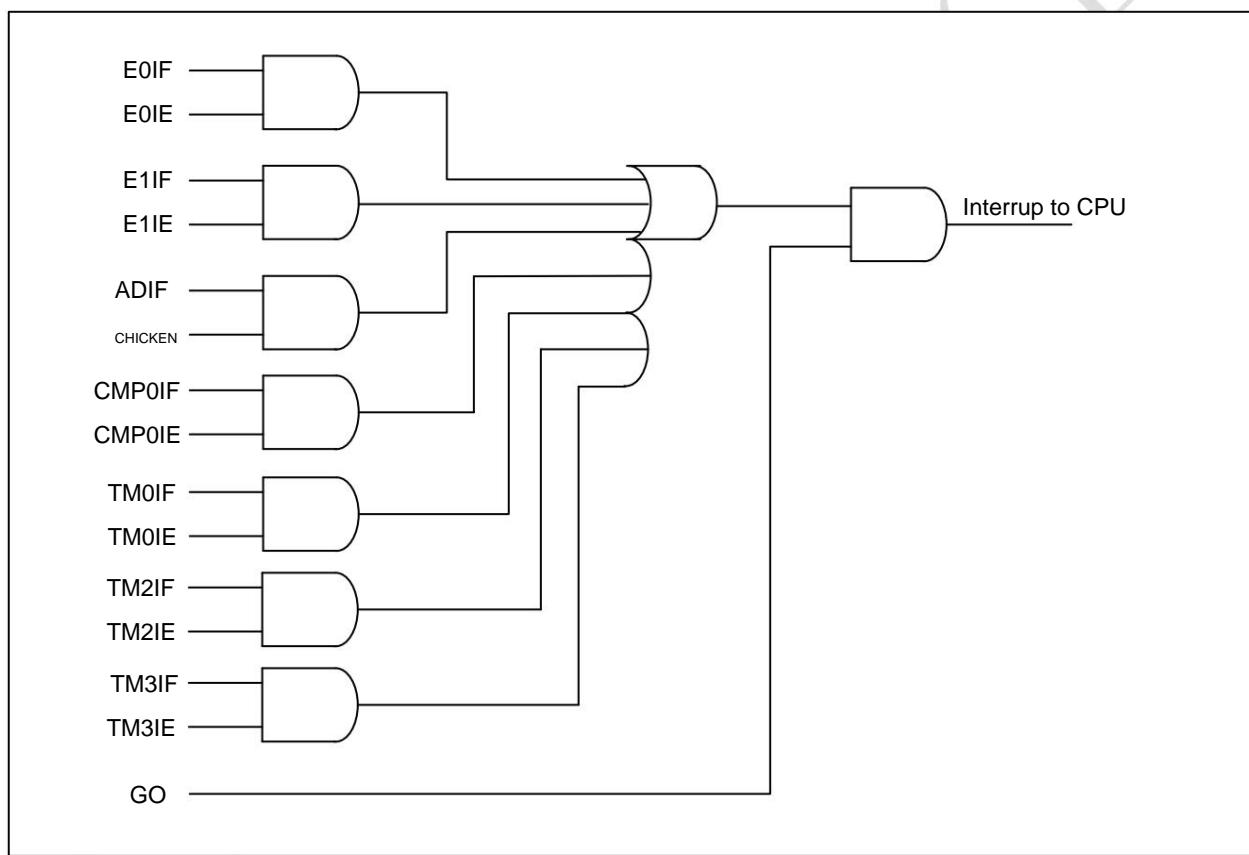


Figure 2-8 Interrupt logic

2.4.2 Interrupt Enable Register

2.4.2.1 INTE register (address 07h)

Table 2-16

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
NOT	GO	TM2IE		TM0IE	S.R.A.D.I.E.		E1IE	E0IE

Table 2-17

Bit address identifier		Function
7	GO	Global Interrupt Enable 1 = Enable all non-maskable interrupts 0 = Disable all interrupts
6	TM2IE	12-Bit Timer/Event Counter 2 Interrupt Enable 1 = Enable Timer/Event Counter 2 interrupt 0 = Disable Timer/Event Counter 2 interrupt
5	RESERVE	reserve
4	TM0IE	8-Bit Timer 0 Interrupt Enable 1 = Enable Timer 0 interrupt 0 = Disable Timer 0 interrupt
3	S.R.A.D.I.E.	SAR_ADC interrupt enable 1 = Enable SAR_ADC interrupt 0 = Disable SAR_ADC interrupt
2	RESERVE	reserve
1	E1IE	External interrupt 1 enable 1 = Enable external interrupt 1 0 = Disable external interrupt 1
0	E0IE	External interrupt 0 enable 1 = Enable external interrupt 0 0 = Disable external interrupt 0

2.4.2.2 INTE2 register (address 3Dh)

Table 2-18

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
INTE2	CMPIE			TM3IE				

Table 2-19

Bit address identifier		Function
7	CMPIE	Comparator Interrupt Enable 1 = Enable comparator interrupt 0 = Do not enable comparator interrupt
6~5	RESERVE	reserve
4	TM3IE	12-Bit Timer/Event Counter 3 Interrupt Enable 1 = Enable Timer/Event Counter 3 interrupt

		0 = Disable Timer/Event Counter 3 interrupt
3y0 RESERVE		reserve

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2.4.3 Interrupt Flag Register

The interrupt flag bits are set to 1 by hardware and cleared to 0 by software. If the corresponding interrupt enable bit is not set to 1, the interrupt flag bit will also be cleared to 0 by software. Therefore, it is recommended to first determine whether the interrupt enable bit is on in the interrupt function, and then determine the corresponding interrupt flag bit. Otherwise, there is a possibility that can cause interrupt function to be executed incorrectly.

2.4.3.1 INTF register (address 06h)

Table 2-20

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INTF		TM2IF		TM0IF	SRADIF		E1IF	E0IF

Table 2-21

Bit address identifier		Functionality
7	RESERVE	Retention
6	TM2IF	12-Bit Timer/Counter 2 Interrupt Flag, Cleared by Software, Set by Hardware 1 = A timer interrupt occurs, must be cleared to 0 by software 0 = No timer interrupt occurred
5	RESERVE	reserve
4	TM0IF	8-Bit Timer 0 interrupt flag, cleared by software and set by hardware 1 = A timer interrupt occurs, must be cleared to 0 by software 0 = No timer interrupt occurred
3	SRADIF	AD interrupt flag, cleared by software and set by hardware 1 = AD interrupt occurs, must be cleared to 0 by software 0 = No AD interrupt occurred
2	RESERVE	reserve
1	E1IF	External interrupt 1 interrupt flag, cleared by software and set by hardware 1 = External interrupt 1 An interrupt occurs and must be cleared by software 0 = External interrupt 1 No interrupt occurred
0	E0IF	External interrupt 0 interrupt flag, cleared by software and set by hardware 1 = External interrupt 0 occurs, must be cleared by software 0 = External interrupt 0 No interrupt occurred

2.4.3.2 INTF2 register (address 3Ch)

Table 2-22

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R	W-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
INTF2	CMPIF			TM3IF				

Table 2-23

Bit address identifier		Function
7	CMPIF	Comparator interrupt flag, cleared by software and set by hardware 1 = A comparator interrupt has occurred, must be cleared to 0 by software 0 = No comparator interrupt occurred
6~5	RESERVE	reserve



Gathering tiny bits of information together to form a vast ocean

4	TM3IF	12-Bit Timer/Counter 3 Interrupt Flag, Cleared by Software, Set by Hardware 1 = A timer interrupt occurs, must be cleared to 0 by software 0 = No timer interrupt occurred
3y0	RESERVE	reserve

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2.4.4 External Interrupt 0

PT1.0 is the input terminal of external interrupt 0. The trigger mode is determined by the E0M[1:0] register in the PT1CON register. E0IE in the register is the enable bit of external interrupt 0, and E0IF in the INTF register is the interrupt flag bit, which is set to 1 by hardware and cleared to 0 by software. sleep or halt mode. Whenever PT1.0 is triggered, the interrupt flag E0IF will be set to 1.

2.4.4.1 PT1CON Register (Address 23h)

Table 2-24

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT1CON	PT11OD	PT1W[3:0]				E1M	E0M[1:0]	

Table 2-25

Bit address identifier		
2	E1M	Function External interrupt 1 Trigger mode 1 = External interrupt 1 is triggered by falling edge 0 = External interrupt 1 is triggered when the state changes
1y0	E0M[1:0]	External interrupt 0 trigger mode 11 = External interrupt 0 is triggered when the state changes 10 = External interrupt 0 is triggered when the state changes 01 = External interrupt 0 is triggered by rising edge 00 = External interrupt 0 is triggered by falling edge

2.4.5 External Interrupt 1

PT1.1, PT1.3, PT1.4, PT1.5, PT1.6, PT3.0, PT3.1, PT3.2, PT3.3, PT3.4 can all be used as external interrupts. The trigger mode is determined by the E1M register in the PT1CON register. The E1IE register in the INTF register is the external interrupt 1 input. Enable bit, E1IF in the INTF register is the interrupt flag bit, which is set to 1 by hardware and cleared to 0 by software. It can wake up the sleep or halt mode. The corresponding PT port is used as the external interrupt input terminal, and when external interrupt 1 is triggered, the interrupt flag E1IF will be set to 1.

2.4.5.1 PT1CON Register (Address 23h)

Table 2-26

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT1CON	PT11OD	PT1W[3:0]				E1M	E0M[1:0]	

Table 2-27

Bit address identifier		Function
6	PT1W[3]	PT1.5 External interrupt 1 enable 0 = Disable PT1.5 external interrupt 1 1 = Enable PT1.5 external interrupt 1
5	PT1W[2]	PT1.4 External interrupt 1 enable 0 = Disable PT1.4 external interrupt 1 1 = Enable PT1.4 external interrupt 1
4	PT1W[1]	PT1.3 External interrupt 1 enable

		0 = Disable PT1.3 external interrupt 1 1 = Enable PT1.3 external interrupt 1
3	PT1W[0]	PT1.1 External interrupt 1 enable 0 = Disable PT1.1 external interrupt 1 1 = Enable PT1.1 external interrupt 1

2.4.5.2 METCH1 Register (Address 2Eh)

Table 2-28

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
METCH1	P3HINV P3LINV		PT1W[6:4]		PWM2PO	PWM2PO1		

Table 2-29

Bit address identifier		Function
5	PT1W[6]	PT3.2 External interrupt 1 enable 0 = Disable PT3.2 external interrupt 1 1 = Enable PT3.2 external interrupt 1
4	PT1W[5]	PT3.1 External interrupt 1 enable 0 = Disable PT3.1 external interrupt 1 1 = Enable PT3.1 external interrupt 1
3	PT1W[4]	PT3.0 external interrupt 1 enable 0 = Disable PT3.0 external interrupt 1 1 = Enable PT3.0 external interrupt 1

2.4.5.3 INTCFG Register (Address 40h)

Table 2-30

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics RX		R-X	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
INTCFG	LVD36	LVD24					INTCFG[2:0]	

Table 2-31

Bit address identifier		Functionality
7:3	RESERVE	Retention
2	INTCFG [2]	PT3.4 External interrupt 1 enable 0 = Disable PT3.4 external interrupt 1 1 = Enable PT3.4 external interrupt 1
1	INTCFG [1]	PT3.3 External interrupt 1 enable 0 = Disable PT3.3 external interrupt 1 1 = Enable PT3.3 external interrupt 1
0	INTCFG [0]	PT1.6 External interrupt 1 enable 0 = Disable PT1.6 external interrupt 1 1 = Enable PT1.6 external interrupt 1

2.4.6 AD Interrupt Overflow

SRADIE in the INTE register is the enable bit for the ADC interrupt, and SRADIF in the INTF register is the interrupt flag bit.

0. When the ADC conversion is complete, SRADIF will be set to 1 by hardware.

2.4.7 Comparator Interrupt

CMPIE in the INTE2 register is the enable bit for the comparator interrupt, and CMPIF in the INTF2 register is the comparator interrupt flag bit.

Cleared by software. CMPIF is set to 1 by hardware when the comparator result changes.

2.4.8 Timer 0 overflow interrupt

TM0IE in the INTE register is the enable bit for the timer 0 interrupt, and TM0IF in the INTF register is the interrupt flag bit. The software clears the interrupt flag bit.

0. When Timer 0 overflows, TM0IF will be set to 1 by hardware.

2.4.9 Timer/Event Counter 2 Overflow Interrupt

TM2IE in the INTE register is the enable bit for the timer/counter 2 interrupt, and TM2IF in the INTF register is the interrupt flag bit.

Cleared by software. When Timer/Event Counter 2 overflows, TM2IF will be set to 1 by hardware.

2.4.10 Timer/Event Counter 3 Overflow Interrupt

TM3IE in the INTE register is the enable bit for the timer/counter 3 interrupt, and TM3IF in the INTF register is the interrupt flag.

When the Timer/Event Counter 3 overflows, TM3IF will be set to 1 by hardware.

2.4.11 PUSH and POP Processing

CSU32M10/CSU32M11 has 8 levels of PUSH and POP stacks. After an interrupt request is responded to, the program jumps to 004h to execute the subroutine. Before responding to an interrupt, the flags in WORK and STATUS must be saved (only C, DC, and Z are saved). Before exiting the interrupt,

Use POP instruction to pop the stack. The chip provides PUSH and POP instructions for stack storage and stack recovery, thus avoiding the interruption after the end of the Program running error. The PUSH and POP instructions can also be used in the subroutine to save and restore WORK and STATUS (C, DC, Z).

PUSH and POP must appear in pairs.

2.4.12 Interrupt function processing

The CSU32M10/CSU32M11 interrupt response has no interrupt priority level and only has one interrupt entry address 004h.

The hardware can also set the interrupt enable bit when it is not enabled. Therefore, it is recommended to first determine the interrupt enable bit before determining the interrupt flag bit.

If the enable is always on, you can ignore this suggestion.

When clearing an interrupt flag, it is recommended to use the BCF instruction to clear a single interrupt flag instead of using the CLRINTF instruction.

Clear the line to avoid clearing other interrupt flags by mistake.

2.4.13 SLEEP/HALT wakeup

Not all interrupts in CSU32M10/CSU32M11 can wake up SLEEP mode. The interrupts that can wake up SLEEP mode are as follows:

- ÿ External interrupt 0
- ÿ External interrupt 1
- ÿ Timer 0 (can wake up SLEEP only when using WDT clock as clock source and WDT clock is turned on)

In HALT mode, since the peripheral clocks are not shut down, all interrupts can wake up HALT mode.

```

...
ORG 004H
GOTO int_server
...

int_server:
PUSH
BTFS S INTE,E0IE ; Check external interrupt 0 interrupt enable
GOTO $+3
BTFS C INTF,E0IF; Determine external interrupt 0 flag
GOTO ex0_int

BTFS S INTE,E1IE ; Check external interrupt 1 interrupt enable
GOTO $+3
BTFS C INTF,E1IF ; Determine external interrupt 1 flag
GOTO ex1_int

BTFS S INTE,TM0IE ; Check if timer/counter 0 interrupt is enabled
GOTO $+3
BTFS C INTF,TM0IF; Determine the timer 0 interrupt flag
GOTO tm0_int

BTFS S INTE,TM2IE ; Check whether timer/counter 2 interrupt is enabled
GOTO $+3
BTFS C INTF,TM2IF; Determine the interrupt flag of timer/counter 2
GOTO tm2_int

BTFS S INTE,TM3IE ; Check whether timer/counter 3 interrupt is enabled
GOTO $+3
BTFS C INTF,TM3IF; Determine the interrupt flag of timer/counter 3
GOTO tm3_int
...

ex0_int:
BCF INTF, E1IF ; Clear E1IF
...
POP
RETFIE
...

```

2.5 Timer 0

2.5.1 Timer 0 Overview

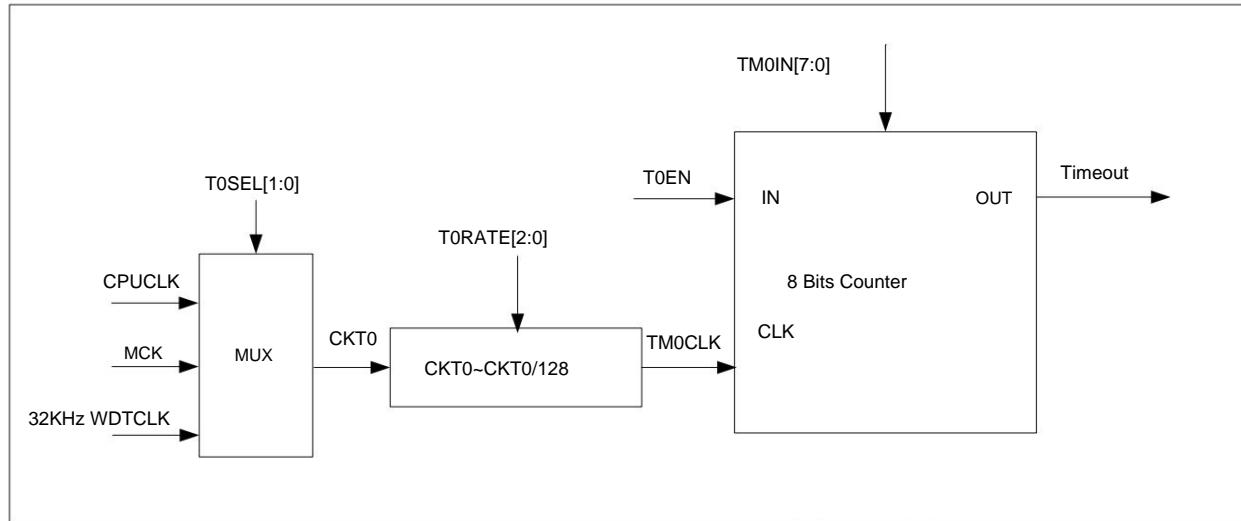


Figure 1 Timer 0 functional block diagram

The input clock of the Timer 0 module is selected by T0SEL[1:0]. The optional clock sources are CPUCLK, MCK or internal 32K WDT clock. When the internal 32K WDT clock is selected for counting, the Sleep mode can be awakened. The Timer 0 module integrates a frequency divider. The divided clock TM0CLK is used as the input clock of the 8-bit counter.

When the user sets the enable bit of the Timer 0 module, the 8-bit counter will start and the count value will increase from 000H to TM0IN. The user needs to set TM0IN (Timer 0 module count overflow value) to select the timer timeout interrupt time.

When a timer timeout occurs, the Timer 0 interrupt flag TM0IF is set to 1 by hardware. This bit can only be cleared by software. If the Timer 0 interrupt (TM0IE=1) and the interrupt general enable (GIE) are enabled, the program counter will jump to 004H to execute the interrupt service routine.

2.5.2 Timer 0 Register List

Table 2-32

Address	Name	Bit7		Bit6	Bit5	Bit4	Bit3		Bit2	Bit1	Bit0	Power-on reset
												Place value
06h	INTF			TM2IF			TM0IF SRADIF			E1IF	E0IF	00u00
07h	NOT		GO	TM2IE			TM0IE SRADIE			E1IE	E0IE	00u00
0Fh	TM0CON	10h	T0EN	T0RATE[2:0]				T0RSTB	T0SEL[1:0]			0000u100
TM0IN	11h			TM0IN[7:0]								11111111
TM0CNT				TM0CNT[7:0]								00000000

2.5.2.1 TM0CON register (address 0Fh)

Table 2-33

Bit number	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
TM0CON	T0EN	T0RATE[2:0]				T0RSTB	T0SEL[1:0]	

Table 2-34

Bit address identifier																					
7	T0EN	Function timer 0 enable bit 1: Enable timer 0 0: Disable timer 0																			
6:4	T0RATE[2:0]	Timer 0 clock division selection, where CKT0 is the clock selected by T0SEL[1:0] source. <table border="1"> <tr><th>T0RATE [2:0]</th><th>TM0CLK</th></tr> <tr><td>000</td><td>CKT0</td></tr> <tr><td>001</td><td>CKT0/2</td></tr> <tr><td>010</td><td>CKT0/4</td></tr> <tr><td>011</td><td>CKT0/8</td></tr> <tr><td>100</td><td>CKT0/16</td></tr> <tr><td>101</td><td>CKT0/32</td></tr> <tr><td>110</td><td>CKT0/64</td></tr> <tr><td>111</td><td>CKT0/128</td></tr> </table>		T0RATE [2:0]	TM0CLK	000	CKT0	001	CKT0/2	010	CKT0/4	011	CKT0/8	100	CKT0/16	101	CKT0/32	110	CKT0/64	111	CKT0/128
T0RATE [2:0]	TM0CLK																				
000	CKT0																				
001	CKT0/2																				
010	CKT0/4																				
011	CKT0/8																				
100	CKT0/16																				
101	CKT0/32																				
110	CKT0/64																				
111	CKT0/128																				
2	T0RSTB	Timer 0 reset, default value is 1 1: Disable timer 0 reset 0: Enable timer 0 reset When this bit is set to 0, Timer 0 reset is completed after one instruction cycle, and T0RSTB hardware Set to 1.																			
1:0	T0SEL[1:0]	Clock source selection <table border="1"> <tr><th>T0SEL[1:0] Timer 0 clock source</th><th></th></tr> <tr><td>00</td><td>CPUCLK</td></tr> <tr><td>01</td><td>MCK</td></tr> <tr><td>1x</td><td>Internal 32K WDT clock, Only valid when the internal WDT crystal oscillator is turned on.</td></tr> </table>		T0SEL[1:0] Timer 0 clock source		00	CPUCLK	01	MCK	1x	Internal 32K WDT clock, Only valid when the internal WDT crystal oscillator is turned on.										
T0SEL[1:0] Timer 0 clock source																					
00	CPUCLK																				
01	MCK																				
1x	Internal 32K WDT clock, Only valid when the internal WDT crystal oscillator is turned on.																				

2.5.2.2 TM0IN register (address 10h)

Table 2-35

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R	W-1	R/W-1						
TM0IN	TM0IN[7:0]							

Table 2-36

Bit address identifier function	
7:0 TM0IN[7:0] Timer 0 overflow value (overflow value: 1~255)	

2.5.2.3 TM0CNT register (address 11h)

Table 2-37

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R-0		R-0						
TM0CNT	TM0CNT[7:0]							

Table 2-38

Bit address identifier	Function
7:0 TM0CNT[7:0]	Timer 0 count register, read only

2.5.3 Timing function

The clock source of Timer 0 can be selected from CPUCLK, MCK, or internal 32K WDT clock.

When counting, the Sleep mode can be awakened.

The timing function operation steps are as follows. Operation:

- 1) Set the lower 2 bits of TM0CON to select the clock input for the Timer0 module.
- 2) Set TM0IN and select the overflow value of timer 0. (Overflow value: 1~255)
- 3) Clear the Timer 0 interrupt flag: Clear the TM0IF bit in the INTF register to 0.
- 4) Set Timer 0 interrupt enable: Set the TM0IE bit and GIE bit in the INTE register to enable Timer 0 interrupt.
- 5) Clear the Timer 0 count value: Set the T0RSTB bit in the TM0CON register to 0 to reset the Timer 0 module counter.
- 6) Enable the Timer 0 module: Set the T0EN bit in the TM0CON register to enable the 8-bit counter of the Timer 0 module.
- 7) When the timer timeout occurs, the program counter will jump to 004H.

Timer 0 overflow time calculation method:

$$\text{Timer 0 overflow time} = (\text{TM0IN}+1)/\text{TM0CLK}.$$

2.6 I/O PORT

Table 2-39 I/O port register table

Address	Name	Bit7		Bit6 Bit5		Bit4	Bit3	Bit2	Bit1	Bit0	Power on Place value
20h	PT1					PT1[5:3]			PT1[1:0]		uuxxxxxx
21h	PT1EN					PT1EN[6:3]			PT1EN[1:0]	uu0000u00	
22h	PT1PU					PT1PU[6:3]			PT1PU[1:0]	uu0000u00	
23h	PT1CON PT11OD					PT1W[3:0]		E1M	E0M[1:0]		00000000
28h	PT3						PT3[5:0]				uuuxxxxx
29h	PT3EN						PT3EN[5:0]				uu000000
2Ah	PT3PU						PT3PU[5:0]				uu000000
2Bh	PT3CON						PT3CON[5:0]				uu000000
30h	PT5								PT5[1:0]		uuuuuuuxx
31h	PT5EN								PT5EN[1:0]	uuuuuuu00	
32h	PT5PU								PT5PU[1:0]	uuuuuuu00	
33h	PT5CON								PT51OD PT50OD	uuuuuuu00	
41h	PT1CON1								PT1CON[0]		uuuuuuu0
42h	PT1PD					PT1PD[6:3]			PT1PD[1:0]	u0000u00	
43h	PT3PD						PT3PD[5:0]				uu000000
44h	PT5PD								PT5PD[1:0]	uuuuuuu0	

The general purpose I/O port (GPIO) in the microcontroller is used for general input and output functions. Users can receive data signals through GPIO Or transmit data to other digital devices. Some GPIOs of CSU32M10/CSU32M11 can be defined as other special functions.

This section only describes the general I/O port functions of GPIO. Special functions will be described in the following sections.

2.6.1 GPIO pull-up and pull-down resistors

All GPIOs of CSU32M10/CSU32M11 support internal pull-up and pull-down resistors. The pull-up and pull-down resistors are both 30K Ω . When GPIO is configured as an analog port, the pull-up and pull-down resistors inside the chip are automatically disconnected.

When GPIO is configured as a digital output port, the pull-up and pull-down resistors will not be automatically disconnected.

In addition to the above general pull-down resistors, PT3.4 and PT5.1 can be configured with 10 K Ω pull-down resistors, and PT1.0 can be configured with 3 K Ω pull-down resistors. The PT1.3 port can be configured with a 400K Ω pull-down resistor. The above pull-down resistor is configured through the code option bit PD_OP.

When the 30 K Ω pull-down of the GPIO and the pull-down controlled by the code option are turned on at the same time, the two are in parallel relationship.

2.6.2 PT1 port

2.6.2.1 PT1 register (address 20h)

Table 2-40

Bit number	Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0			R/W-X	R/W-X	R/W-X	R/W-X	U-0	R/W-X	R/W-X
PT1					PT1[6:3]				PT1[1:0]

Table 2-41

Bit address identifier		Functionality
7	RESERVE	Retention
6:3 PT1[6:3]		PT1 port bit6~bit4 data bit Read GPIO value when performing a read operation Perform write operation to configure the GPIO port output value.
2	RESERVE	reserve
1~0	PT1[1:0]	PT1 port bit1~bit0 data bit Read GPIO value when performing a read operation Perform write operation to configure the GPIO port output value.

2.6.2.2 PT1EN register (address 21h)

Table 2-42

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PT1EN		PT1EN[6:3]					PT1EN[1:0]	

Table 2-43

Bit address identifier 7		Functionality
	RESERVE	Retention
6	PT1EN[6]	PT1.6 port input and output control bit 0 = Defined as input port 1 = Defined as output port
5	PT1EN[5]	PT1.5 port input and output control bits 0 = Defined as input port 1 = Defined as output port
4	PT1EN[4]	PT1.4 port input and output control bit 0 = Defined as input port 1 = Defined as output port
3	PT1EN[3]	PT1.3 port input and output control bit 0 = Defined as input port 1 = Defined as open drain output
2	RESERVE	reserve
1	PT1EN[1]	PT1.1 port input and output control bit 0 = Defined as input port 1 = Defined as output port
0	PT1EN[0]	PT1.0 port input and output control bit 0 = Defined as input port 1 = Defined as output port

2.6.2.3 PT1PU register (address 22h)

Table 2-44

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PT1PU		PT1PU[6:3]					PT1PU[1:0]	

Table 2-45

Bit address identifier		Functionality
7	RESERVE	Retention
6	PT1PU[6]	PT1.6 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
5	PT1PU[5]	PT1.5 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
4	PT1PU[4]	PT1.4 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
3	PT1PU[3]	PT1.3 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
2	RESERVE	reserve
1	PT1PU[1]	PT1.1 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
0	PT1PU[0]	PT1.0 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port

2.6.2.4 PT1CON Register (Address 23h)

Table 2-46

Bit number	Bit7 Characteristic	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT1CON	PT11OD		PT1W[3:0]			E1M		E0M[1:0]

Table 2-47

Bit address identifier		Function
7	PT11OD	PT1.1 open-drain enable bit 0 = Disable PT1.1 open drain 1 = Enable PT1.1 open drain
6	PT1W[3]	PT1.5 External interrupt 1 enable 0 = Disable PT1.5 external interrupt 1 1 = Enable PT1.5 external interrupt 1
5	PT1W[2]	PT1.4 External interrupt 1 enable 0 = Disable PT1.4 external interrupt 1 1 = Enable PT1.4 external interrupt 1
4	PT1W[1]	PT1.3 External interrupt 1 enable 0 = Disable PT1.3 external interrupt 1

		1 = Enable PT1.3 external interrupt 1
3	PT1W[0]	PT1.1 External interrupt 1 enable 0 = Disable PT1.1 external interrupt 1 1 = Enable PT1.1 external interrupt 1
2	E1M	External interrupt 1 trigger mode 1 = External interrupt 1 is triggered by falling edge 0 = External interrupt 1 is triggered when the state changes
1y0	E0M[1:0]	External interrupt 0 trigger mode 11 = External interrupt 0 is triggered when the state changes 10 = External interrupt 0 is triggered when the state changes 01 = External interrupt 0 is triggered by rising edge 00 = External interrupt 0 is triggered by falling edge

2.6.2.5 PT1CON1 Register (Address 41h)

Table 2-48

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
PT1CON1								PT1CON[0]

Table 2-49

Bit address identifier	Functionality
7y1 RESERVE	Retention
0	GPIO1bit 0 I/O control bit 0 = Defined as digital port 1 = Defined as analog port

2.6.2.6 PT1PD register (address 42h)

Table 2-50

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PT1PD				PT1PD[6:3]				PT1PD[1:0]

Table 2-51

Bit address identifier	Functionality
7	RESERVE
6	PT1PD[6] PT1.6 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
5	PT1PD[5] PT1.5 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
4	PT1PD[4] PT1.4 port pull-down resistor enable bit 0 = disconnect the pull-down resistor

		1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
3	PT1PD[3]	PT1.3 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
2	RESERVE	reserve
1	PT1PD[1]	PT1.1 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
0	PT1PD[0]	PT1.0 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port

2.6.3 PT3 port

2.6.3.1 PT3 register (address 28h)

Table 2-52

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
PT3					PT3[5:0]			

Table 2-53

Bit address identifier	Functionality
7:6 RESERVE	Retention
5:0 PT3[5:0]	PT3 port bit5~bit0 data bit Read GPIO value when performing a read operation Perform write operation to configure the GPIO port output value.

2.6.3.2 PT3EN Register (Address 29h)

Table 2-54

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT3EN					PT3EN[5:0]			

Table 2-55

Bit address identifier	Functionality
7:6	RESERVE
5	PT3.5 port input and output control bits 0 = Defined as input port 1 = Defined as output port
4	PT3.4 port input and output control bits 0 = Defined as input port 1 = Defined as output port
3	PT3.3 port input and output control bits 0 = Defined as input port 1 = Defined as output port
2	PT3.2 port input and output control bits 0 = Defined as input port 1 = Defined as output port
1	PT3.1 port input and output control bits 0 = Defined as input port 1 = Defined as output port
0	PT3.0 port input and output control bits 0 = Defined as input port 1 = Defined as output port

2.6.3.3 PT3PU register (address 2Ah)

Table 2-56

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT3PU								PT3PU[5:0]

Table 2-57

Bit address identifier		Functionality
7:6	RESERVE	Retention
5	PT3PU[5]	<p>PT3.5 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>
4	PT3PU[4]	<p>PT3.4 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>
3	PT3PU[3]	<p>PT3.3 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>
2	PT3PU[2]	<p>PT3.2 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>
1	PT3PU[1]	<p>PT3.1 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>
0	PT3PU[0]	<p>PT3.0 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>

2.6.3.4 PT3CON Register (Address 2Bh)

Table 2-58

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PT3CON								PT3CON[5:0]

Table 2-59

Bit address identifier		Functionality
7:6 RESERVE		Retention
5	PT3CON[5]	<p>PT3.5 port control bit 0 = Defined as digital port 1 = Defined as analog port</p>
4	PT3CON[4]	<p>PT3.4 port control bit 0 = Defined as digital port</p>

		1 = Defined as analog port
3	PT3CON[3]	PT3.3 port control bit 0 = Defined as digital port 1 = Defined as analog port
2	PT3CON[2]	PT3.2 port control bit 0 = Defined as digital port 1 = Defined as analog port
1	PT3CON[1]	PT3.1 port control bit 0 = Defined as digital port 1 = Defined as analog port
0	PT3CON[0]	PT3.0 port control bit 0 = Defined as digital port 1 = Defined as analog port

2.6.3.5 PT3PD register (address 43h)

Table 2-60

Bit number	Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
U-0			U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PT3PD			PT3PD[5:0]								

Table 2-61

Bit address identifier		Functionality
7:6	RESERVE	Retention
5	PT3PD[5]	PT3.5 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
4	PT3PD[4]	PT3.4 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
3	PT3PD[3]	PT3.3 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
2	PT3PD[2]	PT3.2 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
1	PT3PD[1]	PT3.1 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port
0	PT3PD[0]	PT3.0 port pull-down resistor enable bit 0 = disconnect the pull-down resistor 1 = Enable pull-down resistor GPIO port pull-down resistor is automatically disconnected when configured as an analog port

2.6.4 PT5 port

2.6.4.1 PT5 register (address 30h)

Table 2-62

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	R/W-X	R/W-X
PT5							PT5[1:0]	

Table 2-63

Bit address identifier		Functionality
7y2 RESERVE		Retention
1y0	PT5[1:0]	PT5 port bit1~bit0 data bit Read GPIO value when performing a read operation Perform write operation to configure the GPIO port output value.

2.6.4.2 PT5EN register (address 31h)

Table 2-64

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PT5EN							PT5EN[1:0]	

Table 2-65

Bit address identifier		Functionality
7y2 RESERVE		Retention
1	PT5EN[1]	PT5.1 port input and output control bit 0 = Defined as input port 1 = Defined as output port
0	PT5EN[0]	PT5.0 port input and output control bit 0 = Defined as input port 1 = Defined as output port

2.6.4.3 PT5PU register (address 32h)

Table 2-66

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PT5PU							PT5PU[1:0]	

Table 2-67

Bit address identifier 7:2		Functionality
	RESERVE	Retention
1	PT5PU[1]	PT5.1 port pull-up resistor enable bit 0 = disconnect the pull-up resistor 1 = Enable pull-up resistor

		The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port
0	PT5PU[0]	<p>PT5.0 port pull-up resistor enable bit</p> <p>0 = disconnect the pull-up resistor</p> <p>1 = Enable pull-up resistor</p> <p>The pull-up resistor of the GPIO port is automatically disconnected when it is configured as an analog port</p>

2.6.4.4 PT5CON Register (Address 33h)

Table 2-68

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PT5CON							PT51OD	PT50OD

Table 2-69

Bit address identifier		Functionality
7:2	RESERVE	Retention
1	PT51OD	<p>PT5.1 port open drain enable bit</p> <p>0 = Open-drain output disabled</p> <p>1 = Enable open-drain output</p>
0	PT50OD	<p>PT5.0 port open drain enable bit</p> <p>0 = Open-drain output disabled</p> <p>1 = Enable open-drain output</p>

2.6.4.5 PT5PD register (address 44h)

Table 2-70

Bit number Bit7	Feature	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
U-0		U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PT5PD							PT5PD[1:0]	

Table 2-71

Bit address identifier		Functionality
7:2	RESERVE	Retention
1	PT5PD[1]	<p>PT5.1 port pull-down resistor enable bit</p> <p>0 = disconnect the pull-down resistor</p> <p>1 = Enable pull-down resistor</p> <p>GPIO port pull-down resistor is automatically disconnected when configured as an analog port</p>
0	PT5PD[0]	<p>PT5.0 port pull-down resistor enable bit</p> <p>0 = disconnect the pull-down resistor</p> <p>1 = Enable pull-down resistor</p> <p>GPIO port pull-down resistor is automatically disconnected when configured as an analog port</p>

3 Enhancements

3.1 Halt and Sleep Modes

CSU32M10/CSU32M11 supports low power operation mode. To put CSU32M10/CSU32M11 in standby mode, you can let the CPU

Stopping operation puts the CSU32M10/CSU32M11 into stop mode or sleep mode to reduce power consumption. These two modes are described as follows:

Stop Mode After

the CPU executes the stop instruction, the program counter stops counting until an interrupt event occurs. In stop mode, the internal high-speed oscillator of the chip

The internal 32KHz WDT clock still works normally, the core clock stops, the timer can count normally, and the ADC can continue to process.

Completed conversion.

Sleep Mode After

the CPU executes the sleep instruction, all oscillators stop working until an interrupt event occurs to wake up the CPU.

Consumes about 1uA.

In order to minimize the power consumption of the CPU in sleep mode, it is necessary to ensure that all input ports are connected to VDD before executing the sleep instruction.

The ADC module must be turned off in SLEEP mode, and the analog input channel cannot be configured as 1/8 VDD (SRADCON2 register

The CHS[3:0] bits of the register cannot be configured as 0101).

Note:

If the chip is in sleep state, the voltage is reduced at this time. The 2.4V low voltage reset will not work. If it is lower than 2.0V, the power-off reset will

If the device is still below the low voltage reset point after waking up from sleep, it will be reset immediately.

Halt demonstration program:

```

...
MOVLW 08h
MOVWF pt1up ; disconnect the pull-up resistors of all interfaces except bit3 (pt1[3]) of pt1
MOVLW 0f7h
MOVWF pt1en; pt1 port except bit3 (pt1[3]) as input port
CLRF pt1      ; Output pt1[4:1] as low
CLRF pt3up ; disconnect pt3 pull-up resistor
CLRF pt3en     ; pt3 port is used as input port
CLRF pt3con; pt3 port is used as a digital port
CLRF pt3      ; Output pt3 as low
CLRF pt5up; disconnect pt5 pull-up resistor
CLRF pt5en ;      ; pt5 port is used as input port
CLRF pt5      Output pt5 as low
CLRF intf ; Clear interrupt flag
MOVLW 81h
MOVWF inte ; Enable external interrupt 0
halt       ;Enter stop mode
...

```

Sleep Demonstration Program:

```

...
MOVLW 08h
MOVWF pt1up ; disconnect the pull-up resistors of all interfaces except bit3 (pt1[3]) of pt1
MOVLW 0f7h
MOVWF pt1en; pt1 port except bit3 (pt1[3]) as input port
CLRF pt1      ; Output pt1[4:1] as low
CLRF pt3up ; disconnect pt3 pull-up resistor
CLRF pt3en     ; pt3 port is used as input port
CLRF pt3con; pt3 port is used as a digital port
CLRF pt3      ; Output pt3 as low
CLRF pt5up; disconnect pt5 pull-up resistor
CLRF pt5en ;      ; pt5 port is used as input port
CLRF pt5      Output pt5 as low
CLRF intf ; Clear interrupt flag
MOVLW 81h
MOVWF inte ; Enable external interrupt 0
sleep      ; Enter sleep mode
...

```

3.2 Watchdog (WDT)

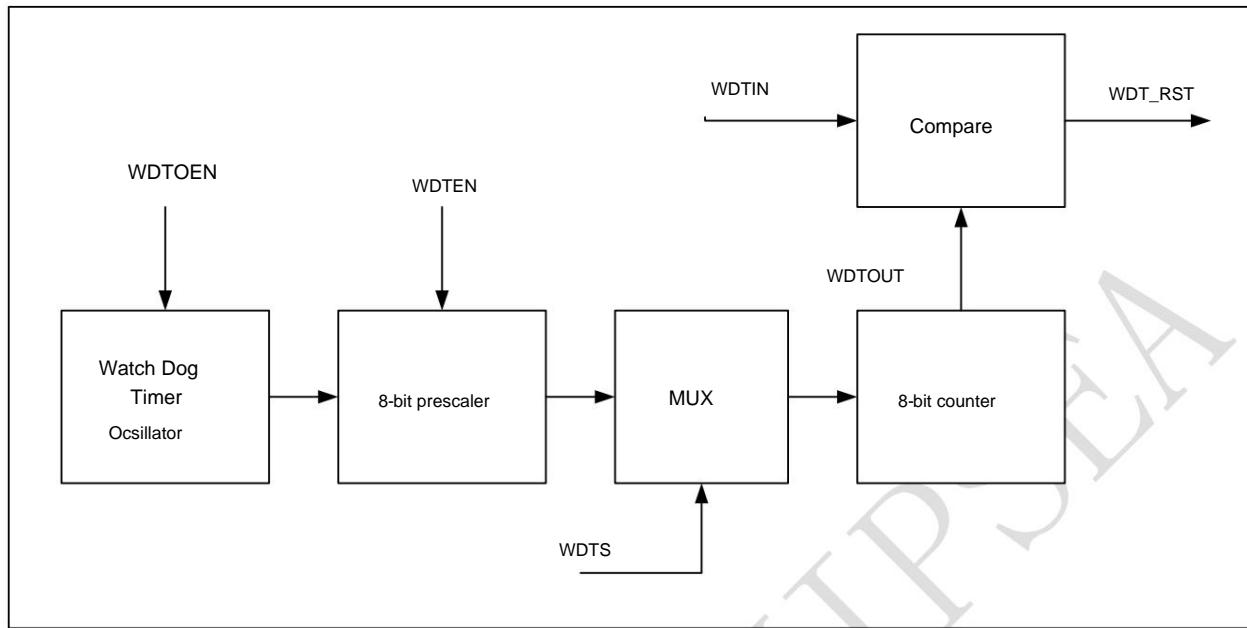


Figure 3-1 Watchdog timer function block diagram

The watchdog timer (WDT) is used to prevent the program from losing control due to some uncertain factors. When the WDT is enabled, the WDT counts down. After the timeout, the CPU will be reset. The running program usually clears the WDT count value before the WDT resets the CPU.

When the WDT count value is cleared, the program does not clear the WDT count value, and the CPU is reset to normal state after the WDT timing expires.

The WDT module enable and 32KHz WDT clock enable are controlled by the code option WDT_CFG. When this bit is set to 0, the WDT module enable and The 32KHz WDT clock enable is fixed on and cannot be turned off by software; when this bit is set to 1, the WDT module enable is controlled by WDTEN and the 32KHz WDT clock enable is controlled by CST_WDT.

When the user clears CST_WDT to 0, the internal watchdog timer oscillator (32KHz) will start and the generated clock will be sent to the 8-bit prescaler counter. When the user sets WDTEN, the 8-bit prescaler counter starts counting. The prescaler clock is controlled by WDTS[2:0]. The multiplexer is used to select the WDT counter clock. When the 8-bit counter count value is equal to the WDTIN value, the overflow occurs. When it is out, it will send WDTOUT signal to reset CPU and set TO flag. User can use instruction CLRWDT to reset WDT.

3.2.1 Watchdog Timer Register Table

Table 3-1

Address	Name	Bit7		Bit6	Bit5	Bit4		Bit3	Bit2	Bit1	Bit0	Power-on reset			value
04H	STATUS	LVD24				PD	TO	DC	C			WDT[2:0]		xuu00000	
0Dh	WDTCON	WDTEN										WDTS[2:0]		0uuuu000	
0Eh	WDTIN													11111111	

3.2.1.1 WDTCON Register (Address 0Dh)

Table 3-2

Bit number	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
WDTCON	WDTEN							WDTS[2:0]

Table 3-3

Bit address identifier																				
7	WDTEN	Function Watchdog enable bit, high level is effective. When WDT_CFG is configured as WDT module is always on, this bit is invalid. 0: Disable WDT module 1: Enable WDT module																		
6:3 Reserved		reserve																		
2:0 WDTS[2:0]		WDT count clock division <table border="1" data-bbox="568 511 1055 850"> <thead> <tr> <th>WDTS [2:0]</th><th>WDT count clock</th></tr> </thead> <tbody> <tr><td>000</td><td>WDTCLK /256</td></tr> <tr><td>001</td><td>WDTCLK /128</td></tr> <tr><td>010</td><td>WDTCLK /64</td></tr> <tr><td>011</td><td>WDTCLK /32</td></tr> <tr><td>100</td><td>WDTCLK /16</td></tr> <tr><td>101</td><td>WDTCLK /8</td></tr> <tr><td>110</td><td>WDTCLK /4</td></tr> <tr><td>111</td><td>WDTCLK /2</td></tr> </tbody> </table>	WDTS [2:0]	WDT count clock	000	WDTCLK /256	001	WDTCLK /128	010	WDTCLK /64	011	WDTCLK /32	100	WDTCLK /16	101	WDTCLK /8	110	WDTCLK /4	111	WDTCLK /2
WDTS [2:0]	WDT count clock																			
000	WDTCLK /256																			
001	WDTCLK /128																			
010	WDTCLK /64																			
011	WDTCLK /32																			
100	WDTCLK /16																			
101	WDTCLK /8																			
110	WDTCLK /4																			
111	WDTCLK /2																			

3.2.1.2 WDTIN register (address 0EH)

Table 3-4

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WDTIN	WDT_IN[7:0]							

Table 3-5

Bit address identifier		Function
7:0 WDT_IN[7:0]		WDT count input, default value is FFH This register value cannot be written to 00h. If 00h is written, the value of WDT_IN[7:0] will be hard-coded. Writing values other than 00h will not be affected.

3.2.2 WDT Timer Function

The clock source of the WDT timer can only be the internal 32KHz WDT clock. When you want to enable the WDT timer, you must first set the MCK register to Clear the CST_WDT bit to enable the internal 32K WDT clock. Even in Sleep mode, the WDT timer can still work normally.

The steps are as follows:

1. Set the WDTS[3:0] bits in the WDTCON register to select the WDT clock frequency.
2. Set WDTIN and select different overflow time values
3. Enable 32K WDT clock: Clear the CST_WDT bit in the MCK register to 0 and turn on the WDT crystal oscillator.
4. Enable WDT timer: Set the WDTEN bit in the WDTCON register to 1 to enable WDT.
5. Execute the CLRWDT instruction in the program to clear the WDT count value.

WDT overflow time calculation formula:

$$\text{Overflow time} = \frac{2(8^{\text{WDTS } [2:0]})}{32 k} * 2^{[7:\text{WDTIN}]} \text{ ms}$$

The range of WDTS[2:0] is 0~7, and the range of WDTIN[7:0] is 0~255.

Table 3-6

WDTS[2:0]	Counter clock	Time (when WDTIN==FFH)
000	WDTA [0]	2048ms
001	WDTA [1]	1024ms
010	WDTA [2]	512ms
011	WDTA [3]	256ms
100	WDTA [4]	128ms
101	WDTA [5]	64ms
110	WDTA [6]	32ms
111	WDTA [7]	16ms

3.3 Window Watchdog Timer (WWDT)

WWDT is mainly used to detect software errors caused by external interfaces or unpredictable logic errors.

If the sequence runs out, the WWDT can generate a reset request to reset the MCU.

WWDT is a down counter, counting down from 7Fh. When the count value jumps from 40h to 3Fh, WWDT will generate an MCU reset. If the program refreshes the counter value before the count value decreases below 40h (i.e. TR[6] becomes 0), WWDT will not generate a reset. If the 7-bit down count value of WWDT is refreshed before reaching the window register WWDTWR value WD[6:0], WWDT will also generate a reset.

3.3.1 WWDT Characteristics

ÿ Programmable down counter ÿ

Conditional reset -

When the down counter value is less than 40h, a reset is generated - When
the down counter value refreshes the TR value above the window value, a reset is generated

3.3.2 WWDT Function Description

When WWDT is enabled (WWDTEN is set), the 7-bit down counter value (TR[6:0]) changes from 40h to 3Fh (TR[6] is cleared), it will generate a reset signal to reset the chip. When software refreshes the counter value when the counter value is greater than the window value (WD[6:0]), WWDT will also generate a reset.

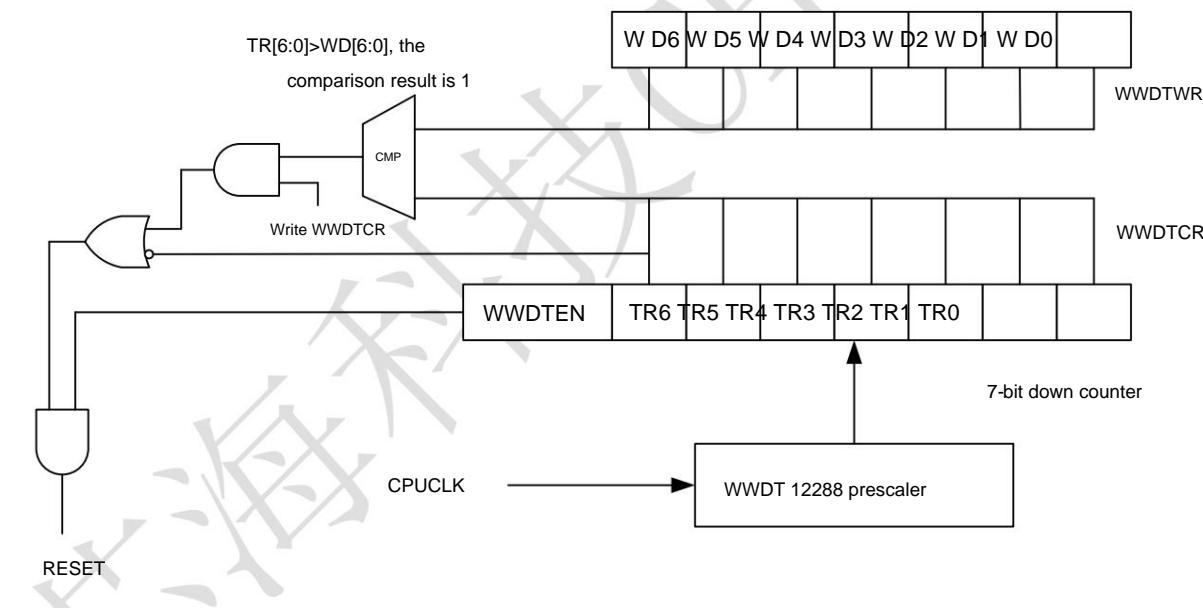


Figure 3-2 WWDT block diagram

The application must update the count value of the WWDTCR register at regular intervals to prevent the MCU from being reset. The update operation can only be performed when the counter value is lower than the window value. The value written to WWDTCR must be between FFh and C0h, that is, the value written to TR[6:0] must be between 7Fh and 40h.

3.3.2.1 WWDT Enable

After the chip is reset, the WWDT is disabled by default. To enable the WWDT, set the WWDTEN bit of the WWDTCR register to 1.

There is no other way to turn off WWDT.

When WWDT is not enabled, the WWDT counter will still count, but no reset will be generated even if the count value jumps from 40h to 3Fh.

Bit.

Before enabling WWDT, the WWDT count value must be updated to a value greater than 40h. Otherwise, when WWDT is enabled, the Bit.

3.3.2.2 WWDT Timing

The WWDT timing timeout calculation formula is as follows:

$$T_{WWDT} = f_{CPU} * 12288 * TR[6:0] - 40H + 1$$

The unit of fCPU clock cycle is ms.

The WWDT counting timing diagram is as follows

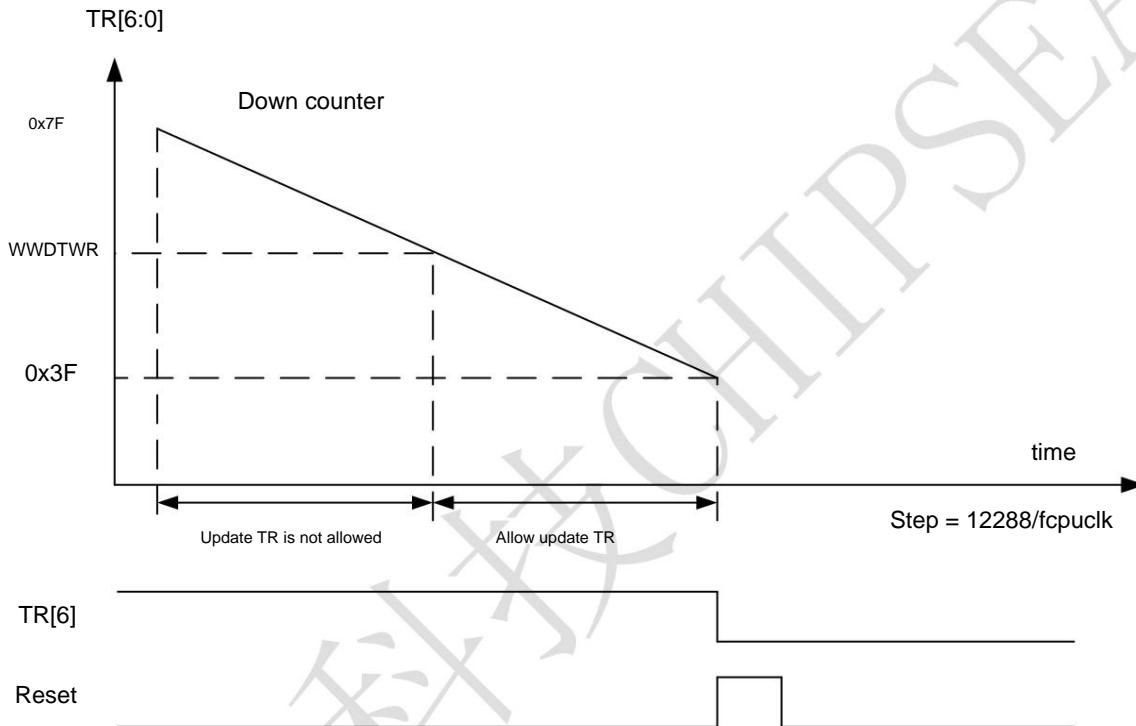


Figure 3-3 WWDT timing diagram

The theoretical time corresponding to counting from the current TR value to 3Fh under different instruction cycles.

Table 3-7

TR[6:0]	fCPU(MHz)		
	4	2	1
40h	3.072ms	6.144ms	12.288ms
7Fh	196.608ms	393.216ms	786.432ms

3.3.2.3 WWDT Configuration Description

When configuring WWDT for the first time, you need to configure WWDTCR and WWDTWR first. There is no requirement for the configuration order of these two registers. But the TR[6:0] value of WWDTCR register must be greater than 40H. Then configure WWDTEN to 1, and WWDT starts to work normally.

When WWDT is enabled, when TR[6:0]>WD[6:0], the value of TR[6:0] cannot be updated.

When TR[6:0]<WD[6:0], if you need to update the values of TR and WD, you need to update the value of TR first, and then update the value of WD.

Otherwise it may be reset directly.

3.3.2.4 Software reset function

WWDT can be used as a software reset function. When the WWDT count value TR[6:0] is greater than the window value WD[6:0] (the WWDTWR register When the WWDTCR register is set to zero, writing to the WWDTCR register will directly generate an MCU reset signal to reset the chip.

3.3.2.5 WWDT Behavior in Halt Mode and SLEEP Mode

In SLEEP mode, the WWDT will automatically stop counting and the WWDT will not generate power.
The behavior of the WWDT in HALT mode can be configured by code options to continue counting in HALT mode or
Or no counting is performed in HALT mode.

3.3.3 Register Description

Table 3-8 WWDT register list

land y	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-on reset value
47h	WWDTCR	WWDTEN								01111111
48h	WWDTWR									u1111111

3.3.3.1 WWDTCR register (address 47h)

Table 3-9

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Characteristics	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
WWDTCR	WWDTEN	TR[6:0]							

Table 3-10

Bit address identifier		Function
7	WWDTEN	<p>WWDT module enable bit</p> <p>This bit is set to 1 by software and cleared to 0 by hardware only at reset.</p> <p>Reset.</p> <p>0: WWDT off</p> <p>1: WWDT enabled</p>
6:0	TR[6:0]	<p>7-bit count value, default value is 7Fh</p> <p>This register is the count value of the WWDT counter. It decreases by 1 every 12288 CPU clock cycles.</p> <p>When the count value jumps from 40H to 3Fh, a reset signal will be generated. Software can write WWDTCR Register to update the value of TR[6:0] to avoid MCU reset.</p>

3.3.3.2 WWDTWR Register (Address 48h)

Table 3-11

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Characteristics	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
WWDTWR		WD[6:0]							

Table 3-12

Bit address identifier		Functionality
7	Reserved	Retention
6:0	WD[6:0]	7-bit window value, default value is 7Fh The register value is a 7-bit window value used to compare with the counter count value.

3.4 Timer/Counter 2

3.4.1 Timer/Counter 2 Overview

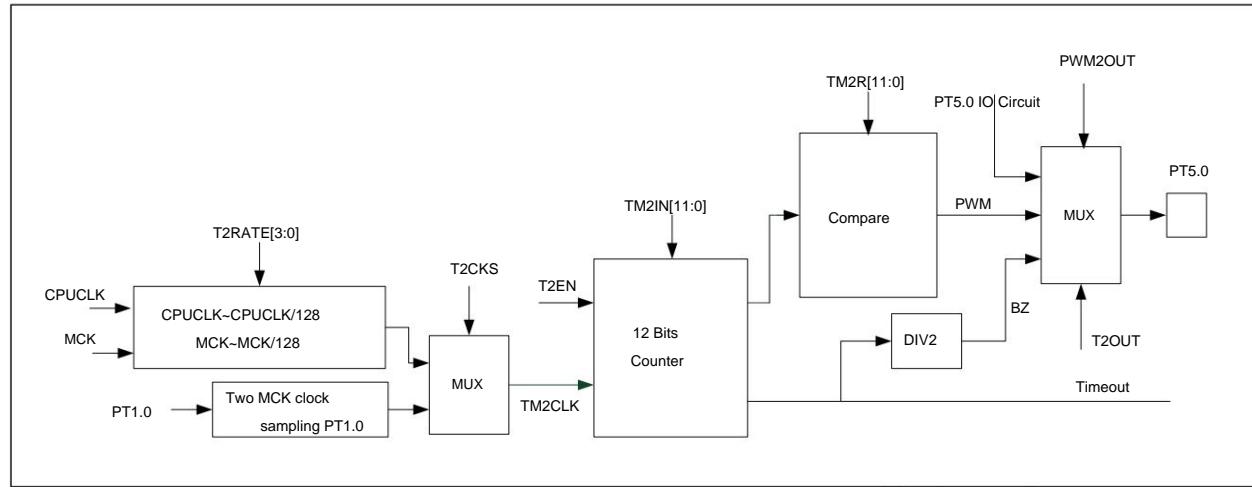


Figure 3-4 Functional block diagram of the timer/counter 2 module

The input clock of the Timer/Event Counter 2 module is TM2CLK. When the user sets the enable bit of the Timer/Event Counter 2 module, the 12-bit count The timer will start and increment from 00h to TM2IN. The user needs to set TM2IN (timer module count overflow value) to select the timeout time. After the timeout, an interrupt signal will be generated.

When a timer timeout occurs, the Timer 2 interrupt flag TM2IF is set to 1 by hardware. This bit can only be cleared by software. If the Timer 2 interrupt (TM2IE=1) and the interrupt general enable (GIE) are enabled, the program counter will jump to 004H to execute the interrupt service routine.

Key features:

- 1) 12-bit programmable timer;
- 2) External event counting;
- 3) Buzzer output;
- 4) PWM2 output;

3.4.2 Register Description

Table 3-13 Timer register list

addr site	Name	Bit7	Bit6	Bit5			Bit4	Bit3			Bit2		Bit1		Bit0	Power on Place value
06h	INTF				TM2IF				TM0IF SRADIF				E1IF		E0IF 00000000	
07h	NOT			GO	TM2IE				TM0IE SRADIE				E1IE		E0IE 00000000	
17h	TM2CON	T2EN			T2RATE[2:0]			T2CKS	T2RSTB			T2OUT		PWM2OUT	00000100	
18h	TM2IN								TM2IN[7:0]						11111111	
19h	TM2CNT								TM2CNT[7:0]						00000000	
1Ah	TM2R								TM2R[7:0]						00000000	
24h	TM2INH									TM2IN[11:8]					uuuu0000	
25h	TM2CNTH									TM2CNT[11:8]					uuuu0000	
26h	TM2RH									TM2R[11:8]					uuuu0000	
2Eh	METCH1 P3HINV P3LINV						PT1W[6:4]			PWM2PO PWM2PO1					00000000u	
2Fh	METCH	VTHSEL			REF_SEL[2:0]			PWMIS	T3RATE[3] T2RATE[3]	P14_CUR	00000000					

3.4.2.1 TM2CON register (address 17h)

Table 3-14

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
TM2CON	T2EN		T2RATE[2:0]		T2CKS	T2RSTB	T2OUT PWM2OUT	

Table 3-15

Bit address identifier																																					
7	T2EN	Function Timer/Event Counter 2 Enable Bit 1: Enable timer 2 0: Disable timer 2																																			
6:4	T2RATE[2:0]	The timer/counter 2 clock is divided and combined with T2RATE[3] in the METCH register to form 4 Bit clock divider and select register. <table border="1"> <tr><td>T2RATE [3:0]</td><td>TM2CLK</td></tr> <tr><td>0000</td><td>CPUCLK</td></tr> <tr><td>0001</td><td>CPUCLK /2</td></tr> <tr><td>0010</td><td>CPUCLK /4</td></tr> <tr><td>0011</td><td>CPUCLK /8</td></tr> <tr><td>0100</td><td>CPUCLK /16</td></tr> <tr><td>0101</td><td>CPUCLK /32</td></tr> <tr><td>0110</td><td>CPUCLK /64</td></tr> <tr><td>0111</td><td>CPUCLK /128</td></tr> <tr><td>1000</td><td>MCK</td></tr> <tr><td>1001</td><td>MCK /2</td></tr> <tr><td>1010</td><td>MCK /4</td></tr> <tr><td>1011</td><td>MCK /8</td></tr> <tr><td>1100</td><td>MCK /16</td></tr> <tr><td>1101</td><td>MCK /32</td></tr> <tr><td>1110</td><td>MCK /64</td></tr> <tr><td>1111</td><td>MCK /128</td></tr> </table>		T2RATE [3:0]	TM2CLK	0000	CPUCLK	0001	CPUCLK /2	0010	CPUCLK /4	0011	CPUCLK /8	0100	CPUCLK /16	0101	CPUCLK /32	0110	CPUCLK /64	0111	CPUCLK /128	1000	MCK	1001	MCK /2	1010	MCK /4	1011	MCK /8	1100	MCK /16	1101	MCK /32	1110	MCK /64	1111	MCK /128
T2RATE [3:0]	TM2CLK																																				
0000	CPUCLK																																				
0001	CPUCLK /2																																				
0010	CPUCLK /4																																				
0011	CPUCLK /8																																				
0100	CPUCLK /16																																				
0101	CPUCLK /32																																				
0110	CPUCLK /64																																				
0111	CPUCLK /128																																				
1000	MCK																																				
1001	MCK /2																																				
1010	MCK /4																																				
1011	MCK /8																																				
1100	MCK /16																																				
1101	MCK /32																																				
1110	MCK /64																																				
1111	MCK /128																																				
3	T2CKS	Timer/Event Counter 2 Clock Source Select Bit 1: PT1.0 as clock 0: CPUCLK or MCK divided clock																																			
2	T2RSTB	Timer/Event Counter 2 Reset 1: Disable timer/counter 2 reset 0: Enable timer/counter 2 reset When this bit is set to 0, Timer 2 reset is completed after one instruction cycle, and T2RSTB hardware Set to 1.																																			
1	T2OUT	PWM and buzzer output control, output IO is selected by PWM2PO, PWM2PO1. <table border="1"> <tr><td>T2OUT</td><td>PWM2OUT</td><td>PWM and buzzer output control, only when The IO port should be configured as output valid</td></tr> <tr><td>0</td><td>0</td><td>Ordinary IO port</td></tr> <tr><td>0</td><td>1</td><td>PWM2 Output</td></tr> <tr><td>1</td><td>0</td><td>Buzzer output</td></tr> <tr><td>1</td><td>1</td><td>PWM2 Output</td></tr> </table>		T2OUT	PWM2OUT	PWM and buzzer output control, only when The IO port should be configured as output valid	0	0	Ordinary IO port	0	1	PWM2 Output	1	0	Buzzer output	1	1	PWM2 Output																			
T2OUT	PWM2OUT	PWM and buzzer output control, only when The IO port should be configured as output valid																																			
0	0	Ordinary IO port																																			
0	1	PWM2 Output																																			
1	0	Buzzer output																																			
1	1	PWM2 Output																																			
0	PWM2OUT	PT5.0 can be used as a buzzer and PWM output port, while the other PT1.5, PT1.4 and PT3.1 can only be used as It can be used as a PWM output port. So when the above registers are configured as buzzer output, and PWM2PO,																																			

		If the IO port selected by PWM2PO1 is not PT5.0 port, the above 4 ports will have no output.
--	--	--

3.4.2.2 TM2IN register (address 18h)

Table 3-16

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TM2IN	TM2IN[7:0]							

Table 3-17

Bit address identifier	
7:0 TM2IN[7:0]	Function Timer/Counter overflow value lower 8 bits

3.4.2.3 TM2INH register (address 24h)

Table 3-18

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TM2INH	TM2INH[11:8]							

Table 3-19

Bit address identifier		Function
3:0 TM2INH[11:8]	Timer/Event Counter	overflow value high 4 bits

3.4.2.4 TM2CNT register (address 19h)

Table 3-20

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TM2CNT	TM2CNT[7:0]							

Table 3-21

Bit address identifier function	
7:0 TM2CNT[7:0]	Timer/Counter 2 count register lower 8 bits, read only

3.4.2.5 TM2CNTH register (address 25h)

Table 3-22

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
TM2CNTH	TM2CNTH[11:8]							

Table 3-23

Bit address identifier function								
3:0	TM2CNTH[11:8]	Timer/Counter 2 count register high 4 bits, read only						

3.4.2.6 TM2R register (address 1Ah)

Table 3-24

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TM2R	TM2R[7:0]							

Table 3-25

Bit address identifier								
7 ѿ TM2R[7:0]								

Function Timer/Event Counter 2 PWM high level duty cycle control register lower 8 bits.
Note: When TM2STP=1 in the CMPCON2 register, the comparator output will flip and
When the comparator interrupt flag is set, the TM2R register value will be configured by hardware as
8'hFFÿ

3.4.2.7 TM2RH register (address 26h)

Table 3-26

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TM2RH	TM2R[11:8]							

Table 3-27

Bit address identifier								
3:0 TM2RH[11:8]								

Function Timer/Event Counter 2 PWM high level duty cycle control register upper 4 bits.
Note: When TM2STP=1 in the CMPCON2 register is configured, a toggle occurs at the comparator output.
When the comparator interrupt flag is set to 1, the TM2RH register value will be configured by hardware as
4'hFÿ

3.4.2.8 METCH Register (Address 2Fh)

Table 3-28

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
METCH	VTHSEL	REF_SEL[2:0]				PWMIS T3RATE[3] T2RATE[3] P14_CUR		

Table 3-29

Bit address identifier		Function
------------------------	--	----------

1	T2RATE[3]	<p>Timer 2 clock source selection 0: CPUCLK 1: MCK</p> <p>The clock selected can be pre-divided. For specific pre-divided multiples, refer to TM2CON register. T2RATE description of the register.</p>
---	-----------	--

3.4.2.9 METCH1 Register (Address 2Eh)

Table 3-30

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
METCH1	P3HINV P3LINV			PT1W[6:4]		PWM2PO	PWM2PO1	

Table 3-31

Bit address identifier		Function		
2	PWM2PO	PWM2 output pin selection		
1	PWM2PO1	PWM2PO	PWM2PO1	
		0	0	PT5.0 as PWM2 output port
		0	1	PT1.5 as PWM2 output port
		1	0	PT3.1 as PWM2 output port
		1	1	PT1.4 as PWM2 output port

3.4.3 Timer/Counter Function

The clock source of Timer 2 can be selected from CPUCLK and MCK. In HALT mode, Timer 2 can still continue counting, so it can In SLEEP mode, the internal high-speed oscillator stops working and Timer 2 stops counting, so it cannot wake up the SLEEP mode.

Mode.

operate:

- 1) Configure T2RATE[3] of METCH to select the clock source for the timer module.
- 2) Configure T2RATE[2:0] of the TM2CON register to select the clock division for Timer 2.
- 3) Set TM2IN[11:0] to select the timer overflow value
- 4) Set register bits TM2IE and GIE to enable timer interrupt.
- 5) Clear register bit T2RSTB to reset the counter of the timer module.
- 6) Set register bit T2EN to enable the 12-bit counter of the timer module.
- 7) When the timing timeout occurs, the BZ output signal jumps and can be used as a buzzer output; the program counter will jump to 004H.

Timer 2 overflow time calculation method:

$$\text{Timer 2 overflow time} = (\text{TM2IN}[11:0]+1)/\text{TM2CLK}. (\text{TM2IN} \text{ is not } 0)$$

3.4.4 Buzzer

The buzzer output of Timer 2 is low by default. When a count overflow event occurs in Timer 2, the buzzer output flips.

The buzzer output is a square wave with a fixed duty cycle of 50% and a period twice the overflow time of Timer 2.

Configure the buzzer output operation:

- 1) Configure PT5.0 as output port.
- 2) Configure the lower 2 bits of the TM2CON register, T2OUT is set to 1, PWM2OUT is set to 0

- 3) Configure T2RATE[3] of METCH to select the clock source for the timer module.
- 4) Configure T2RATE[2:0] of the TM2CON register to select the clock division for Timer 2.
- 5) Set TM2IN and select the timer overflow value.
- 6) Clear register bit T2RSTB to reset the counter of the timer module.
- 7) Set register bit T2EN to enable the 12-bit counter of the timer module.
- 8) When the timing timeout occurs, the BZ output signal jumps and can be used as a buzzer output.

Buzzer cycle calculation method:

$$\text{Buzzer period} = (\text{TM2IN}[11:0]+1)*2/\text{TM2CLK. } (\text{TM2IN is not } 0)$$

3.4.5 PWM

PWM Output Priority

The PWM output priority of Timer 2 decreases from top to bottom.

Table 3-32

condition						PWM Priority
PT5EN[0]	PT3EN[1]	P3L_OEN	T2OUT	PWM2OUT	PWM2IN	
0	0	X	X	X	X	PT5.0, PT3.1 as input port
1	0	1	X	X	X	PT5.0 as timer 3 complementary PWM output Port, PT3.1 as input port
1	x	0	X	1	0	PT5.0 is used as the PWM output port of timer 2. PT3.1 is used as a normal IO port
1	x	0	1	1	1	PT5.0 is used as buzzer output of timer 2 Port, PT3.1 is used as a common IO port
1	1	0	1	1	1	PT5.0 is used as buzzer output of timer 2 Port, PT3.1 is used as PWM output of timer 2 mouth
x	1	0	0	1	1	PT5.0 is used as a common IO port, PT3.1 is used as a fixed IO port. PWM output port of timer 2
1	1	0	1	0	X	PT5.0 is used as buzzer output of timer 2 Port, PT3.1 as common output port
x	1	0	0	0	X	PT5.0 is used as a common IO port, PT3.1 is used as a common Output port

Steps to configure PWM output:

- 1) Configure PT5.0 as output port.
- 2) Configure the lower 2 bits of the TM2CON register, T2OUT is set to 0, PWM2OUT is set to 1
- 3) Configure T2RATE[3] of METCH to select the clock source for the timer module.
- 4) Configure T2RATE[2:0] of the TM2CON register to select the clock division for Timer 2.
- 5) Set TM2IN[11:0] to configure the period of PWM2.
- 6) Set TM2R[11:0] to configure the high level pulse width of PWM2.
- 7) Enable PWM2OUT output, configure PT5.0 as output port, and then set T2EN to 1 to start the timer.
- 8) PWM is output from PT5.0.

The period is TM2IN+1, and the high level pulse width is TM2R. If TM2IN=0x0F, TM2R=0x03, the PWM2 waveform output is as follows:

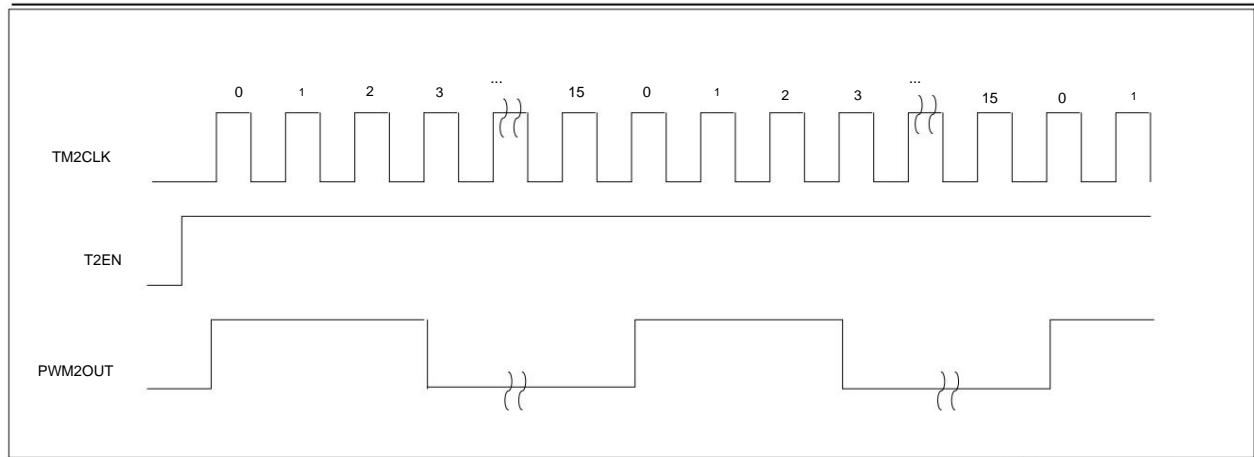


Figure 3-5

3.5 Timer/Counter 3

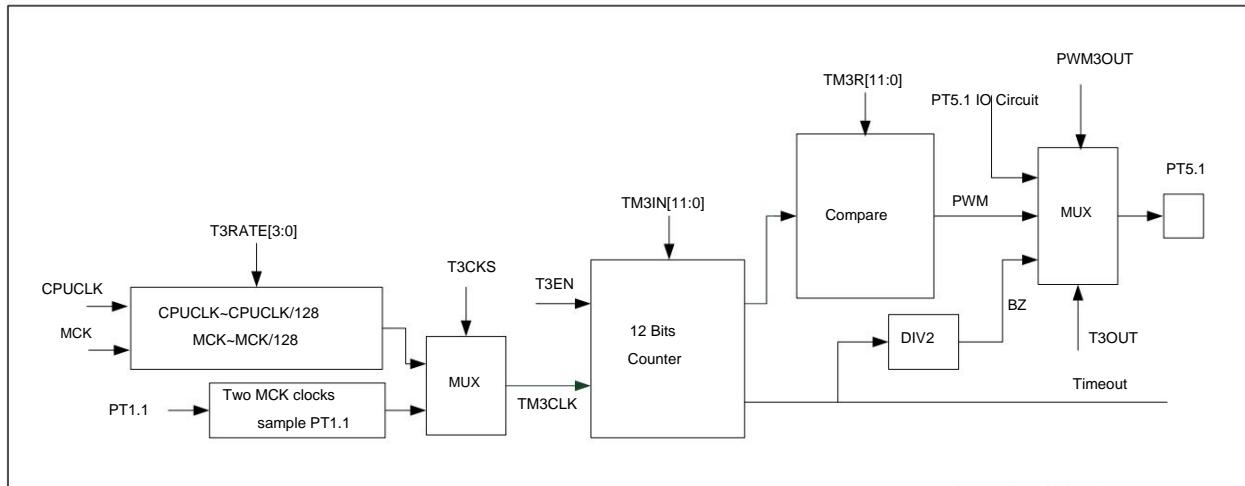


Figure 3-6 Functional block diagram of the timer/counter 3 module

The input clock of the Timer/Event Counter 3 module is TM3CLK. When the user sets the enable bit of the Timer/Event Counter 3 module, the 12-bit count The timer will start and increment from 00h to TM3IN. The user needs to set TM3IN (timer module count overflow value) to select the timeout time. After the timeout, an interrupt signal will be generated.

When a timer timeout occurs, the Timer 3 interrupt flag TM3IF is set to 1 by hardware. This bit can only be cleared by software. If the Timer 3 interrupt (TM3IE=1) and the interrupt general enable (GIE) are enabled, the program counter will jump to 004H to execute the interrupt service routine.

Key features:

- 1) 12-bit programmable timer;
- 2) External event counting;
- 3) Buzzer output;
- 4) PWM output;

3.5.1 Register Description

Table 3-33 Timer register list

land site	Name	Bit7	Bit6	Bit5	Bit4	Bit3			Bit2	Bit1	Bit0	Power on Place value			
3Ch	INTF2	CMPIF					TM3IF					0uu0uuuu			
3Dh	INTE2	CMPIE					TM3IE					0uu0uuuu			
1Bh	M3CON	T3EN	T3RATE[2:0]			T3CKS	T3RSTB		T3OUT	PWM3OUT	00000	100			
1Ch	TM3IN	TM3IN[7:0]										11111111			
1Dh	TM3CNT	TM3CNT[7:0]										00000000			
1Eh	TM3R	TM3R[7:0]										00000000			
1Fh	TM3INH						TM3IN[11:8]					uuuu0000			
27h	TM3CNTH						TM3CNT[11:8]					uuuu0000			
2Ch	TM3RH						TM3R[11:8]					uuuu0000			
2Fh	METCH	VTHSEL	REF_SEL[2:0]			PWMIS	T3RATE[3]	T2RATE[3]	E[3]	P14_CUR	00000000				
2Dh	M3CON2	DT3CK[1:0]		DT3CNT[2:0]			DT3_EN	P3H_OEN	P3L_OEN	00000000					
2Eh	METCH1	P3HINV	P3LINV	PT1W[6:4]			PWM2PO	PWM2PO1			0000000u				
45h	M3CON3	PWM3PO				P3H2INV	P3L2INV	P3H2OEN	P3L2OEN	0uu0000					

3.5.1.1 TM3CON register (address 1Bh)

Table 3-34

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
TM3CON	T3EN	T3RATE[2:0]			T3CKS	T3RSTB	T3OUT PWM	T3OUT

Table 3-35

Bit address identifier																																					
7	T3EN	Function Timer/Event Counter 3 Enable Bit 1: Enable timer 3 0: Disable timer 3																																			
6:4	T3RATE[2:0]	Timer/Counter 3 clock division selection, combined with T3RATE[3] in the METCH register to form 4 Bit clock select register. <table border="1"> <tr><td>T3RATE [3:0]</td><td>TM3CLK</td></tr> <tr><td>0000</td><td>CPUCLK</td></tr> <tr><td>0001</td><td>CPUCLK /2</td></tr> <tr><td>0010</td><td>CPUCLK /4</td></tr> <tr><td>0011</td><td>CPUCLK /8</td></tr> <tr><td>0100</td><td>CPUCLK /16</td></tr> <tr><td>0101</td><td>CPUCLK /32</td></tr> <tr><td>0110</td><td>CPUCLK /64</td></tr> <tr><td>0111</td><td>CPUCLK /128</td></tr> <tr><td>1000</td><td>MCK</td></tr> <tr><td>1001</td><td>MCK /2</td></tr> <tr><td>1010</td><td>MCK /4</td></tr> <tr><td>1011</td><td>MCK /8</td></tr> <tr><td>1100</td><td>MCK /16</td></tr> <tr><td>1101</td><td>MCK /32</td></tr> <tr><td>1110</td><td>MCK /64</td></tr> <tr><td>1111</td><td>MCK /128</td></tr> </table>		T3RATE [3:0]	TM3CLK	0000	CPUCLK	0001	CPUCLK /2	0010	CPUCLK /4	0011	CPUCLK /8	0100	CPUCLK /16	0101	CPUCLK /32	0110	CPUCLK /64	0111	CPUCLK /128	1000	MCK	1001	MCK /2	1010	MCK /4	1011	MCK /8	1100	MCK /16	1101	MCK /32	1110	MCK /64	1111	MCK /128
T3RATE [3:0]	TM3CLK																																				
0000	CPUCLK																																				
0001	CPUCLK /2																																				
0010	CPUCLK /4																																				
0011	CPUCLK /8																																				
0100	CPUCLK /16																																				
0101	CPUCLK /32																																				
0110	CPUCLK /64																																				
0111	CPUCLK /128																																				
1000	MCK																																				
1001	MCK /2																																				
1010	MCK /4																																				
1011	MCK /8																																				
1100	MCK /16																																				
1101	MCK /32																																				
1110	MCK /64																																				
1111	MCK /128																																				
		Note: T3RATE[3] is in bit 2 of the METCH register.																																			
3	T3CKS	Timer/Event Counter 3 Clock Source Select Bit 1: PT1.1 as clock 0: CPUCLK or MCK divided clock																																			
2	T3RSTB	Timer/Event Counter 3 Reset 1: Disable timer/counter 3 reset 0: Enable timer/counter 3 reset When this bit is set to 0, Timer 3 reset is completed after one instruction cycle, and T3RSTB is set to 1ÿ																																			
1	T3OUT	PWM and buzzer output control, when only the output of PWM3H/PWM3L or PWM3H2/PWM3L2 is needed When PWM3 output is not needed, the following two bits need to be configured as 00.																																			
0	PWM3OUT	<table border="1"> <tr><td>T3OUT</td><td>PWM3OUT</td><td>PWM and buzzer output control, only when the corresponding IO port is configured Output valid</td></tr> <tr><td>0</td><td>0</td><td>Ordinary IO port</td></tr> <tr><td>0</td><td>1</td><td>PWM3 Output</td></tr> <tr><td>1</td><td>0</td><td>Buzzer output</td></tr> </table>		T3OUT	PWM3OUT	PWM and buzzer output control, only when the corresponding IO port is configured Output valid	0	0	Ordinary IO port	0	1	PWM3 Output	1	0	Buzzer output																						
T3OUT	PWM3OUT	PWM and buzzer output control, only when the corresponding IO port is configured Output valid																																			
0	0	Ordinary IO port																																			
0	1	PWM3 Output																																			
1	0	Buzzer output																																			

		1	1	PWM3 Output	
--	--	---	---	-------------	--

3.5.1.2 TM3IN register (address 1Ch)

Table 3-36

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TM3IN	TM3IN[7:0]							

Table 3-37

Bit address identifier		
7:0 TM3IN[7:0]		Function Timer/Counter overflow value lower 8 bits

3.5.1.3 TM3INH register (address 1Fh)

Table 3-38

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TM3INH	TM3INH[11:8]							

Table 3-39

Bit address identifier		Function
3:0 TM3INH[11:8]		Timer/Event Counter overflow value high 4 bits

3.5.1.4 TM3CNT register (address 1Dh)

Table 3-40

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TM3CNT	TM3CNT[7:0]							

Table 3-41

Bit address identifier function		
7:0 TM3CNT[7:0]		Timer/Counter 3 count register low 8 bits, read only

3.5.1.5 TM3CNTH register (address 27h)

Table 3-42

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
TM3CNTH	TM3CNTH[11:8]							

Table 3-43

Bit address identifier	function	
3:0 TM3CNTH[11:8]	Timer/Counter 3 count register high 4 bits, read only	

3.5.1.6 TM3R register (address 1Eh)

Table 3-44

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TM3R	TM3R[7:0]							

Table 3-45

Bit address identifier		
7:0 TM3R[7:0]		Function Timer/Counter 3 PWM high level duty cycle control register lower 8 bits Note: When TM3STP=1 in the CMPCON2 register, the comparator output will flip and When the comparator interrupt flag is set to 1, the TM3R register value will be configured by hardware as 8'hFFÿ

3.5.1.7 TM3RH register (address 2Ch)

Table 3-46

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TM3RH	TM3R[11:8]							

Table 3-47

Bit address identifier		
3:0 TM3RH[11:8]		Function Timer/Counter 3 PWM high level duty cycle control register upper 4 bits Note: When TM3STP=1 in the CMPCON2 register is configured, a toggle occurs at the comparator output. When the comparator interrupt flag is set to 1, the TM3RH register value will be configured by hardware as 4'hFÿ

3.5.1.8 METCH Register (Address 2Fh)

Table 3-48

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
METCH	VTHSEL	REF_SEL[2:0]			PWMIS T3RATE[3]	T2RATE[3]	P14_CUR	

Table 3-49

Bit address identifier		
2	T3RATE[3]	Function Timer 3 Clock Selection 0: CPUCLK 1: MCK The clock selected can be pre-divided. For specific pre-divided multiples, refer to TM3CON register.

		T3RATE description of the register.
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3.5.1.9 TM3CON2 register (address 2Dh)

Table 3-50

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TM3CON2	DT3CK[1:0]		DT3CNT[2:0]			DT3_EN	P3H_OEN	P3L_OEN

Table 3-51

Bit address identifier		Function
7:6	DT3CK[1:0]	Timer 3 Dead Time Clock Selection
		DT3CK[1:0] DT3_CLK
		00 MCK
		01 MCK/2
		10 MCK/4
		11 MCK/8
5:3	DT3CNT[2:0]	Dead time selection Dead time = DT3CNT[2:0]*DT3_CLK
2	DT3_EN	Dead zone generator 3 enable bit 0: Disable dead zone generator 3 1: Enable dead zone generator 3
1	P3H_OEN	Complementary PWM3H output enabled from PT5.1 0: PWM3H does not output 1: PWM3H output from PT5.1
0	P3L_OEN	Complementary PWM3L output enabled from PT5.0 0: PWM3L does not output 1: PWM3L output from PT5.0

3.5.1.10 METCH1 Register (Address 2Eh)

Table 3-52

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristic	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
METCH1	P3HINV	P3LINV	PT1W[6:4]			PWM2PO	PWM2PO1	

Table 3-53

Bit address identifier		Function
7	P3HINV	Complementary PWM3H Output inversion control bit from PT5.1 0: PWM3H does not invert output 1: PWM3H inverted output
6	P3LINV	Complementary PWM3L outputs the inverted control bit from PT5.0 0: PWM3L does not invert the output 1: PWM3L inverted output

3.5.1.11 TM3CON3 register (address 45h)

Table 3-54

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TM3CON3	PWM3PO				P3H2INV P3L2INV		P3H2OEN	P3L2OEN

Table 3-55

Bit address identifier		Function
7	PWM3PO	PWM3 output pin selection 0: PT5.1 as PWM3 output port 1: PT3.5 as PWM3 output port
6:4	RESERVE	reserve
3	P3H2INV	Complementary PWM3H2 outputs the inverted control bit from PT1.0 0: PWM3H2 does not invert the output 1: PWM3H2 inverted output
2	P3L2INV	Complementary PWM3L2 outputs the inverted control bit from PT3.5 0: PWM3L does not invert the output 1: PWM3L inverted output
1	P3H2OEN	Complementary PWM3H2 output enable from PT1.0 output 0: PWM3H2 does not output from PT1.0 1: PWM3H2 outputs from PT1.0
0	P3L2OEN	Complementary PWM3L2 output enable from PT3.5 output 0: PWM3L2 does not output from PT3.5 1: PWM3L2 output from PT3.5

3.5.2 Timer/Counter Function

The clock source of Timer 3 can be selected from CPUCLK and MCK. In HALT mode, Timer 3 can still continue counting, so it can work in SLEEP mode, the internal high-speed oscillator stops working and Timer 3 stops counting, so it is impossible to wake up the SLEEP mode.

Mode.

Timer/Counter Operation:

- 1) Configure T3RATE[3] of METCH to select the clock source for the timer module.
- 2) Configure T3RATE[2:0] of TM3CON register to select clock division for Timer 3.
- 3) Set TM3IN[11:0] to select the timer overflow value.
- 4) Set register bits TM3IE and GIE to enable timer interrupt.
- 5) Clear register bit T3RSTB to reset the counter of the timer module.
- 6) Set register bit T3EN to enable the 12-bit counter of the timer module.
- 7) When the timing timeout occurs, the BZ output signal jumps and can be used as a buzzer output; the program counter will jump to 004H.

Timer 3 overflow time calculation method:

$$\text{Timer 3 overflow time} = (\text{TM3IN}[11:0]+1)/\text{TM3CLK}. \quad (\text{TM3IN is not } 0)$$

3.5.3 Buzzer

The buzzer output of Timer 3 is low level by default. When Timer 3 overflows, the buzzer output flips.

The buzzer output is a square wave with a fixed duty cycle of 50% and a period twice the overflow time of Timer 3.

Configure the buzzer output operation:

- 1) Configure PT5.1 as output port.

- 2) Configure the lower 2 bits of the TM3CON register, T3OUT is set to 1, PWM3OUT is set to 0
- 3) Configure T3RATE[3] of METCH to select the clock source for the timer module.
- 4) Configure T3RATE[2:0] of the TM3CON register to select the clock division for Timer 3.
- 5) Configure TM3IN and select the timer overflow value.
- 6) Clear the count value of Timer 3: Configure T3RSTB in the TM3CON register to 0 to reset the counter of Timer 3.
- 7) Enable the timer module: Set T3EN of TM3CON to 1 to enable the 12-bit counter of the timer module.
- 8) When the timing timeout occurs, the BZ output signal jumps and can be used as a buzzer output

Buzzer cycle calculation method:

$$\text{Buzzer period} = (\text{TM3IN}[11:0]+1)*2/\text{TM3CLK}. \text{ (TM3IN is not 0)}$$

3.5.4 PWM

PWM Output Priority

Timer 3 has multiple forms of PWM output, and the priority of PWM output decreases from top to bottom.

Table 3-56

condition					PWM Priority
PT5EN[1:0] P3H_OEN		P3L_OEN	T3OUT	PWM3OUT	
00	X	X	X	X	PT5.0, PT5.1 as input port
11	1	1	X	X	PT5.0 and PT5.1 are complementary PWM output ports.
11	1	0	X	X	PT5.1 outputs PWM3H, PT5.0 does not function as timer 3 PWM output port
11	0	1	X	1	PT5.1 outputs normal PWM of timer 3, PT5.0 Output PWM3L
11	0	0	X	1	PT5.1 outputs normal PWM of timer 3, PT5.0 Do not use the PWM output port of timer 3
11	0	0	1	0	PT5.1 is used as the buzzer output port of timer 3. PT5.0 is not used as the PWM output port of timer 3
11	0	0	0	0	PT5.1 is used as a normal output port, PT5.0 is not used as a timer 3 PWM output ports

Configure PWM output operation:

- 1) Configure PT5.1 as output port.
- 2) Set T3RATE[3] of METCH to select the clock input for the timer module.
- 3) Set TM3IN to configure the period of PWM3.
- 4) Set TM3R to configure the high level pulse width of PWM3.
- 5) Enable PWM3OUT output, configure PT5.1 as output port, and then set T3EN to 1 to start the timer.
- 6) PWM3 is output from PT5.1.

The cycle is TM3IN+1, and the high level pulse width is TM3R. If TM3IN=0x0F, TM3R=0x03, the PWM3 waveform output is as follows:

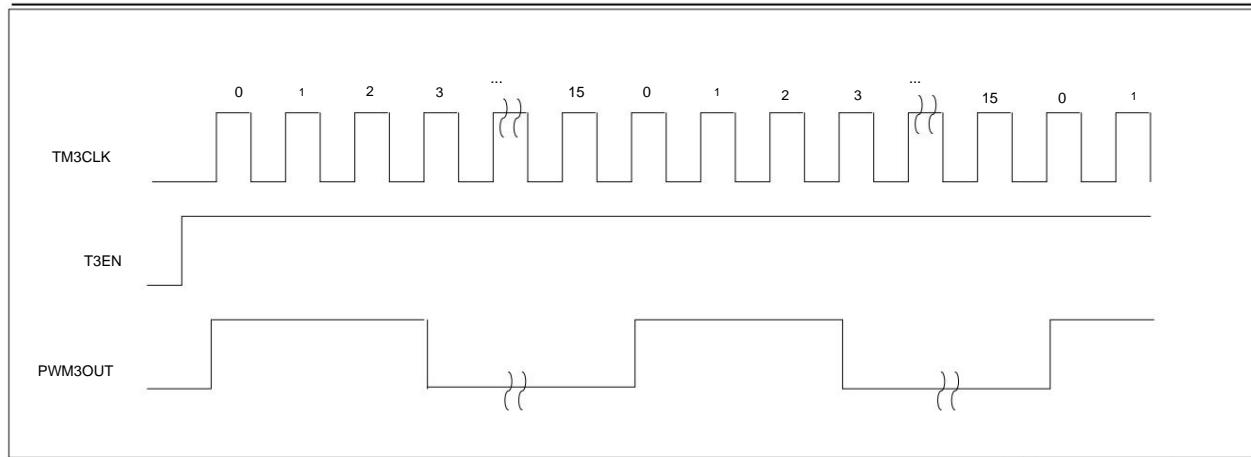


Figure 3-7

3.5.5 Complementary PWM output

CSU32M10/CSU32M11 provides a pair of complementary outputs from Timer 3 that can be used as PWM drive signals.

For NMOS drive, PWM output is low level active, while for PMOS drive, PWM output is high level active.

When used to drive PMOS and NMOS, the dead time generator inserts a dead time to prevent excessive DC current. The dead time can be

The DT3CK[1:0] and DT3CNT[2:0] bits of the TM3CON2 register are defined.

Through the dead time insertion circuit, the output signal is finally sent to the external power transistor.

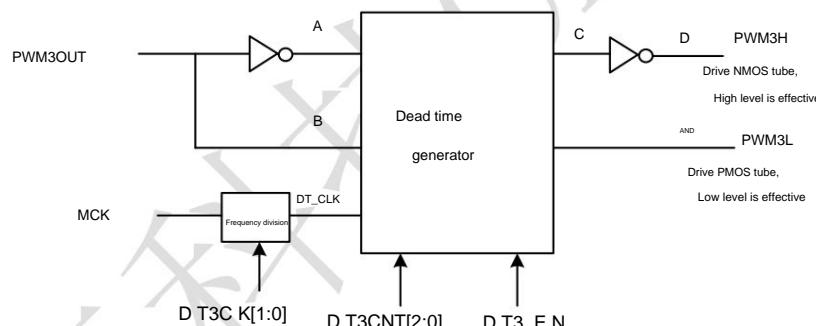


Figure 3-8 Complementary PWM output block diagram

Complementary PWM output waveform

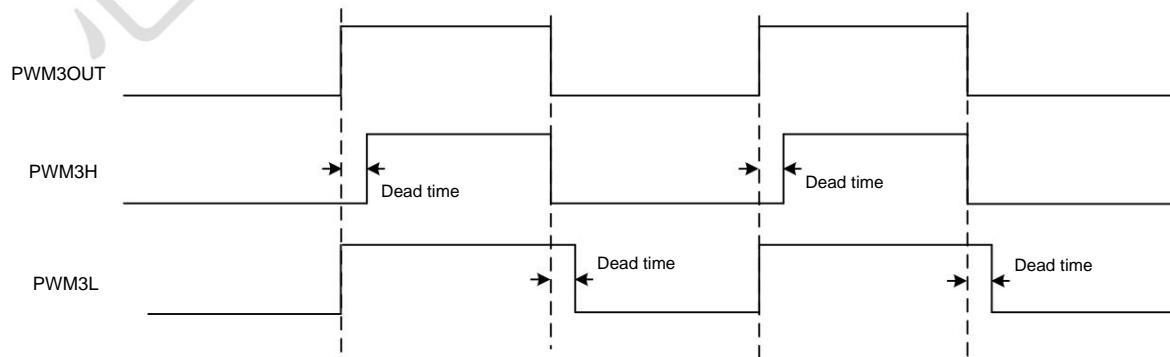


Figure 3-9

Complementary PWM output after PWM output is inverted

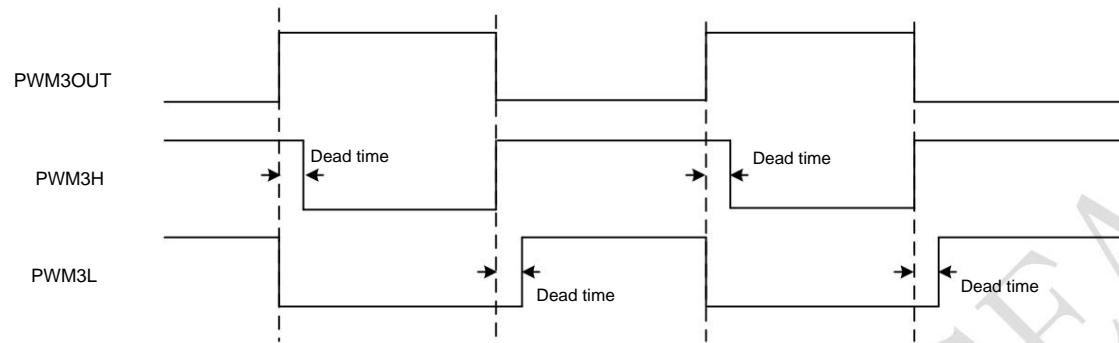


Figure 3-10

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3.6 Analog-to-Digital Converter (ADC)

The CSU32M10/CSU32M11 analog-to-digital conversion modules share 7 external channels (AIN0~AIN6) and 3 special channels (AIN7: internal 1/8VDD; AIN8: internal reference voltage; AIN9: GND), which can convert analog signals into 12-bit digital signals.

When you use the ADC, you must first select the input channel (AIN0~AIN9), then set SRADEN to 1 to enable ADC, and then set SRADS to 1 to start the AD conversion.

After the conversion is completed, the system automatically clears SRADS to 0 and stores the conversion results in registers SRADL and SRADH.

When the code option PD_OP = 1, P1.0 and P3.4 will be connected to the pull-down, and the data will be inaccurate when the AD conversion of this channel is performed.

For AD channel, you need to configure PD_OP=0.

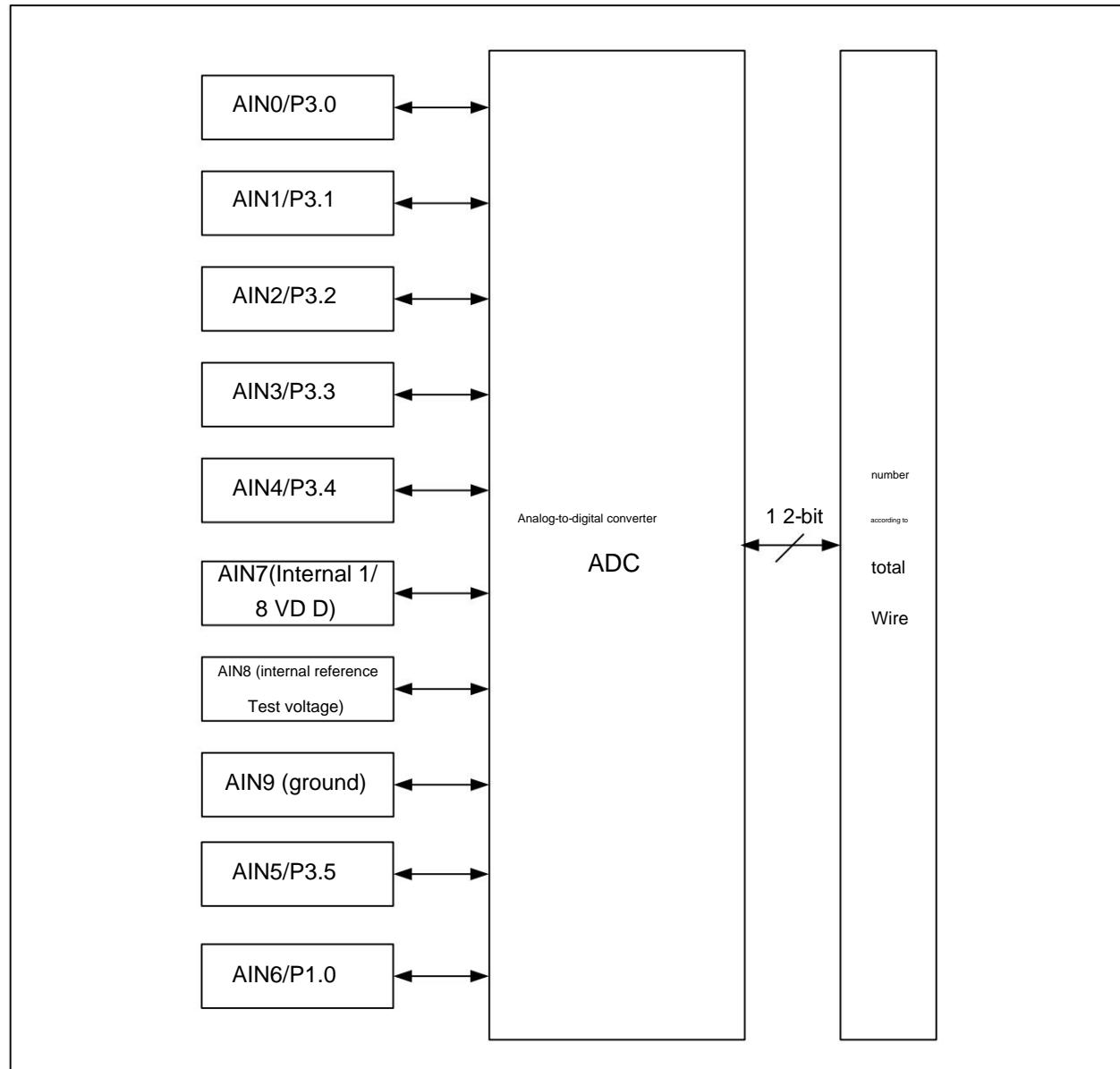


Figure 3-11 Analog-to-digital converter ADC functional block diagram

3.6.1 Register Description

Table 3-57 ADC register list

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2					Bit1	Bit0	Power-On Reset value
06h	INTF				TM2IF			TM0IF	SRADIF			E1IF	E0IF	00u00u0000
07h	NOT		GO	TM2IE		TM0IE	SRADIE				E1IE	E0IE	00u00u0000	

34h	SRADCON0	35h			SRADACKS[1:0]			SRADCKS[1:0]	uu00uu00
SRADCON1	36h	SRADEN	SRADS	OFTEN	CALIF	ENOV		VREFS[1:0]	00000u00
SRADCON2	37h			CHS[3:0]					0000uuuu
SRAD					SRAD[7:0]				00000000
38h	STREET						SRAD[11:8]		uuuu0000
39h	SROFTL				ROUGH[7:0]				00000000
3Ah	SROFTH						SROFT[11:8]		uuuu0000

3.6.1.1 SRADCON0 Register (Address 34h)

Table 3-58

Bit number	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics		U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
SRADCON0				SRADACKS[1:0]				SRADCKS[1:0]	

Table 3-59

Bit address identifier		Function
5y4 SRADACKS[1:0]		ADC input signal sampling clock number selection signal
		SRADACKS[1:0]
		00
		16 ADC clocks
		01 8 ADC clocks
		10 4 ADC clocks
1y0	SRADCKS[1:0]	ADC clock frequency selection signal
		SRADCKS[1:0]
		00
		CPUCLK
		01
		CPUCLK/2
		10
		CPUCLK/4
		11
		CPUCLK/8

3.6.1.2 SRADCON1 Register (Address 35h)

Table 3-60

Bit number	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics		R/W-0	R/W-0	R/W-0	R/W-0 R/W-0		U-0	R/W-0	R/W-0
HEARTCON1		SRADEN	SRADS	OFTEN	CALIF	ENOV		VREFS[1:0]	

Table 3-61

Bit address identifier		Function
7	SRADEN	ADC Enable Bit 1: Enable 0: Disable
6	SRADS	ADC start bit/status control bit 1: Start, conversion in progress 0: Stop, conversion ends When set, ADC conversion is started and the bit is automatically cleared to 0 after the conversion is completed.

5	OFTEN	Conversion result selection control bit 1: The conversion result is placed in the SROFT register 0: The conversion result is placed in the SRAD register										
4	CALIF	Calibration control bit (valid when OFTEN is 0) 1: Enable correction, that is, the result of AD conversion is minus the SROFT offset voltage value 0: Disable correction, that is, the AD conversion result does not subtract the SROFT offset voltage value										
3	ENOV	Enable comparator overflow mode (valid when CALIF is 1) 1: Enable, overflow or underflow is directly the result of subtraction 0: Disable, underflow is 000h, overflow is ffFh										
2	RESERVE	reserve										
1:0	VREFS[1:0]	<p>ADC reference power selection Note: When switching between different reference voltages, it is recommended to delay 40uS before doing AD conversion</p> <table border="1"> <tr> <td>VREFS[1:0]</td> <td>AD reference voltage</td> </tr> <tr> <td>00</td> <td>VDD</td> </tr> <tr> <td>01</td> <td>PT3.0 external reference power input</td> </tr> <tr> <td>10</td> <td>Internal reference voltage</td> </tr> <tr> <td>11</td> <td>Internal reference voltage, PT3.0 can be connected to external voltage The capacitor is used as a built-in reference voltage filter. To improve accuracy.</td> </tr> </table>	VREFS[1:0]	AD reference voltage	00	VDD	01	PT3.0 external reference power input	10	Internal reference voltage	11	Internal reference voltage, PT3.0 can be connected to external voltage The capacitor is used as a built-in reference voltage filter. To improve accuracy.
VREFS[1:0]	AD reference voltage											
00	VDD											
01	PT3.0 external reference power input											
10	Internal reference voltage											
11	Internal reference voltage, PT3.0 can be connected to external voltage The capacitor is used as a built-in reference voltage filter. To improve accuracy.											

3.6.1.3 METCH register (address 2Fh)

Table 3-62

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
METCH	VTHSEL		REF_SEL[2:0]	PWMIS T3RATE[3] T2RATE[3]	P14_CUR			

Table 3-63

Bit address identifier		Function												
6~4 REF_SEL [2:0]		<p>Internal reference voltage selection</p> <table border="1"> <tr> <td>REF_SEL [2:0]</td> <td>Internal reference voltage</td> </tr> <tr> <td>0XX</td> <td>1.4V</td> </tr> <tr> <td>100</td> <td>1.4V</td> </tr> <tr> <td>101</td> <td>2.0V</td> </tr> <tr> <td>110</td> <td>3.0V</td> </tr> <tr> <td>111</td> <td>4.0V</td> </tr> </table>	REF_SEL [2:0]	Internal reference voltage	0XX	1.4V	100	1.4V	101	2.0V	110	3.0V	111	4.0V
REF_SEL [2:0]	Internal reference voltage													
0XX	1.4V													
100	1.4V													
101	2.0V													
110	3.0V													
111	4.0V													

3.6.1.4 SRADCON2 Register (Address 36h)

Table 3-64

Bit number Bit7 Characteristics	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
SRADCON2		CHS[3:0]					

Table 3-65

Bit address identifier		Function
------------------------	--	----------

7:0 CHS[3:0]		ADC input channel selection bits								
		CHS[3:0]								
		Input Channels								
		0000 AIN0 Input								
		0001 AIN1 Input								
		0010 AIN2 Input								
		0011 AIN3 Input								
		0100 AIN4 Input								
		0101 AIN7 input, internal 1/8VDD								
		0110 AIN8 input, internal reference voltage								
		0111 AIN9 input, internal ground								
		1000 AIN5 Input								
		1001 AIN6 Input								
		Others Reserved (internal ground)								

3.6.1.5 SRADL register (address 37h)

Table 3-66

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SRADL	SRAD[7:0]							

Table 3-67

Bit address identifier	Function
7:0 SRAD[7:0]	The lower 8 bits of ADC data are readable only.

3.6.1.6 SRADH register (address 38h)

Table 3-68

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
STREET	SRAD[11:8]							

Table 3-69

Bit address identifier	Function
3:0 SRAD[11:8]	The upper 4 bits of ADC data are readable only.

3.6.1.7 SROFTL register (address 39h)

Table 3-70

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0 R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SROFTL	ROUGH[7:0]							

Table 3-71

Bit address identifier	Function
7:0 SROFTL[7:0]	The lower 8 bits of the calibration value data

3.6.1.8 SROFTH register (address 3Ah)

Table 3-72

Bit number	Bit7 Characteristics	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SROFTH					SROFT[11:8]			

Table 3-73

Bit address identifier	Function
3:0 SROFT[11:8]	The upper 4 bits of the calibration value data

3.6.2 Relationship between input voltage and SRAD output data

Table 3-74 Relationship between input voltage and SRAD output data

Input voltage	SRAD[11:0] 6												
	11	10	9	8	7	6	5	4	3	2	1	0	
0/4096*VREF	0	0	0	0	0	0	0	0	0	0	0	0	
1/4096*VREF	0	0	0	0	0	0	0	0	0	0	0	1	
...													
...													
4094/4096*VREF 1		1	1	1	1	1	1	1	1	1	1	0	
4095/4096*VREF 1		1	1	1	1	1	1	1	1	1	1	1	

If the reference voltage value is determined and the ADC code value is obtained through ADC conversion, the ADC input voltage can be obtained through simple calculation.

The calculation formula is as follows

$$\text{ADC input voltage} = (\text{SRAD}[11:0]/4096)*\text{VREF}$$

For example, when the ADC reference voltage is 2V, the ADC conversion code value is 0x200, which is 512 in decimal. Then the input voltage value is

$$512/4096 \times 2 = 0.25V$$

3.6.3 Conversion time

$$12\text{-bit AD conversion time} = (1/\text{ADC clock frequency}) \times (12 + \text{CALIF} + \text{ADC input signal acquisition time})$$

Table 3-75 Conversion time description table

CLKDIV ⁽²⁾	CALIF	SRADCKS	SRADACKS	AD conversion time
4M refers to Order cycle	0	01	00	$1/((16MHz / 4) / 2) \times (12 + 0 + 16) = 14\mu s$
			01	$1/((16MHz / 4) / 2) \times (12 + 0 + 8) = 10\mu s$
		10	00	$1/((16MHz / 4) / 4) \times (12 + 0 + 16) = 28\mu s$
			01	$1/((16MHz / 4) / 4) \times (12 + 0 + 8) = 20\mu s$
			10	$1/((16MHz / 4) / 4) \times (12 + 0 + 4) = 16\mu s$
		11	00	$1/((16MHz / 4) / 8) \times (12 + 0 + 16) = 56\mu s$
			01	$1/((16MHz / 4) / 8) \times (12 + 0 + 8) = 40\mu s$
			10	$1/((16MHz / 4) / 8) \times (12 + 0 + 4) = 32\mu s$
			11	$1/((16MHz / 4) / 8) \times (12 + 0 + 2) = 28\mu s$

	2M refers to Order cycle	1	01	00	$1 / ((16\text{MHz} / 4) / 2) \times (12 + 1 + 16) = 14.5\mu\text{s}$
				01	$1 / ((16\text{MHz} / 4) / 2) \times (12 + 1 + 8) = 10.5\mu\text{s}$
				00	$1 / ((16\text{MHz} / 4) / 4) \times (12 + 1 + 16) = 29\mu\text{s}$
			10	01	$1 / ((16\text{MHz} / 4) / 4) \times (12 + 1 + 8) = 21\mu\text{s}$
				10	$1 / ((16\text{MHz} / 4) / 4) \times (12 + 1 + 4) = 17\mu\text{s}$
			11	00	$1 / ((16\text{MHz} / 4) / 8) \times (12 + 1 + 16) = 58\mu\text{s}$
				01	$1 / ((16\text{MHz} / 4) / 8) \times (12 + 1 + 8) = 42\mu\text{s}$
				10	$1 / ((16\text{MHz} / 4) / 8) \times (12 + 1 + 4) = 34\mu\text{s}$
				11	$1 / ((16\text{MHz} / 4) / 8) \times (12 + 1 + 2) = 30\mu\text{s}$
		0	01	00	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 0 + 16) = 28\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 0 + 8) = 20\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 0 + 4) = 16\mu\text{s}$
			10	00	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 0 + 16) = 56\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 0 + 8) = 40\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 0 + 4) = 32\mu\text{s}$
				11	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 0 + 2) = 24\mu\text{s}$
			11	00	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 0 + 16) = 112\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 0 + 8) = 80\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 0 + 4) = 64\mu\text{s}$
				11	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 0 + 2) = 48\mu\text{s}$
		1	01	00	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 1 + 16) = 29\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 1 + 8) = 21\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 2) \times (12 + 1 + 4) = 17\mu\text{s}$
			10	00	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 1 + 16) = 58\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 1 + 8) = 42\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 1 + 4) = 34\mu\text{s}$
				11	$1 / ((16\text{MHz} / 8) / 4) \times (12 + 1 + 2) = 30\mu\text{s}$
			11	00	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 1 + 16) = 116\mu\text{s}$
				01	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 1 + 8) = 84\mu\text{s}$
				10	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 1 + 4) = 68\mu\text{s}$
				11	$1 / ((16\text{MHz} / 8) / 8) \times (12 + 1 + 2) = 60\mu\text{s}$
		0	01	00	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 0 + 16) = 56\mu\text{s}$
				01	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 0 + 8) = 40\mu\text{s}$
				10	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 0 + 4) = 32\mu\text{s}$
				11	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 0 + 2) = 28\mu\text{s}$
			10	00	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 0 + 16) = 112\mu\text{s}$
				01	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 0 + 8) = 80\mu\text{s}$
				10	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 0 + 4) = 64\mu\text{s}$
				11	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 0 + 2) = 48\mu\text{s}$
			11	00	$1 / ((16\text{MHz} / 16) / 8) \times (12 + 0 + 16) = 224\mu\text{s}$
				01	$1 / ((16\text{MHz} / 16) / 8) \times (12 + 0 + 8) = 160\mu\text{s}$
				10	$1 / ((16\text{MHz} / 16) / 8) \times (12 + 0 + 4) = 128\mu\text{s}$
				11	$1 / ((16\text{MHz} / 16) / 8) \times (12 + 0 + 2) = 96\mu\text{s}$
		1	01	00	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 1 + 16) = 58\mu\text{s}$
				01	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 1 + 8) = 42\mu\text{s}$
				10	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 1 + 4) = 34\mu\text{s}$
				11	$1 / ((16\text{MHz} / 16) / 2) \times (12 + 1 + 2) = 15\mu\text{s}$
			10	00	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 1 + 16) = 116\mu\text{s}$

			01	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 1 + 8) = 84\text{us}$
			10	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 1 + 4) = 68\text{us}$
			11	$1 / ((16\text{MHz} / 16) / 4) \times (12 + 1 + 2) = 60\text{us}$
500K Instruction Week Expect	0	01	00	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 0 + 16) = 112\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 0 + 8) = 80\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 0 + 4) = 64\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 0 + 2) = 56\text{us}$
		10	00	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 0 + 16) = 224\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 0 + 8) = 160\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 0 + 4) = 128\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 0 + 2) = 96\text{us}$
		11	00	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 0 + 16) = 448\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 0 + 8) = 320\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 0 + 4) = 256\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 0 + 2) = 192\text{us}$
		01	00	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 1 + 16) = 116\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 1 + 8) = 84\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 1 + 4) = 68\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 2) \times (12 + 1 + 2) = 60\text{us}$
		10	00	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 1 + 16) = 232\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 1 + 8) = 168\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 1 + 4) = 136\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 4) \times (12 + 1 + 2) = 120\text{us}$
		11	00	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 1 + 16) = 464\text{us}$
			01	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 1 + 8) = 336\text{us}$
			10	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 1 + 4) = 272\text{us}$
			11	$1 / ((16\text{MHz} / 32) / 8) \times (12 + 1 + 2) = 240\text{us}$

(1) dark=16MHz

(2) Code options

(3) The AD conversion time changes with the change of fosc frequency.

3.6.4 ADC sampling time

The ADC sampling time is configured through the SRADCON0 register, the number of sampling clocks is configured through SRADACKS[1:0], and the SRADCKS[1:0] configures the ADC clock frequency.

$$\text{ADC sampling time} = \text{number of sampling clocks} / \text{ADC clock frequency}.$$

The following example uses the internal high-speed clock of 16MHz and the instruction cycle of 4MHz to calculate the sampling time under different configurations (the blue

Some of them are configurations that do not meet the requirements and are prohibited from use)

Table 3-76

SRADCKS	SRADACKS	AD sampling time
00	00	$16/(4\text{MHz}/1) = 4\text{us}$
	01	$8/(4\text{MHz}/1) = 2\text{us}$

		10	$4/(4\text{MHz}/1) = 1\mu\text{s}$	
		11	$2/(4\text{MHz}/1) = 0.5\mu\text{s}$	
01	01	00	$16/(4\text{MHz}/2) = 8\mu\text{s}$	
		01	$8/(4\text{MHz}/2) = 4\mu\text{s}$	
		10	$4/(4\text{MHz}/2) = 2\mu\text{s}$	
		11	$2/(4\text{MHz}/2) = 1\mu\text{s}$	
10	10	00	$16/(4\text{MHz}/4) = 16\mu\text{s}$	
		01	$8/(4\text{MHz}/4) = 8\mu\text{s}$	
		10	$4/(4\text{MHz}/4) = 4\mu\text{s}$	
		11	$2/(4\text{MHz}/4) = 2\mu\text{s}$	
11	11	00	$16/(4\text{MHz}/8) = 32\mu\text{s}$	
		01	$8/(4\text{MHz}/8) = 16\mu\text{s}$	
		10	$4/(4\text{MHz}/8) = 8\mu\text{s}$	
		11	$2/(4\text{MHz}/8) = 4\mu\text{s}$	

The ADC sampling time is related to the chip voltage and external load. The following table lists the sampling time requirements under typical conditions.

Table 3-77

parameter	Test conditions	Min	Typ	Max	Unit
Sampling time	3V \leq VDD \leq 5.5V, RAIN \geq 10 k Ω , 2.8V \leq VDD $<$ 3V,	4			μs
	RAIN \geq 10 k Ω , 2.6V \leq VDD $<$ 2.8V, RAIN \geq 10 k Ω	8			μs
		16			μs

RAIN is the input load resistance.

3.6.5 AD Offset Voltage Correction

Due to the discreteness of different chips, the offset voltage of AD may be positive or negative.

Methods for correcting offset voltage:

1. The chip was tested for ADC offset voltage during mass production, and the code value corresponding to the offset voltage (under 1.4V reference voltage) was stored in the information area address 0xF003, and the lower 8 bits are valid. The user needs to use the MOVP instruction in the user program to read the data.
2. Write the data into the SROFTL register and write 00h to SROFTH.
3. Set the OFTEN bit of the SRADCON1 register to 0, the CALIF bit to 1, and the ENOV bit to 0.
4. Enable ADC conversion, then the AD value read from SRADH/SRADL is the value minus the offset.

```

...
MOVlw F0H
MOVwf EADRH ; assign value to high byte address
MOVlw 03H
MOVwf EADRL; assign value to low byte address;
MOVp          execute read operation
NOP
MOVwf SROFTL
MOVlw 00H
MOVwf SROFTH
BCF SRADCON1,OFTEN
BSF SRADCON1,CALIF
BCF SRADCON1,ENOV
CLRF SRADCON1      ;VDD is the reference voltage, often=0,calif=0;enov=0,offex=0,vrefs=00
MOVlw 20h
MOVwf SRADCON2; chs[3:0]=0010, select channel 2
BSF SRADCON1,7 ; Enable ADC module
CALL delay_40us
...
BSF SRADCON1,6 ;srads=1, start conversion
BTFSC SRADCON1,6 ; Check if the conversion is completed
GOTO $-1
MOVlw sradl
MOVwf adtmp1_I
MOVlw sradh
MOVwf adtmpm_I
...

```

3.6.6 ADC reference voltage load capacity

The reference voltage of the ADC module is designed only for ADC reference. It can be output through the PT3.0 port and connected to an external filter capacitor to improve accuracy. The timing does not take into account the scenario of using the reference voltage to power the external circuit. Therefore, when the internal reference voltage needs to be output for use, it is necessary to ensure that the external equivalent resistance is greater than 50K Ω . If the equivalent resistance is less than 50K Ω , the output voltage accuracy cannot be guaranteed.

3.6.7 Digital Comparator

The ADC module can be used as a digital comparator. The input frequency of the measured signal should be less than 1/2 of the conversion frequency. The comparator rate is related to the AD conversion frequency. The difference between the two input signals must be less than VREF/2, otherwise the comparison result will be wrong.

Operation: 1) Select the signal input of the negative terminal of the comparator through the ADC channel selection control bit chs[3:0], then set OFTEN to 1 and CALIF to 0.

Set ENOV to 0, set SRADEN to 1 to enable ADC, set SRADS to 1 to start conversion, and write the conversion result to the SROFT register after the conversion is completed; you can also directly write the AD value of the negative terminal signal to the SROFT register, that is, manually specify the negative terminal voltage value. 2) Select the signal input of the positive terminal of the comparator through the ADC channel selection control bit chs[3:0], then set OFTEN to 0, clear CALIF to 1, Set ENOV to 1, set SRADEN to 1 to enable ADC, and set SRADS to 1 to start conversion.

3) The highest bit of the AD data, SRAD[11], is the result of the comparator. When it is 0, it means that the positive voltage is greater than the negative voltage. When it is 1, it means that the positive voltage is less than the negative voltage.

The voltage at the positive terminal is less than the voltage at the negative terminal. SRAD[11:0] is the difference, with the complement of the sign bit.

Compare the voltage values of channel 0 and channel 1. Channel 0 is connected to the positive terminal of the comparator, and channel 1 is connected to the negative terminal of the comparator.

```

...
CLRF SRADCON1      ;VDD is the reference voltage, often=0,calif=0,enov=0,offex=0,vrefs=00
BSF SRADCON1,5 ; often = 1, the result is saved in the sroft register
MOVLW 00h
MOVWF SRADCON2; chs[3:0]=0000, select channel 0 as the negative terminal of the comparator
BSF SRADCON1,7 ; Enable ADC module
CALL delay_40us
BSF SRADCON1,6 ;srads=1, start conversion
BTFSC SRADCON1,6 ; Check if the conversion is completed
GOTO $-1
...
MOVLW 10h
MOVWF SRADCON2; chs[3:0]=0001, select channel 1 as the positive terminal of the comparator
BCF SRADCON1,5 ;often=0
BSF SRADCON1,4 ;calif=1
BSF SRADCON1,3 ;enov=1
BSF SRADCON1,6 ;srads=1, start conversion
BTFSC SRADCON1,6 ; Check if the conversion is completed
GOTO $-1
BTFSC sradh,3
GOTO le_cmp; The positive terminal voltage is less than the negative terminal voltage
GOTO gt_cmp; the positive terminal is greater than or equal to the negative terminal voltage
...

```

Compare 1V voltage with the voltage of channel 1. Channel 1 is connected to the positive terminal of the comparator and 1V is connected to the negative terminal of the comparator. Assume that 5V VDD is used as the reference voltage, then the AD value of 1V is 0x333.

```

...
CLRF SRADCON1      ;VDD is the reference voltage, often=0,calif=0,enov=0,offex=0,vrefs=00
MOVLW 10h
MOVWF SRADCON2; chs[3:0]=0001, select channel 1 as the positive terminal of the comparator
BSF SRADCON1,4      ;calif=1
BSF SRADCON1,3      ;enov=1
MOVLW 03h
MOVWF srofth
MOVLW 33h
MOVWF sroftl        ;sroft register stores 333h, i.e. 1V as the negative terminal of the comparator
BSF SRADCON1,7 ; Enable ADC module
CALL delay_40us
BSF SRADCON1,6 ;srads=1, start conversion
BTFSC SRADCON1,6 ; Check if the conversion is completed
GOTO $-1
BTFSC sradh,3
GOTO le_cmp; The positive terminal voltage is less than the negative terminal voltage
GOTO gt_cmp; the positive terminal is greater than or equal to the negative terminal voltage
...

```

3.6.8 Internal measurement of VDD voltage

The user can use the internal reference voltage or external reference voltage input (the external reference voltage is fixed and does not change with the VDD voltage).

There are two methods to test the VDD voltage inside the chip.

When using an external reference voltage, an additional reference source

is required. When using an internal reference voltage, no additional hardware is required. However, using an internal reference voltage may cause the internal reference voltage value to

The accuracy of the test can be improved by correcting the internal reference voltage.

Connect 3V as reference voltage and measure VDD voltage. Select channel 5 and measure the AD value of 1/8VDD, then multiply it by 8 to get the AD value of VDD, and then multiply it by the reference voltage to get the VDD voltage.

```

...
CLRF SRADCON1 ;often=0,calif=0;enov=0,offex=0,vrefs=00
BSF SRADCON1,0 ;vrefs=01, select external reference voltage, connect to 3V
MOVLW 50h
MOVWF SRADCON2; chs[3:0]=0101, select channel 5, 1/8VDD
BSF SRADCON1,7 ; Enable ADC module
CALL delay_40us
BSF SRADCON1,6 ;srads=1, start conversion
BTFSC SRADCON1,6 ; Check if the conversion is completed
GOTO $-1
MOVLW sradl
MOVWF adtmp1
MOVLW sradh
MOVWF adtmpf
BCF status,c
RLF adtmp1
RLF adtmpf      ;AD value multiplied by 2
RLF adtmp1      ;AD value multiplied by 4
RLF adtmp1
RLF adtmpf      ;AD value multiplied by 8, the decimal point is between bit3 and bit4 of adtmpf
...

```

3.7 Analog Comparator

The CSU32M10/CSU32M11 has an analog comparator with two analog inputs C0P (PT3.4) and C0N (PT3.3).

Use VDD or PT3.4 minus 80/200/320/480mv as the comparator input, and C0 (PT3.1) pin can be used as the comparator output. This output is a digital output and there is no need to configure this port as an analog port.

The analog comparator does not work properly in SLEEP mode. Therefore, the analog comparator must be enabled and disabled before entering SLEEP mode.

3.7.1 Analog Comparator Block Diagram

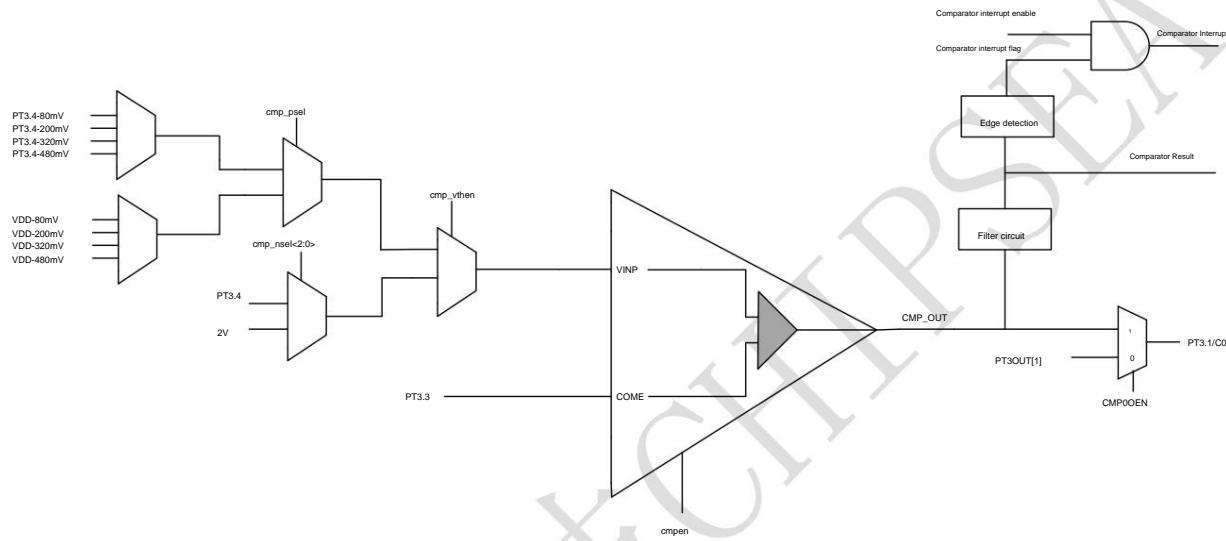


Figure 3-12 Analog comparator block diagram

3.7.2 Analog comparator function

3.7.2.1 Analog Comparator Enable

The analog comparator can be enabled in three ways, selected by the CMPENS[1:0] bits in the CMPCON2 register. When CMPENS[1:0] is configured as 00, the comparator is enabled by the CMPEN control of CMPCON0. A high level enables the comparator and a low level disables the comparator.

close

When CMPENS[1:0] is configured as 01, the comparator is enabled through the output control of PWM3, low level enables, high level disables,

At this time, CMPEN is invalid.

When CMPENS[1:0] is configured as 1x, the comparator is enabled through the output control of PWM2, low level enables, high level disables,

At this time, CMPEN is invalid.

3.7.2.2 Analog Comparator Input

The analog comparator input includes positive and negative terminals. The positive input can select PT3.4 input, 2V reference input or built-in threshold input, and the negative input is fixed to PT3.3 input, where the PT3.4 input voltage is required to be greater than 2.4V.

3.7.2.3 Comparator built-in threshold

The comparator has four built-in thresholds, namely VDD or PT3.4 minus 80/200/320/480mv, which are configured through CMPCON1 register CMPVTHS[1:0].

3.7.2.4 Analog Comparator Results

When the analog comparator's positive input is greater than its negative input, the analog comparator's output is high.

When the positive input is less than the negative input, the output of the analog comparator is low.

When the analog comparator input signal is close and has jitter, the comparator result will be unstable.

Set the filter circuit for filtering, and configure it through CMP_FLT[2:0] of the CMPCON1 register. The filter time range is 0~128 instructions. cycle.

When the CMPOEN bit in the CMPCON1 register is set to 1, the result of the analog comparator can be output through the PT3.1 port.

Digital output, no need to configure PT3.1 as analog port.

3.7.2.5 Analog Comparator Interrupt

When the result of the analog comparator changes, the analog comparator interrupt flag CMPIF is set. This bit is set to 1 by hardware and cleared to 0 by software.

The edge of the comparator interrupt generated by the comparator result can be configured through CMPINTS[1:0] of the CMPCON2 register, which can be configured as only the rising edge.

When the analog comparator result has a corresponding edge jump, the hardware automatically

When CMPIF is set, the chip will generate an analog comparator interrupt enable CMPIE when it is turned on and the general interrupt enable GIE is also turned on.

Device interrupt and enter the interrupt service function.

The analog comparator does not work properly in SLEEP mode, so the analog comparator cannot be used to wake up the SLEEP mode.

The block needs to be turned off in SLEEP mode, otherwise there will be power consumption.

3.7.2.6 Analog comparator result triggers PWM output stop

CSU32M10/CSU32M11 can change the PWM output to a high level by changing the comparator result. Comparator that triggers PWM output to stop

The resulting edge is the same as the edge that generates the interrupt, which is configured by CMPINTS[1:0] in the CMPCON2 register.

The PWM output stop of device 3 is controlled by separate enable bits, namely TM2STP and TM3STP. Only when the corresponding enable bits are enabled,

The PWM output of the corresponding timer can be stopped by setting the corresponding timer TMxR/TMxRH value to all 1s without turning off the PWM output.

The PWM output of Timer 3 includes normal PWM output and complementary PWM output.

When the output is stopped, their outputs will return to the default values.

3.7.3 Register Description

Table 3-78

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2						Bit1	Bit0	Power-On Reset
3Ch INTF2		CMPIF						TM3IF							Value 0uu0uuuu
3Dh INTE2		CMPIE						TM3IE							0uu0uuuu
6Ah CMPCON0		CMPEN				HYSN	CMP_PSEL			CMP_NSEL[2:0]		CMPOUT	0	0000000	
6Bh CMPCON1		CMPOEN	CMPVTH	IN	CMPVTHS[1:0]	VTHOEN			CMP_FLT[2:0]					00000000	
6Ch CMPCON2		CMPENS[1:0]			CMPINTS[1:0]						TM3STP	TM2STP	0	00000000	

3.7.3.1 CMPCON0 register (address 6AH)

Table 3-79

Bit number	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2		Bit1	Bit0
Characteristic	R/W-0		U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0
CMPCON0	CMPEN		HYSN	CMP_PSEL		CMP_NSEL[2:0]		CMPOUT		

Table 3-80

Bit address	identifier	Function
-------------	------------	----------

7	CMPEN	Comparator Enable Bit 1: Enable 0: Disable																		
6	Reserve	Must remain at 0																		
5	HYSEN	Comparator hysteresis function enable bit, closed by default 0: Disable comparator hysteresis function 1: Enable comparator hysteresis function																		
4	CMP_PSEL	When the built-in threshold is enabled (CMPVTHEN = 1), the comparator positive terminal selection signal 0: PT3.4 (input voltage needs to be greater than 2.4V) 1: VDD																		
3:1	CMP_NSEL[2:0]	When the built-in threshold enable is turned off (CMPVTHEN = 0), the comparator/operational amplifier positive input Signal selection <table border="1" data-bbox="536 630 1234 982"> <tr><td>CMP_NSEL[2:0] Input port</td><td></td></tr> <tr><td>3'b000 PT3.4 (input voltage needs to be greater than 2.0V)</td><td></td></tr> <tr><td>3'b 001 3'b</td><td>2.0V</td></tr> <tr><td>010 3'b 011</td><td>reserve</td></tr> <tr><td>3'b 100 3'b</td><td>reserve</td></tr> <tr><td>101 3'b 110</td><td>reserve</td></tr> <tr><td>3'b 111</td><td>reserve</td></tr> <tr><td></td><td>reserve</td></tr> <tr><td></td><td>reserve</td></tr> </table> Negative input is always connected to PT3.3	CMP_NSEL[2:0] Input port		3'b000 PT3.4 (input voltage needs to be greater than 2.0V)		3'b 001 3'b	2.0V	010 3'b 011	reserve	3'b 100 3'b	reserve	101 3'b 110	reserve	3'b 111	reserve		reserve		reserve
CMP_NSEL[2:0] Input port																				
3'b000 PT3.4 (input voltage needs to be greater than 2.0V)																				
3'b 001 3'b	2.0V																			
010 3'b 011	reserve																			
3'b 100 3'b	reserve																			
101 3'b 110	reserve																			
3'b 111	reserve																			
	reserve																			
	reserve																			
0	CMPOUT	Comparator comparison result, read only 1: C0P voltage is greater than C0N 0: C0P voltage is less than C0N																		

3.7.3.2 CMPCON1 register (address 6BH)

Table 3-81

Bit number	Bit7 Characteristic	Bit6	Bit5	Bit4 Bit3		Bit2	Bit1	Bit0
R/W-0		R/W-0	R/W-0 R/W-0	R/W-0		R/W-0	R/W-0	R/W-0
CMPCON1	CMPOEN CMPVTHEN		CMPVTHS[1:0]	VTHOEN		CMP_FLT[2:0]		

Table 3-82

Bit address identifier	Function								
7 CMPOEN	comparator result is output from PT3.1 port to enable control bit 0: Disable comparator result output from PT3.1 port 1: Enable the comparator result to be output from port PT3.1								
6 CMPVTHEN	Comparator built-in threshold function 0: Disable the built-in threshold of the comparator 1: Enable comparator built-in threshold								
5:4 CMPVTHS[1:0]	Comparator built-in threshold selection <table border="1" data-bbox="568 1841 1218 2005"> <tr><td>CMPVTHS[1:0] Comparator built-in threshold selection</td><td></td></tr> <tr><td>2'b00 VDD/PT3.4-80mv</td><td></td></tr> <tr><td>2'b01</td><td>VDD/PT3.4-200mv</td></tr> <tr><td>2'b10</td><td>VDD/PT3.4-320mv</td></tr> </table>	CMPVTHS[1:0] Comparator built-in threshold selection		2'b00 VDD/PT3.4-80mv		2'b01	VDD/PT3.4-200mv	2'b10	VDD/PT3.4-320mv
CMPVTHS[1:0] Comparator built-in threshold selection									
2'b00 VDD/PT3.4-80mv									
2'b01	VDD/PT3.4-200mv								
2'b10	VDD/PT3.4-320mv								

		2'b11	VDD/PT3.4-480mv																			
		VDD or PT3.4 is selected using CMP_PSEL.																				
3	VTHOEN	The comparator built-in threshold is output through the PT3.0 port control register 0: Disable the comparator built-in threshold to be output through PT3.0 port 1: Enable the built-in threshold of the comparator to be output through the PT3.0 port This function is only for testing and is not recommended for actual application.																				
2:0	CMP_FLT[2:0]	Comparator output filtering: Filter the comparator output to prevent the comparator output from The glitch in the result causes the interruption <table border="1"> <tr><th>CMP_FLT [2:0] Number of filter clocks</th></tr> <tr><td>000</td><td>reserve</td></tr> <tr><td>001</td><td>2 instruction cycles</td></tr> <tr><td>010</td><td>4 instruction cycles</td></tr> <tr><td>011</td><td>8 instruction cycles</td></tr> <tr><td>100</td><td>16 instruction cycles</td></tr> <tr><td>101</td><td>32 instruction cycles</td></tr> <tr><td>110</td><td>64 instruction cycles</td></tr> <tr><td>111</td><td>128 instruction cycles</td></tr> </table> If the comparator filter configuration is 000, there is no filtering function and it cannot be used. Configure more than 2 filter clocks.				CMP_FLT [2:0] Number of filter clocks	000	reserve	001	2 instruction cycles	010	4 instruction cycles	011	8 instruction cycles	100	16 instruction cycles	101	32 instruction cycles	110	64 instruction cycles	111	128 instruction cycles
CMP_FLT [2:0] Number of filter clocks																						
000	reserve																					
001	2 instruction cycles																					
010	4 instruction cycles																					
011	8 instruction cycles																					
100	16 instruction cycles																					
101	32 instruction cycles																					
110	64 instruction cycles																					
111	128 instruction cycles																					

3.7.3.3 CMPCON2 register (address is 6CH)

Table 3-83

Bit number	Bit7	Characteristic	Bit6	Bit5	Bit4	Bit3		Bit2	Bit1	Bit0
R/W-0			R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0
CMPCON2		CMPENS[1:0]		CMPINTS[1:0]					TM3STP	TM2STP

Table 3-84

Bit address identifier		Function
7:6 CMPENS[1:0]		Comparator Enable Control Register 00: Comparator enable is controlled by software, that is, controlled by CMPEN in CMPCON0 01: Comparator enable is controlled by PWM3 output, low level enables, high level disables 1x: Comparator enable is controlled by PWM2 output, low level enables, high level disables
5:4 CMPINTS[1:0]		Comparator output result generates interrupt control register 00: The comparator interrupt is generated on the rising edge of the comparator result 01: The falling edge of the comparator result generates a comparator interrupt 1x: Both rising and falling edges of the comparator result generate a comparator interrupt.
3:2 Reserved		reserve
1	TM3STP	Comparator interrupt control stops the PWM output of Timer 3 0: Disable comparator output and stop PWM output of timer 3 1: Enable comparator output result to stop PWM output of timer 3 When this bit is enabled and the comparator interrupt edge is configured by CMPINTS[1:0], if If an interrupt occurs, TM3R[11:0] of Timer 3 is configured to 12'hFFF by hardware. To ensure that PWM is turned off, TMnIN[11:0] (n=2,3) cannot be configured as 12'hFFF because PWM can only output high level when TMnR > TMnIN + 1 (n=2,3).
0	TM2STP	The comparator output result controls the PWM output enable bit that stops timer 2. 0: Disable comparator output and stop PWM output of timer 2

		<p>1: Enable comparator output result to stop PWM output of timer 2</p> <p>When this bit is enabled and the comparator interrupt edge is configured by CMPINTS[1:0], if</p> <p>When an interrupt occurs, TM2R[11:0] of Timer 3 is configured as 12'hFFF by hardware.</p>
--	--	--

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3.8 5*8 software LCD

3.8.1 Register Description

Table 3-85 LCD register list

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2			Bit1	Bit0	Power-On Reset value
46h	LCD COM							LCD COM[4:0]				uuu00000

3.8.1.1 LCD COM Register (Address 46h)

Table 3-86

Bit number	Bit7 Characteristics	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
LCD COM				LCD COM[4:0]							

Table 3-87

Bit address identifier		Functionality
7y5	RESERVE	Retention
4	LCD COM[4]	<p>PT1.1 port as LCD COM port enable bit</p> <p>0: Disable PT1.1 from being used as LCD COM port</p> <p>1: Enable PT1.1 as LCD COM port</p>
3	LCD COM[3]	<p>PT1.6 port as LCD COM port enable bit</p> <p>0: Disable PT1.6 from being used as LCD COM port</p> <p>1: Enable PT1.6 as LCD COM port</p>
2	LCD COM[2]	<p>PT5.0 port as LCD COM port enable bit</p> <p>0: Disable PT5.0 from being used as LCD COM port</p> <p>1: Enable PT5.0 as LCD COM port</p>
1	LCD COM[1]	<p>PT5.1 port as LCD COM port enable bit</p> <p>0: Disable PT5.1 from being used as LCD COM port</p> <p>1: Enable PT5.1 as LCD COM port</p>
0	LCD COM[0]	<p>PT1.4 port as LCD COM port enable bit</p> <p>0: Disable PT1.4 from being used as LCD COM port</p> <p>1: Enable PT1.4 as LCD COM port</p>

3.8.2 Software LCD Implementation Method

The method to implement 1/2 BIAS LCD driving by software is as follows:

When 1/2VDD output is required, configure the corresponding LCD COM[n] (n=0, 1, 2, 3, 4) to 1, and set the corresponding IO

If the IO port is configured as input and the pull-up resistor and pull-down resistor of the IO port are enabled at the same time, the corresponding IO port output is 1/2VDD.

0V or VDD can be directly realized through the IO port output function, so you only need to configure the corresponding IO port as a normal output

When configured as a common IO port, LCD COM[n] (n=0, 1, 2, 3, 4) needs to be configured as 0 to ensure that the corresponding IO port is Ordinary IO port.

3.9 Data Lookup Table

The MOVP instruction can be used to read data from the user program memory and EEPROM. The address range of the user program memory is The range of the EEPROM address is 000H~7FFH, and the EEPROM address range is 0x2000~0x207F. The TBLP instruction can be used to write to the EEPROM. Each EEPROM address stores one byte of data, so during read and write operations, only the lower 8 bits of data are valid.

In user mode, the program memory (MTP) does not support write operations.

3.9.1 Unlock for Write Operation

When writing to the EEPROM, the write protection must be unlocked. When unlocking the EEPROM write operation, the WRPRT register must be connected to Continue to write 96H, 69H, and 5AH. When writing to other address registers, the unlocking will automatically fail.

It is recommended to disable the global interrupt enable when executing the TBLP instruction. The write operation time is 3 instruction cycles when the write operation is not unlocked.

3.9.2 EEPROM write operation flow

The steps for writing to EEPROM are as follows:

- ÿ The EEPROM write operation takes a long time. It is recommended to enable the WDT module (if it is already enabled, this step is not required) and execute Line CLRWDT
- ÿ Configure {EADRH, EADRL} write operation address.
- ÿ Disable global interrupt enable GIE
- ÿ Write the unlock sequence to the WRPRT register to unlock the write protection.
- ÿ Configure WORK write operation data.
- ÿ Execute instruction TBLP XH operation
- ÿ After the write operation is completed, check the CHKRSLT bit of the ISPCON1 register. When the bit is 0, it means that the write operation verification failed.

The read data is inconsistent with the written data. When this bit is 1, it indicates that the write operation is successful.

- ÿ Turn on the global interrupt enable GIE

3.9.3 MTP and EEPROM read operations

The steps for reading MTP and EEPROM are as follows:

- ÿ Configure {EADRH, EADRL} write operation address.
- ÿ Disable global interrupt enable GIE
- ÿ Execute instruction MOVP operation
- ÿ Reading completed
- ÿ Turn on the global interrupt enable GIE

EADRH/EADRL provides the data address for the read operation; EDATH/WORK provides the data used for the read operation. The MTP read operation is based on

The read operation of EEPROM is based on a byte (8 bits), and the 8-bit data is stored in the WORK register.

In the device.

When performing a read operation, enter the corresponding value in the address register, and then execute the MOVP instruction to obtain the data at the corresponding MTP address. Read into the EDATH/WORK register. It takes 6 instruction cycles to execute a read operation.

MOVLW 03H	
MOVWF EADRH	; Assign value to high byte address
MOVLW 00H	
MOVWF EADRL	; Assign value to low byte address
BCF DON'T,GIVE	
MOVP	;Perform a read operation
NOP	
MOVWF DATAH	;Store low 8 bits of data
MOVFW EDATH	
MOVWF DATAH	;Store high 8 bits of data
BSF DON'T,GIVE	
...	

3.9.4 EEPROM Write Operation

The EEPROM address range is 0x2000~0x207F. The operation of EEPROM is in bytes (8 bits). The EEPROM size is 128 ×8bit, when reading and writing EEPROM, the upper 8 bits are invalid, and only the lower 8 bits are valid.

Ensure that the VDD voltage is greater than 2.5V, otherwise it may cause write failure.

3.9.5 Register Description

Table 3-88 Data lookup register list

land	NameBit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power on Bit
Address 05h	WORK									value 00000000
0Ah	EADRH									00000000
0Mh	EADRL									00000000
0Ch	EDATH									00000000
60h	ISPCON1	CHKRSLT								0uuuuuuuu
63h	WRPRT									WRPRTF 00000000

3.9.5.1 EADRH register (address 0Ah)

Table 3-89

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EADRH	EADR[15:8]							

Table 3-90

Bit address identifier		
7:0 EADR[15:8]		Function: Read operation address high bit. This register and EADRL form a 16-bit address control register. To access 2K*16 MTP program memory and 128 byte EEPROM space.

3.9.5.2 EADRL Register (Address 0Bh)

Table 3-91

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EADRL	EADR[7:0]							

Table 3-92

Bit address identifier		
7:0 EADR[7:0]		Function read operation address lower 8 bits, this register and EADRH form a 16-bit address control register. Can access 2K*16 MTP program memory and 128 byte EEPROM space.

3.9.5.3 EDATH register (address 0Ch)

Table 3-93

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDIT	EDIT [7:0]							

Table 3-94

Bit address identifier		The
7:0 EDIT[7:0]		function reads the high 8 bits of data, and the low 8 bits of data are stored in the WORK register, together forming a 16-bit data.

3.9.5.4 ISPCON1 register (address is 60H)

Table 3-95

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R-0	U-0						
ISPCON1	CHKRSLT							

Table 3-96

Bit address identifier		Function
7	CHKRSLT	TBLP Read the written value for verification, read only 0: Verification failed, the read data is inconsistent with the written data 1: Verification is successful, the read data is consistent with the written data Each time a TBLP is performed, the write address is automatically read to verify the read data and the write address. Whether the input data is consistent, if it is consistent, this position is 1, otherwise it is cleared.
6:0	RESERVE	reserve

3.9.5.5 WRPRT register (address 63H)

Table 3-97

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	W-0	W-0	W-0	W-0	W-0	W-0	W-0	R/W-0

WRPRT								WRPRTF
-------	--	--	--	--	--	--	--	--------

Table 3-98

Bit address identifier		When
0	WRPRTF	<p>the function unlocks the EEPROM write operation, it is necessary to continuously write 96H, 69H, 5AH, if unlocking is successful, WRPRTF is set to 1. WRPRTF indicates whether unlocking is successful.</p> <p>The position is read-only.</p> <p>0: unlock failed 1: Indicates successful unlocking</p>

3.10 Input Logic Level Voltage Configuration

3.10.1 Register Description

Table 3-99 METCH register list

land site	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power on Place value
2Fh	METCH	VTHSEL		REF_SEL[2:0]	PWMIS	T3RATE[3]	T2RATE[3]	P14_CUR	00000000	

3.10.1.1 METCH register bit function table

Table 3-100

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
METCH	VTHSEL		REF_SEL[2:0]	PWMIS	T3RATE[3]	T2RATE[3]	P14_CUR	

Table 3-101

Bit address	identifier function	Input logic level voltage control signal						
7	VTHSEL	VTHSEL Input Logic Level						
		0	Symbol	Parameter	Min	Typ	Mak	Unit
			VIH1	Digital input high level 0.75VDD	Reset input			In
				high level 0.8VDD				In
			VIL1	Digital input low level reset			0.3VDD	V
		1		input low level symbol			0.2VDD	V
			parameter		Min	Typ	Mak	Unit
			VIH2	Digital input high level reset		0.5VDD		In
				input high level		0.5VDD		In
			VIL2	Digital input low level Reset		0.5VDD		In
				input low level		0.5VDD		In

3.11 Output Current Configuration

PT5.0 and PT5.1 ports support large drive output, and the output current can be configured through the PWMIS bit of the METCH register.

PT5.0 and PT5.1 can be configured with IOL=20mA@5V or IOL=53mA@5V for sink current and IOH=20mA@5V or IOH=53mA@5V for source current.

IOH=25mA@5V

3.11.1 Register Description

Table 3-102 Register list

land site	Name	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power on Place value
2Fh	METCH	VTHSEL		REF_SEL[2:0]	PWMIS	T3RATE[3]T2RATE[3]	P14_CUR	00000000			

3.11.1.1 METCH Register (Address 2Fh)

Table 3-103

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
METCH	VTHSEL	REF_SEL[2:0]	PWMIS	T3RATE[3]T2RATE[3]	P14_CUR			

Table 3-104

Bit address	identifier function	
3	PWMIS	PT5.0 and PT5.1 current selection 0: IOL=20mA@5V; IOH=20mA@5V 1: IOL=53mA@5V; IOH=25mA@5V
0	P14_CUR	PT1.4 Output current (IOH) selection (valid only when the current limit code option RES_OP[0] is configured as 1). When the current limit code option is configured as 0, the driving capability of the PT1.4 port is normal. Configured as 0) 0: PT1.4 IOH output current is 2.8mA@5V 1: PT1.4 IOH output current is 1.4mA@5V

3.12 Constant Current Source

CSU32M10/CSU32M11 has a built-in 50mA constant current source, in the voltage range of 2.7V~4.3V, temperature range of -20°C~70°C
Internal accuracy is ±5%, output through PT3.2 port.

3.12.1 Register Description

Table 3-105 Register list

Address	Name	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset value
6Dh	CCSCon									CCSOEN	uuuuuuu0

3.12.1.1 CCSCON Register (Address 6Dh)

Table 3-106

Bit number Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Characteristics	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
CCSCon								CCSOEN

Table 3-107

Bit Address	Identifier Function	7: 1
Reserved	Reserved	
0	CCSOEN	Current source output enable control bit 0: Disable 50mA current source output from PT3.2 port 1: Enable 50mA current source output from PT3.2 port

3.13 Online Debug Function (ICD)

3.13.1 Overview of online debugging function

CSU32M10/CSU32M11 supports online debugging function, communicates with CS_Link through PT1.5 port (SWD), and cooperates with IDE realizes online debugging function, and it is an open-drain output port when used as SWD port.

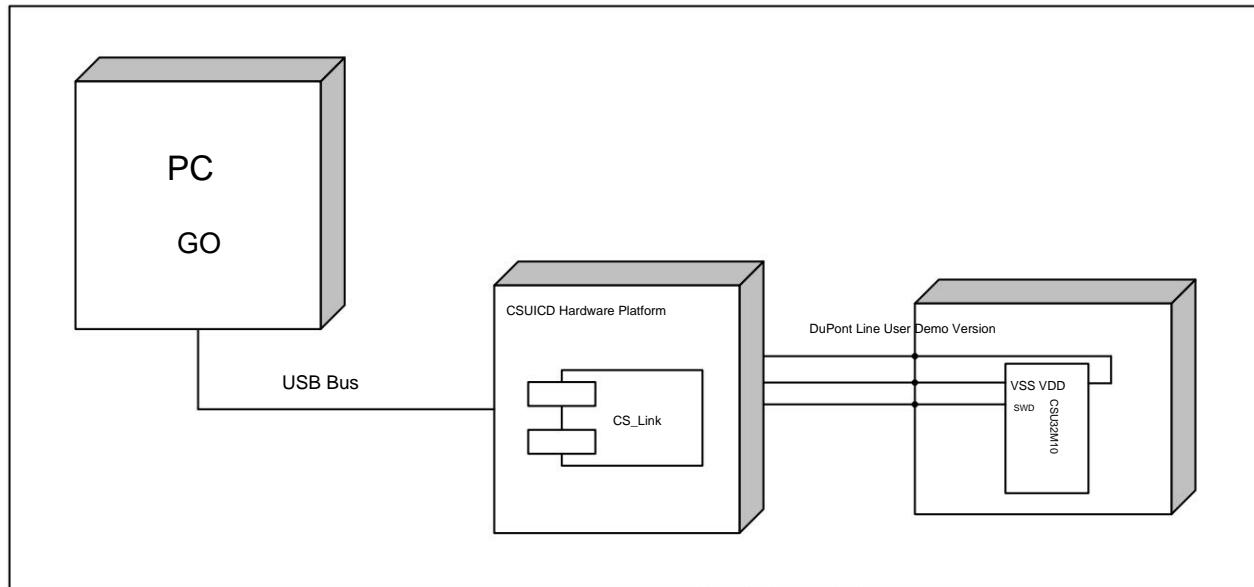


Figure 3-13 Online debugging system block diagram

3.14 Burning module

Burner interface

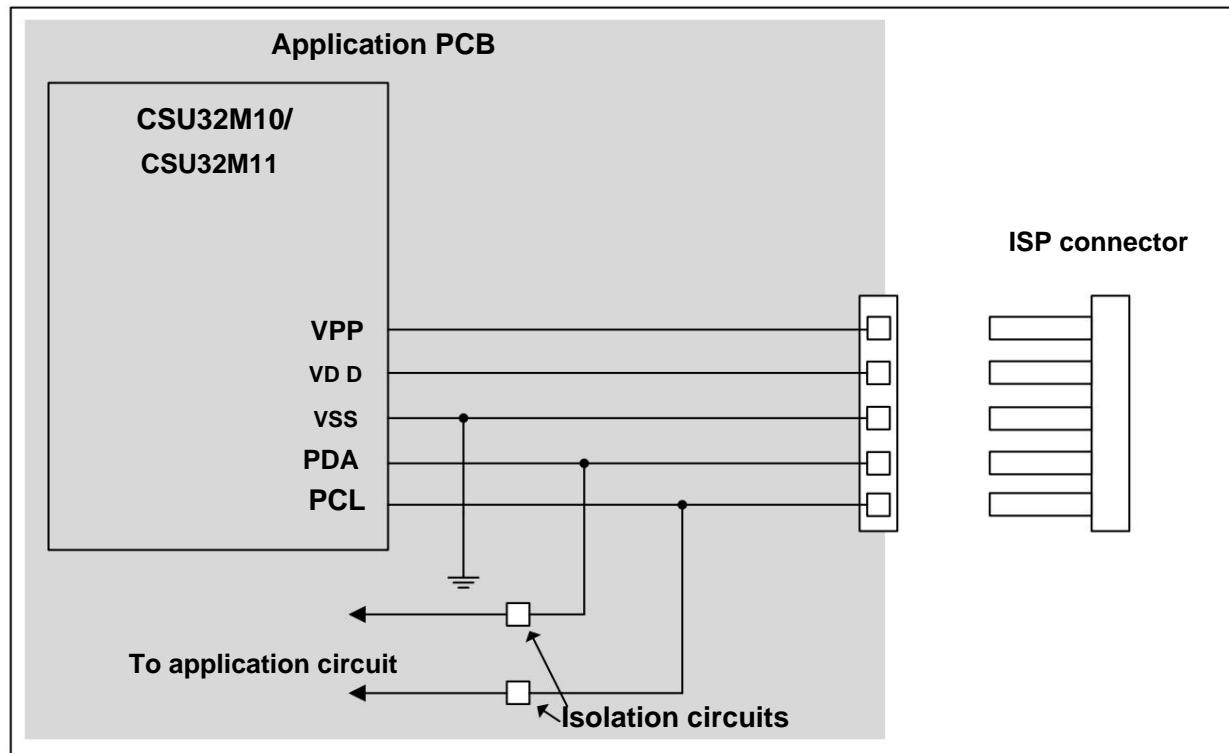


Figure 3-14 Interface diagram of the programmer

Table 3-108 Programming interface description

Port Name	Type	Description	Input
VPP		PT1[3] port, programming power supply	
VDD		Input power positive terminal	
VSS		Input power negative terminal	
PDA		Input/output PT1[4] port, data signal	
PCL	enter	PT1[5] port, clock signal	

3.15 Code Options

The chip will perform an inverse code check on the code option area information. If the inverse code check fails after power-on, the chip will remain in reset state. This measure is mainly used to prevent abnormal chip operation caused by abnormal rewriting of chip code option data.

state.

3.15.1 OPTION1

The address is ID area 0xF000.

Table 3-109

Bit-15	Bit-14 Bit-13		Bit-12 Bit-11		Bit-10	Bit-9	Bit-8
~CLKDIV[1:0]		~LVD_SEL[1:0]		~RESET_PIN ~WWDT_HALT		Reserve ~ SECURITY	
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CLKDIV[1:0]		LVD_SEL[1:0]		RESET_PIN	WWDT_HALT	Preserve SECURITY	

Table 3-110

Bit address identifier function			
15:14	~CLKDIV[1:0]	must be the inverted value of CLKDIV[1:0]	
13:12	~LVD_SEL[1:0]	must be the inverted value of LVD_SEL[1:0]	
11	~RESET_PIN	must be the negated value of RESET_PIN	
10	~WWDT_HALT	must be the negated value of WWDT_HALT	
9	RESERVE	Fixed to 0	
8	~SECURITY	must be the negation of SECURITY	
7:6	CLKDIV[1:0]	Instruction cycle selection	
		CLK_DIV[1:0] instruction cycle	
		00	Instruction cycle = 4 clock cycles (default)
		01	instruction cycle = 8 clock cycles
		10	instruction cycle = 16 clock cycles
		11	Instruction cycle = 32 clock cycles
5:4	LVD_SEL[1:0]	LVD Configuration	
		LVD_SEL[1:0] Function	
		00	2.0V power-on/power-off reset. Low voltage detection disabled. (Default)
		01	2.0V power-on/power-off reset. The LVD24 of STATUS is used as a 2.4V low voltage detector. The LVD36 of STATUS acts as a 3.6V low voltage detector.
		10	2.4V power-on/power-off reset. The LVD36 of STATUS acts as a 3.6V low voltage detector.
		11	3.6V power-on/power-off reset.
3	RESET_PIN	Reset pin selection	
		1: PT1.3 is used as reset pin	
		0: PT1.3 is used as a normal input and output port (default)	
2	WWDT_HALT	WWDT behavior configuration in HALT mode	
		0: WWDT continues counting in HALT mode and a reset is generated after an overflow.	
		1: WWDT does not count in halt mode. (Default)	

1	RESERVE	Reserved, fixed at 1					
0	SECURITY	Burn mode code confidentiality bit 0: Enable code encryption 1: Disable code encryption (default)					

3.15.2 OPTION2

The address is ID area 0xF001.

Table 3-111

Bit-15	Bit-14 Bit-13		Bit-12 Bit-11		Bit-10	Bit-9	Bit-8
reserve	WDT_CFG DR	VE_CF G	ICK_SEL[1:0]		RES_OP[1]]	ICK_SEL [2]	RES_OP[0]
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
reserve	WDT_CFG DR	VE_CF G	ICK_SEL[1:0]		RES_OP[1]]	ICK_SEL [2]	RES_OP[0]

Table 3-112

Bit address identifier														
15	RESERVE	Function must be 0												
14	~WDT_CFG	Must be the inverted value of WDT_CFG												
13	~DRIVE_CFG	Must be the inverse value of DRIVE_CFG												
12:11	~ICK_SEL[1:0]	must be the inverted value of ICK_SEL[1:0]												
10	~RES_OP[1]	must be the negated value of RES_OP[1]												
9	~ICK_SEL[2]	must be the inverted value of ICK_SEL[2]												
8	~RES_OP[0]	must be the negated value of RES_OP[0]												
7	RESERVE	Must be 1												
6	WDT_CFG	WDT module enable and internal 32K low speed oscillator enable configuration bit 1: WDT module enable and internal 32K low speed oscillator enable are configured by software (default) 0: WDT module enable and internal 32K low-speed oscillator enable are fixed on and cannot be modified by software. change.												
5	DRIVE_CFG	PT1.0, PT3.5 IOL configuration 1: IOL is the normal driving capacity, i.e. 20mA. (Default) 0: IOL is 30mA												
4:3	ICK_SEL[1:0]	Internal crystal selection <table border="1"> <tr> <td>ICK_SEL [2:0]} 000</td> <td>Internal crystal frequency</td> </tr> <tr> <td></td> <td>2MHz</td> </tr> <tr> <td>001</td> <td>4MHz</td> </tr> <tr> <td>010</td> <td>8MHz</td> </tr> <tr> <td>011</td> <td>16MHz (default)</td> </tr> <tr> <td>1xx</td> <td>32MHz</td> </tr> </table>	ICK_SEL [2:0]} 000	Internal crystal frequency		2MHz	001	4MHz	010	8MHz	011	16MHz (default)	1xx	32MHz
ICK_SEL [2:0]} 000	Internal crystal frequency													
	2MHz													
001	4MHz													
010	8MHz													
011	16MHz (default)													
1xx	32MHz													
2	RES_OP[1]	Drop-down code options 1: PT3.4, PT5.1 connect to 10K pull-down resistor, PT1.0 connect to 3K pull-down resistor, PT1.3 port Connect 400K Ω pull-down resistor (default) 0: The above IOs are not pulled down, and the driving capability is normal.												
1	ICK_SEL[2]	See internal crystal selection above for description												

0	RES_OP[0]	Current limiting code options 1: PT1.1, PT1.5 port drive capability is configured to 5mA (default) 0: The above IO drive capability is normal value
---	-----------	---

3.15.3 ICD Function Configuration Options

The address is ID area 0xF002.

Table 3-113

Bit-15	Bit-14 Bit-13		Bit-12 Bit-11		Bit-10	Bit-9	Bit-8
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
		ICD_CFG[3:0]					

Table 3-114

Bit address identifier 15:4	Function
Reserve	
3:0	ICD mode enable option 1111: Enable ICD function Others: Disable ICD function When the ICD function is enabled, the PT1.5 port is fixed as a debug port and cannot be used as a normal IO port. The internal high-speed clock will not be turned off in SLEEP mode.

3.15.4 ADC Offset Voltage Correction

ADC offset voltage corresponding code value, using 1.4V reference voltage for testing, address is ID area 0xF003, lower 8 bits.

When using this value, you need to use MOVP to read the address data. The calibration value must be in the range of 0~5, so pay attention to the range when using it.

4 MCU instruction set

Table 4-1 MCU instruction set

instruction	operate	Instruction cycle flag 1	
ADDLW k	[W] ÿ [W]+k		C,DC,Z
ADDP CW	[PC] ÿ[PC]+1+[W]	2	~
ADDWF f,d	[Destination] ÿ[f]+[W]	1	C,DC,Z
ADDWFC f,d	[Destination] ÿ[f]+[W]+C	1	C,DC,Z
ANDLW k	[W] ÿ [W] AND k	1	wrte
ANDWF f,d	[Destination] ÿ [W] AND [f] [f]ÿ0 [f]ÿ1	1	wrte
BCF f,b		1	~
BSF f,b		1	~
BTFS C f,b	Jump if[f]=0	1/2	~
BTFS S f,b	Jump if[f]=1	1/2	~
CALL k	Push PC+1 and Goto K [f]ÿ0	2	~
CLRF f		1	wrte
CLRWD T	Clear watch dog timer [f]ÿNOT([f])	1	~
COMF f,d		1	wrte
Apparently	Decimal Adjust W	1	C,DC
DEC F f,d	[Destination] ÿ[f]-1	1	wrte
DECFSZ f,d	[Destination] ÿ[f]-1,jump if the result is zero	1/2	~
GOTO k	PCÿk	2	~
HALT	CPU Stop	1	~
INCF f,d	[Destination] ÿ[f]+1	1	wrte
INCFSZ f,d	[Destination] ÿ[f]+1,jump if the result is zero	1/2	~
IORLW k	[W] ÿ [W] OR k	1	wrte
IORWF f,d	[Destination] ÿ [W] OR [f]	1	wrte
MOVFW f	[W] ÿ [f]	1	~
MOVLW k	[W] ÿ k	1	~
MOV P	Read table list [f]ÿ[W]	3	~
MOVWF f		1	~
NOP	No operation	1	~
POP	Pop W and Status	2	~
PUSH	Push W and Status	2	~
RETFIE	Pop PC and GIE =1	2	~
RETLW k	RETURN and W=k	2	~
RETURN	POP PC	2	~
RLF f,d	[Destination<n+1>] ÿ[f<n>]	1	C,Z
RRF f,d	[Destination<n-1>] ÿ[f<n>]	1	C,Z
SLEEP	STOP OSC	1	PD
SUBLW k	[W] ÿ k - [W]	1	C,DC,Z
SUBWF f,d	[Destinnation] ÿ [f] - [W]	1	C,DC,Z
SUBWFC f,d	[Destinnation] ÿ [f] - [W] - 1 + C	1	C,DC,Z

SWAPF f,d	swap f	1	-
TBLP k	Write memory	-	-
XORLW k	[W]y[W] XOR k	1	with
XORWF f,d	[Destination] y [W] XOR [f]	1	with

parameter description:

f: Data memory address (00H ~7FH)

W: Working register

k: immediate value

d: Destination address selection: d=0: the result is stored in the working register, d=1: the result is stored in the data memory unit f

b: Bit selection (0~7)

[f]: the content of address f

PC: Program Counter

C: Carry flag

DC: Half-add carry flag

Z: The result is zero.

PD: Sleep flag

TO: Watchdog overflow flag

WDT: Watchdog Timer

Table 4-2 MCU instruction set description

1

ADDLW	Add immediate value to working register
instruction format	ADDLW K (0<=K<=FFh) 6 8
	(W)<—(W)+K
Operation	C, DC, Z
flag bit	The contents of the working register are added to the immediate value K and the result is saved in the working register
	1
description cycle example ADDLW 08h	Before the instruction is executed: W=08h After the instruction is executed: W=10h

2

ADDP CW	Add the contents of W to PC
Instruction Format	ADDP CW 14
operate	(PC)<—(PC)+1+(W) When (W) < 7Fh (PC)<—(PC)+1+(W)-100h Others
Flag bit	No
	Load address PC+1+W into PC
	2
description cycle example 1 ADDP CW	Before the instruction is executed: W=7Eh yPC=0212h After the instruction is executed:

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	PC=0291h
Example 2 ADDPCW	Before instruction execution: W=80h, PC=0212h After instruction execution: PC=0193h
Example 3 ADDPCW	Before instruction execution: W=FEh, PC=0212h After instruction execution: PC=0211h

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ADDWF	Add working register to f ADDWF
Instruction Format	f,d 0<=f<=FFh d=0,1 7
	7 [Destination address]<—(f)+(W)
Operation	C ₇ CD ₀ Z
Flag Description	Add the contents of f and the working register together. If d is 0, the result is stored in the working register. If d is 1, the result is stored in f.
Cycle	1
Example 1 ADDWF f 0	Before the instruction is executed: f=C2h W=17h After the instruction is executed f=C2h W=D9h
Example 2 ADDWF f 1	Before instruction execution f=C2h W=17h After the instruction is executed f=D9h W=17h

4

ADDWFC	Add W f and the carry bit
instruction format	ADDWFC f ₇ d 0<=f<=FFh d=0,1 7 7
	(target address)<—(f)+(W)+C
Operation	C, DC, Z
Flag Description	Add the contents of the working register to the contents of f and the carry bit When d is 0, the result is saved in the working register When d is 1, the result is saved in f
Cycle	1
Example ADDWFC f ₇ 1	Before instruction execution C=1 f=02h W=4Dh After the instruction is executed C=0 f=50h W=4Dh

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ANDLW	AND the working register with the immediate value
Instruction Format	ANDLW K 0<=K<=FFh 6 8
	(W)<—(W) AND K
Operation	W ₇ W ₆ W ₅ W ₄ W ₃ W ₂ W ₁ W ₀
flag bit	AND the contents of the working register with the 8-bit immediate value, and save the result in the working register.
	1
description cycle example ANDLW 5Fh	Before the instruction is executed W=A3h After the instruction is executed W=03h

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ANDWF	AND the contents of the working register with f
Instruction Format	ANDWF fyd 0<=f<=FFh d=0,1 7 7
	(destination address)<—(W) AND (f)
Operation	with
Flag Description	AND the contents of the working register with the contents of f If d is 0, the result is saved in the working register If d is 1, the result is saved in f
Cycle	1
Example 1 ANDWF f0	Before the instruction is executed W=0Fh f=88h After the instruction is executed W=08h f=88h
Example 2 ANDWF f1	Before the instruction is executed W=0Fh f=88h After the instruction is executed W=0Fh f=08h

7

BCF	Clear a bit of f
Instruction Format	BCF fyb 0<=f<=FFh 0<=b<=7 BCF b f 4 3 7
	(f[b])<—0
Operation	none
flag bit	The bth position of F is 0
	1
description cycle example BCF FLAG 2	Before the instruction is executed: FLAG=8Dh After the instruction is executed: FLAG=89h

8

BSF	F's b position 1
Instruction Format	BSF fyb 0<=f<=FFh 0<=b<=7 BSF bf 4 3 7
	(f[b])<—1
Operation	none
flag bit	Set bit b of f to 1
	1
description cycle example BSF FLAG 2	Before the instruction is executed FLAG=89h After the instruction is executed FLAG=8Dh

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BTFSC	If bit[b] of register f is 0, jump
-------	------------------------------------

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Instruction Format	BTFSC fÿb 0<=f<=FFh 0<=b<=7 BTFSC bf 4 3 7
	Skip if (f[b])=0
Operation	none
Flag Description	If the bit of f is 0, the next instruction fetched will be discarded and an empty instruction group will be executed. into a two-cycle instruction.
Cycle	If there is no jump, it takes 1 instruction cycle, otherwise it takes 2 instruction cycles
Example	Before the program is executed PC=address(NODE)
NODE BTFSC FLAG 2	After the instruction is executed If(FLAG[2])=0 PC=address(OP2)
OP1:	If(FLAG[2])=1 PC=address(OP1)
OP2:	

10

BTFS	If bit[b] of register f is 1, jump
instruction format	BTFS fÿb 0<=f<=FFh 0<=b<=7 BTFS bf 4 3 7
	Skip if (f[b])=1
Operation	none
Flag Description	If the bit of f is 1, the next instruction fetched will be discarded and an empty instruction group will be executed. into a two-cycle instruction.
Cycle	If there is no jump, it takes 1 instruction cycle, otherwise it takes 2 instruction cycles
Example	Before the program is executed PC=address(NODE)
NODE BTFS FLAG 2	After the instruction is executed If(FLAG[2])=0 PC=address(OP1)
OP1:	If(FLAG[2])=1 PC=address(OP2)
OP2:	

11

CALL	Subroutine call
instruction format	CALL K 0<=K<=7FFh 3 11
operate	(top stack)←PC+1 PC←K
Flag bit	none
	When calling a subroutine, first push PC+1 into the stack, then download the immediate address into the PC.
description cycle	2

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CLRF	Clear
Instruction Format	CLRF f 0<=f<=FFh 7 7
	(f)<-0
Operation	with
flag bit	Clear the contents of f to zero
	1
description cycle example	Before the instruction is executed
CLRF WORK	WORK=5Ah
	After the instruction is executed
	WORK=00h

*Note. When the CLRF status register is set, the flag bit Z will not be set to 1

13

CLRWD	Clear watchdog timer
Instruction Format	CLRWD 14
	Watchdog counter cleared
Operation	none
flag bit	Clear watchdog timer
	1
description cycle example	After the instruction is executed
CLRWD	WDT=0

14

COMF	f negation
instruction format	COMF f,d 0<=f<=FFh d=0,1 7 7
	(destination address)<—NOT(f)
Operation	with
Flag Description	Invert the contents of f. When d is 0, the result is saved in the working register. When d is 1, the result is stored in f.
Cycle	1
Example COMF f, 0	Before the instruction is executed W=88h & f=23h After the instruction is executed W=DCh & f=23h
Example 2 COMF f, 1	Before the instruction is executed W=88h & f=23h After the instruction is executed W=88h & f=DCh

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Apparently	Decimal adjust W register value
Instruction Format	Apparently 14
	Decimal adjust W register value
Operation	C,DC
Flag Description	Usually used with addition. If the value of the lower nibble is greater than 9 or DC is 1, add 6 to the lower nibble; If the value of the upper nibble is greater than 9 or C is 1, add 6 to the upper nibble.
Cycle	1
Example	Before DAW commands are executed If W=25h; ADDLW 39h Apparently
	W=25+39 =64=ÿ5EH+6ÿ After the instruction is executed W=64H

16

DEC F	f minus 1
Instruction Format	DEC F fyd 0<=f<=FFh d=0,1 7 7
	(destination address)<—(f)-1
Operation	With
Flag Description	The content of F is reduced by 1 When d is 0, the result is saved in the working register When d is 1, the result is stored in f.
Cycle	1
Example	Before the instruction is executed DEC F fÿ0 W=88h f=23h After the instruction is executed W=22h f=23h
Example 2	Before the instruction is executed DEC F f, 1 W=88h f=23h After the instruction is executed W=88h f=22h

17

DECFSZ	f decrements by 1 and jumps if it is 0
instruction format	DECFSZ fyd 0<=f<=FFh d=0,1 7 7
	(destination address)<—(f)-1, if the result is 0, jump
Operation	none
Flag Description	Decrement the contents of f by 1. If d is 0, the result is stored in the working register. If d is 1, the result is stored in f If the result is 0, the next instruction that has been fetched will be discarded and a NOP instruction group will be inserted. into a two-cycle instruction.

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Cycle	If there is no jump, it takes 1 instruction cycle, otherwise it takes 2 instruction cycles
Example	Before the instruction is executed PC=address(Node)
Node DECFSZ FLAG	After the instruction is executed (FLAG)=(FLAG)-1
OP1:	If(FLAG)=0
OP2:	PC=address(OP2)
	If(FLAG)!=0
	PC=address(OP1)

18

GOTO	Unconditional jump
instruction format	GOTO K 0<=K<=7FFh 3 13
	PC<—K
Operation	none
flag bit	Load address to PC immediately
description cycle	2

19

HALT	Stop the CPU clock
instruction format	HALT 14
	CPU Stop
Operation	none
flag bit	The CPU clock stops, the crystal oscillator still works, and the CPU can be restarted through internal or external interrupts.
description cycle	1

20

INCF	f plus 1
instruction format	INCF fyd 0<=f<=FFh d=0,1 7
	7 (destination address)<—(f)+1
Operation	with
Flag Description	f plus 1 If d is 0, the result is stored in the working register. If d is 1, the result is stored in f.
Cycle	1
Example	Before the instruction is executed W=88h f=23h
INCF f	After the instruction is executed W=24h f=23h
Example 2	Before the instruction is executed

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INCFSZ	W=88h f=23h After the instruction is executed W=88h f=24h
--------	---

21

INCFSZ	Add 1 to f, if the result is 0 jump
instruction format	INCFSZ fyd 0<=f<=FFh d=0,1 7 7
	(destination address)<—(f)+1 If the result is 0, jump
Operation	none
Flag Description	The contents of f are incremented by 1. If d is 0, the result is stored in the working register. If d is 1, the result is stored in f If the result is 0, the next instruction that has been fetched will be discarded and a NOP instruction will be inserted. This constitutes a two-cycle instruction.
Cycle	If there is no jump, it takes 1 instruction cycle, otherwise it takes 2 instruction cycles
Example	Before the instruction is executed PC=address(Node)
Node INCFSZ FLAGj1	After the instruction is executed (FLAG)=(FLAG)+1
OP1:	If(FLAG)=0
OP2:	PC=address(OP2) If(FLAG)!=0 PC=address(OP1)

22

IORLW	Working register and immediate value or
instruction format	IORLW K 0<=K<=FFh 7 7
	(W)<—(W) K
Operation	wth
flag bit	The immediate value is ORed with the contents of the working register. The result is stored in the working register.
	1
description cycle example	Before the instruction is executed
IORLW 85H	W=69h
	After the instruction is executed
	W=EDh

23

IORWF	f and the working register or
instruction format	IORWF fyd 0<=f<=FFh d=0,1 7 7
	(destination address)<—(W) (f)
Operation flag	wth

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describe	f and working register or When d is 0, the result is saved in the working register When d is 1, the result is saved in f
Cycle	1
Example IORWF f,1	Before the instruction is executed W=88h f=23h After the instruction is executed W=88h f=ABh

24

MOVFW	Transfer to working register
instruction format	MOVFW f 0<=f<=FFh 7 7
	(W)<—(f)
Operation	none
flag bit	Transfer data from f to working register
	1
description cycle example MOVFW f	Before the instruction is executed W=88h f=23h After the instruction is executed W=23h f=23h

25

MOVLW	Move immediate data into working register
instruction format	MOVLW K 0<=K<=FFh 6 8
	(W)<—K
Operation	none
flag bit	Transfer the 8-bit immediate value to the working register
	1
description cycle example MOVLW 23H	Before the instruction is executed W=88h After the instruction is executed W=23h

26

MOVP	Read table area data
instruction format	MOVP 14
	Read MTP data into EDATH/WORK
Operation	none
flag bit	Read the data in the table lookup area at address EADRH/EADRL into EDATH/WORK
	2
description cycle example	Before the instruction is executed

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MOVW	EADRH=04h EADRL=00h The address of the table lookup area is 0400h, data bit 1234h After the instruction is executed EDATH=12h, W=34h
------	---

27

MOVWF	Transfer the value of the working register to f
Instruction Format	MOVWF f 0<=f<=FFh 7 7 (f)<—(W)
Operation	none
flag bit	Transfer the value of the working register to f 1
description cycle example MOVWF f	Before the instruction is executed W=88h f=23h After the instruction is executed W=88h f=88h

28

NOP	No Action
Instruction Format	NOP 14
	No Action
Operation	none
flag bit	No Action
description cycle	1

29

PUSH	Push the work and status registers onto the stack for protection
Instruction Format	PUSH 14
	(top stack)<—work/status
Operation	none
Flag Description	Push the values of work and status registers onto the stack, supporting 8-level stacks, which is different from the PC stack. The status register does not include LVD36, LVD24, PD and TO.
cycle	2

30

POP	Pop the work and status registers off the stack
Instruction Format	POP 14
operate	(Top Stack)=>work/status

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	Pop Stack
Flag	none
Description	The current value on the stack is processed, and the work and status registers are updated respectively. 8-level stack is supported. The stack is different from the PC stack; the status registers do not include LVD36, LVD24, PD and TO.
cycle	2

31

RETFIE	Returning from an interrupt
Instruction Format	RETFIE 14
operate	(Top Stack)=>PC Pop Stack 1=>GIE
Flag bit	none
	The PC is obtained from the top of the stack, then popped, and the global interrupt enable bit is set to 1.
description cycle	2

32

RETLW	Return and send the immediate value to the working register
instruction format	RETLW K 0<=K<=FFh 6 8
operate	(W)<--K (Top Stack)=>PC Pop Stack
Flag bit	none
	The 8-bit immediate value is sent to the working register, the PC value is obtained from the top of the stack, and then popped
description cycle	2

33

RETURN	Return from a subroutine
Instruction Format	RETURN 14
operate	(Top Stack)=>PC Pop Stack
Flag bit	none
	The PC value is obtained from the top of the stack and then popped
description cycle	2

34

RLF	Shift left with carry
instruction format	RLF fyd 0<=f<=FFh d=0,1 7 7

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operate	(target address [n+1]) <— (f[n]) (target address[0])<—C C<—(f[7])
Flag	C \ddot{y} Z
Description	F Shift left one position with carry If d is 0, the result is stored in the working register If d is 1, the result is stored in f
Cycle	1
Example	Before the instruction is executed RLF f, 1 C=0 W=88h f=E6h After instruction execution C=1 W=88h f=CCh

35

RRF	Shift right with carry
Instruction Format	RRF f \ddot{y} d 0<=f<=FFh d=0,1 7 7
operate	(target address [n-1]) <— (f[n]) (target address[7])<—C C<—(f[0])
Flag	C
Description	F Shift right one position with carry If d is 0, the result is stored in the working register If d is 1, the result is stored in f
Cycle	1
Example	Before the instruction is executed RRF f \ddot{y} 0 C=0 W=88h f=95h After instruction execution C=1 W=4Ah f=95h

36

SLEEP	Crystal oscillator stopped
instruction format	SLEEP 14
	CPU crystal oscillator stopped
Operation	PD
flag bit	CPU crystal oscillator stops. CPU restarts via external interrupt source
description cycle	1

37

SUBLW	Immediately decrement the value of the working register
instruction format	SUBLW K 0<=K<=FFh 6 8
operate	(W)<—K-(W)

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Flag bit	C, DC, Z
	The 8-bit immediate value is subtracted from the value of the working register, and the result is saved in the working register
	1
description cycle example SUBLW 02H	Before the instruction is executed W=01h After the instruction is executed W=01h C=1 (represents no borrow) Z=0 (represents non-zero result)
Example 2 SUBLW 02H	Before the instruction is executed W=02h After the instruction is executed W=00h C=1 (represents no borrow) Z=1 (represents the result is zero)
Example 2 SUBLW 02H	Before the instruction is executed W=03h After the instruction is executed W=FFh C=0 (indicates borrow) Z=0 (indicates result is not zero)

38

SUBWF	The value of f minus the value of the working register
instruction format	SUBWF f ₇ d ₇ 0<=f<=FFh d=0,1
	7 7
	(target address)<—(f)-(W)
Operation	C, DC, Z
Flag Description	The value of f minus the value of the working register. If d is 0, the result is stored in the working register If d is 1, the result is stored in f
Cycle	1
Example SUBWF f ₇ 1	Before the instruction is executed f=33h W=01h After the instruction is executed f=32h C=1 Z=0
Example 2 SUBWF f ₇ 1	Before the instruction is executed f=01h W=01h After the instruction is executed f=00h C=1 Z=1
Example 3 SUBWF f ₇ 1	Before the instruction is executed f=04h W=05h After the instruction is executed f=FFh C=0 Z=0

39

SUBWFC	Subtraction with borrow
instruction format	SUBWFC f ₇ d ₇ 0<=f<=FFh d=0,1
	7
	7 (target address)<—(f)-(W)-1+C
Operation flag	C, DC, Z

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describe	The value of f minus the value of the working register If d is 0, the result is stored in the working register If d is 1, the result is stored in f
Cycle	1
Example SUBWFC f,j1	Before the instruction is executed W=01h f=33h C=1 After the instruction is executed f=32h C=1 Z=0
Example 2 SUBWFC f,j1	Before the instruction is executed W=01h f=02h C=0 After the instruction is executed f=00h C=1 Z=1
Example 3 SUBWFC f,j1	Before the instruction is executed W=05h f=04h C=0 After the instruction is executed f=FEh C=0 Z=0

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SWAPF	Swap register values
instruction format	SWAPF f,jd 0<=f<=FFh d=0,1 7 7
operate	(des[3:0])<-f[7:4] (des[7:4])<-f[3:0]
Flag	none
Description	Put the high 4 bits of data of f register into the low 4 bits of the target register; Put the low-order data of the f register into the high 4 bits of the target register When d is 1, register f is the destination register; otherwise, register w is the destination register
Cycle	1
Example SWAPF f,1	Before the instruction is executed f=ACh After the instruction is executed f=CAh

41

TBLP	Write Memory
instruction format	TBLP k (k is 0) 8 8
	Write Memory
Operation	none
flag bit	Write the data of EDATH/WORK to the memory address EADRH/EADRL
	About 700us time
description cycle example TBLP 0	Before the instruction is executed EDATH=BAh, W=ACh, EADRH=04h, EADRL=00h After the instruction is executed Write BAACh to memory address 0400h

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FREE	The value of the working register is XORed with the immediate value
Instruction Format	XORLW K 0<=K<=FFh 6 8
Operation	(W)<—(W)^K
flag bit	WTFH
	The 8-bit immediate value is XORed with the value of the working register, and the result is stored in the working register
	1
description cycle example XORLW 5Fh	Before the instruction is executed W=ACh After the instruction is executed W=F3h

43

XORWF	The value of f is XORed with the value of the working register
Instruction Format	XORWF fyd 0<=f<=FFh d=0,1 7 7
Operation	(target address)<—(W)^f
Flag	WTFH
Description	The value of F is XORed with the value of the working register. When d is 0, the result is saved in the working register When d is 1, the result is saved in f
Cycle	1
Example XORWF f1	Before the instruction is executed W=ACh f=5Fh After the instruction is executed f=F3h

5 Typical Applications

5.1 Electronic Cigarettes

CSU32M10/CSU32M11 has an internal integrated analog comparator, which can be used to trigger the shutdown of PWM output and make the electronic cigarette load short circuit.

The protection time is usually 5~20us (related to the filter time of the comparator configuration). When using this module, please pay attention to the following issues:

A 1~2 Ω resistor should be connected in series between the VDD and power supply voltage input terminals . A filter capacitor of 2.2uF or more is recommended.

When the short circuit protection is on, it will cause the chip VDD voltage to oscillate, resulting in unstable chip operation and a longer short circuit protection response time. The reference circuit is shown in the figure below.

As shown:

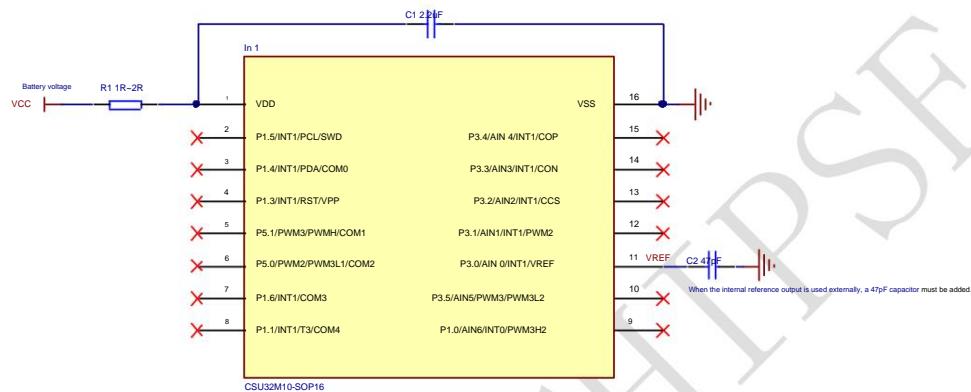


Figure 5-1

6 Electrical characteristics

6.1 Limit values

Table 6-1

	scope	unit
Parameter	-0.3~6.0	In
Power Supply VDD Pin	-0.3~VDD+0.3	In
Input Voltage	-40~85	°C
Operating	-55~150	°C
Temperature Storage	220°C, 10 seconds	

Temperature Soldering Temperature, Time Note: Voltage or temperature exceeding the values listed in the table above may cause permanent damage to the device. These listed values are voltage ratings only.

Functional operation of the device under these and any other conditions beyond those specified in the recommended operating conditions is not implied.

Stresses to maximum rated conditions may affect device reliability.

6.2 DC Characteristics (VDD = 5V, TA = 25°C, unless otherwise specified)

Table 6-2

symbol	parameter	Test conditions:	Min	Typ	Max	Unit		
VDD	Operating voltage	25°C	2.2		5	5.5	In	
		-40°C~85°C	2.35		5	5.5	In	
Tcpu	instruction cycle	VDD: 2.2V~5.5V Digital	250				ns	
HIV1 (VTHSEL=0)	input high Level	PT1, PT3, PT5	0.75VDD				In	
VIL1 (VTHSEL=0)	digital input low Level	PT1, PT3, PT5				0.3VDD	In	
HIV2 (VTHSEL=1)	digital input high Level	PT1, PT3, PT5 (PT1.3 is used as reset port) except)			0.45VDD		In	
VIL2 (VTHSEL=1)	Digital Input Low Level	PT1, PT3, PT5 (PT1.3 is reset (Excluding mouth))			0.45VDD		In	
RPU/RPD	Pull-up/pull-down Resistance	PT1,PT3,PT5 \ddot{y}			32		K \ddot{y}	
	Pull-down resistor PT1.3, VDD=5V Pull-down				400		K \ddot{y}	
	resistor PT3.4, PT5.1, VDD=5V Pull-down resistor PT1.0,				10		K \ddot{y}	
	VDD=5V				3		K \ddot{y}	
IOH	High level output Current (PT1.3 (Excluding mouth))	VOH=0.9VDD \ddot{y} VDD=5V			17		m.a.	
		VOH=0.9VDD \ddot{y} VDD=5V PT5.0 and PT5.1 (PWMIS=1)			21		m.a.	
		VOH=0.9VDD \ddot{y} VDD=3V			7		m.a.	
IOL	Low level output Current	VOL=0.1VDD \ddot{y} VDD=5V			21		m.a.	
		VOL=0.1VDD \ddot{y} VDD=5V PT5.0 and PT5.1 (PWMIS=1)			46		m.a.	
		VOL=0.1VDD \ddot{y} VDD=5V PT1.0 and PT3.5 (DRIVE_CFG=1)			29		m.a.	
		VOL=0.1VDD \ddot{y} VDD=3V			10		m.a.	

LVD	Reset voltage/low Voltage detection circuit Pressure	2.0V power-on/power-off reset point; 25 °C		2.0		In
		2.0V power-on/power-off reset point; -40~85 °C	1.6	2.0	2.2	
		2.4V power-on/power-off reset point; 25 °C	2.2	2.4	2.8	
		2.4V power-on/power-off reset point; -40~85 °C	2.0	2.4	3.0	
		3.6V power-on/power-off reset point; 25 °C	3.3	3.6	3.9	
		3.6V power-on/power-off reset point; -40~85 °C	3.0	3.6	4.2	
IRC	Built-in 16MHz	25~5V	15.84	16.0	16.16	MHz
	RC Clock	-40~85, 2.35V~5.5V 25~	15.52	16.0	16.48	
	Built-in 32MHz	5V	31.68	32.0	32.32	MHz
	RC Clock	-40~85, 2.35V~5.5V 25~	31.04	32.0	32.96	
WDT	Built-in 8MHz	5V	7.92	8.0	8.08	MHz
	RC Clock	-40~85, 2.35V~5.5V 25~	7.76	8.0	8.24	
TINT0/1	Built-in watchdog clock	5V	29	32	35	KHz
		-40~85, 2.35V~5.5V	26	32	38	KHz
TINT0/1	Interrupt trigger pulse Width	25~5V	Tcpu			ns
IDD1	sleep mode Current	VDD=3V, turn off WDT		0.5		a
		VDD=3V, turn on WDT		2.5		a
		VDD=5V, turn off WDT		0.8		a
		VDD=5V, turn on WDT		3.5		a
IDD2	Working current	internal crystal mode, F=16MHz VDD=3V, fcpu=fosc/4 internal		1.2		m.a.
		crystal oscillator mode, F=16MHz VDD=3V, fcpu=fosc/8 internal		0.9		
		crystal oscillator mode, F=16MHz VDD=3V, fcpu=fosc/16 internal		0.75		
		crystal oscillator mode, F=16MHz VDD=3V, fcpu=fosc/32 internal		0.7		
		crystal oscillator mode, F=16MHz VDD=5V, fcpu=fosc/4 internal		2.5		
		crystal oscillator mode, F=16MHz VDD=5V, fcpu=fosc/8 internal		1.5		
		crystal oscillator mode, F=16MHz VDD=5V, fcpu=fosc/16 internal		1.2		
		crystal oscillator mode, F=16MHz VDD=5V, fcpu=fosc/32		1.0		

6.3 ADC Characteristics (VDD = 5V, TA = 25°C, unless otherwise specified)

Table 6-3

symbol	Parameter test conditions		Min	Typ	Max	Unit		
VDD	ADC working voltage Pressure Range	25 °C	2.6		5	5.5	In	
		-40°C ~+85°C		2.7	5	5.5	In	
AIN0~AIN5 analog input range VREF is controlled by register VREFS[1:0]			0			VREF	In	

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input voltage	Wai					
Vref input range	External reference Pressure input range	VREFS[1:0]=01	0		VDD	In
ADC current consumption	ADC Power Consumption	VDD=5V (VDD is used as reference voltage)		0.6		m.a.
		VDD=3V (VDD is used as reference voltage)		0.5		m.a.
RADC	Sampling switch <small>Resistance</small>	VDD=5V		4.5		k Ω
CADC	Internal sampling circuit <small>Allow</small>				17.5	pF
RAIN	External input resistance anti-				10	k Ω
fADC	ADC clock frequency Rate	SRADCCKS[1:0] control	0.5	2	4	MHz
TS	Sampling time	3V \leq VDD \leq 5.5V \leq RAIN \leq 10 k Ω 2.8V \leq VDD $<$ 3V	4			μ s
		RAIN \leq 10 k Ω 2.6V \leq VDD $<$ 2.8V \leq RAIN \leq 10	8			μ s
		k Ω	16			μ s
ADC Conversion Cycle Time	ADC conversion cycle <small>Expect</small>	Including sampling time TS and successive approximation time 12xfADC	3.5	10	464	μ s
fs	ADC sampling rate		2.15	100	285	kHz
INL	Integral Nonlinearity	fADC =2MHz \leq TS =4 μ s 4V \leq VDD \leq 5.5V \leq RAIN \leq 10 k Ω T \leq -40 °C ~+85 °C IVREF= 3V		\pm 4		LSB
		fADC =2MHz \leq TS =4 μ s 2.8V \leq VDD \leq 5.5V \leq RAIN \leq 10 k Ω T \leq -40 °C ~+85 °C IVREF=1.4V or 2V		\pm 4		LSB
		fADC =2MHz \leq TS =16 μ s 2.6V \leq VDD $<$ 2.8V \leq RAIN \leq 10 k Ω T \leq 25 °C IVREF=1.4V		\pm 4		LSB
Gain error		fADC =2MHz \leq TS =4 μ s 4V \leq VDD \leq 5.5V \leq RAIN \leq 10 k Ω T \leq -40 °C ~+85 °C IVREF=1.4V or 2V or 3V		\pm 3		LSB
		fADC =2MHz \leq TS =4 μ s 3.3V \leq VDD \leq 5.5V \leq RAIN \leq 10 k Ω T \leq -40 °C ~+85 °C IVREF=1.4V or 2V		\pm 3		LSB
		fADC =2MHz \leq TS =8 μ s 2.8V \leq VDD $<$ 3.3V \leq RAIN \leq 10 k Ω T \leq -40 °C ~+85 °C IVREF=1.4V		\pm 3		LSB
		fADC =2MHz \leq TS =16 μ s 2.6V \leq VDD $<$ 2.8V \leq RAIN \leq 10 k Ω T \leq 25 °C		\pm 3		LSB

		IVREF=1.4V				
No missing code	No missing codes Pressure	VREFS[1:0]=01, external reference voltage		9		Bits
		VREFS[1:0]=00, VDD is used as reference voltage		9		Bits
		VREFS[1:0]=10, internal reference voltage		9		Bits
IVREF	Internal reference Pressure	REF_SEL[2:0]=0XX or 100, 2.7V~VDD~5.5V~40 °C ~+85 °C	-1.5%	1.4	+1.5%	In
		REF_SEL [2:0]=101 3.25V~VDD~5.5V~40 °C ~+85 °C	-1.5%	2.0	+1.5%	In
		REF_SEL [2:0]=110 4V~VDD~5.5V~40 °C ~+85 °C	-1%	3.0	+1%	In
		REF_SEL [2:0]=111 4.25V~VDD~5.5V~40 °C ~+85 °C	-1%	4.0	+1%	In
IVREF temp drift	Internal reference Voltage temperature drift			50		ppm
Offset	ADC offset Pressure				3	mV

6.4 Analog Comparator Characteristics

symbol		Min. Typ. Max	Unit Test Conditions	-40 °C ~+85 °C		
VCMP	Parameters	2.4	5	5.5	In	
FACING	Operating	-40	25	85	°C	
COME	voltage Temperature Input	2.0		AVDD	In	
VOUT	voltage range Output	0		AVDD	In	
Icomp	voltage range Operating current		80		a	AVDD=5V
Comp Answer	Response time		2	4	uS	
CMP LSB minimum resolution offset voltage			1		mV	
Voffset		-1		1	mV	2.4V~5.5V, -40 °C ~+85 °C

6.5 Constant Current High Drive

symbol		Min Typ Max	Unit Test Conditions			
Vdd	Parameters	2.4	5	5.5	In	
FACING	Operating	-40	25	85	°C	
Iout	voltage	49	50	51	m.a.	3.6V~25 °C
Iout	Temperature Output current Output current	47.5	50	52.5	m.a.	2.7V~4.3V~20~+70
Iripple	Output current ripple Electronic cigarette			1	m.a.	
Rload	application tobacco resistance Anti-range	0.5		3	Oh	2.7V~4.3V~20~+70

6.6 MTP and EEPROM read and write characteristics

6.6.1 EEPROM characteristics are as follows

parameter	Test conditions	Min Typ Max	Unit		

Write operation voltage range -40V~85V	Read	2.5	5	5.5	In
operation voltage range -40V~85V		2.35	5	5.5	In
Write operation time	5V, 25V, 3V,		0.7	5	ms
	25V, 2.5V, 25V		0.9	6	ms
	Write operation		1.2	8	ms
current 5V, 25V 5V, 25V 5V, -40V			7	40	mA
Number of write operations		5000			Second-rate
		500			

6.6.2 MTP features are as follows

Parameter test conditions	Write operation voltage	Min	Typ	Max	Unit
range -40V~85V	Read operation voltage range	4.5	5	5.5	In
-40V~85V	Write operation times 5V, 25V	2.35	5	5.5	In
		1000			Second-rate

6.7 32MHz IRC Clock Frequency Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

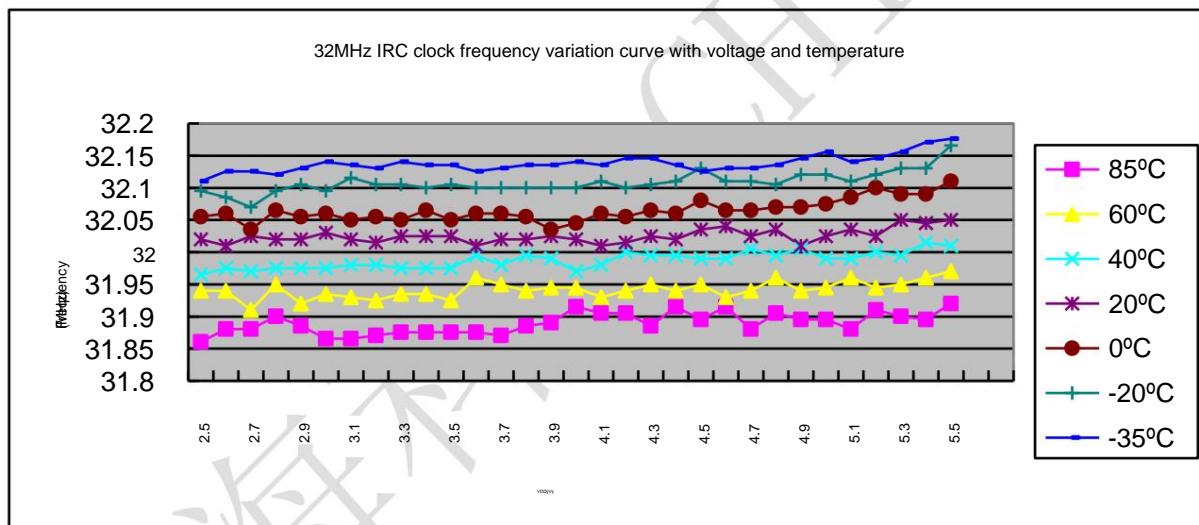


Figure 6-1 Voltage and temperature characteristics of 32MHz RC clock frequency

6.8 16MHz IRC Clock Frequency Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

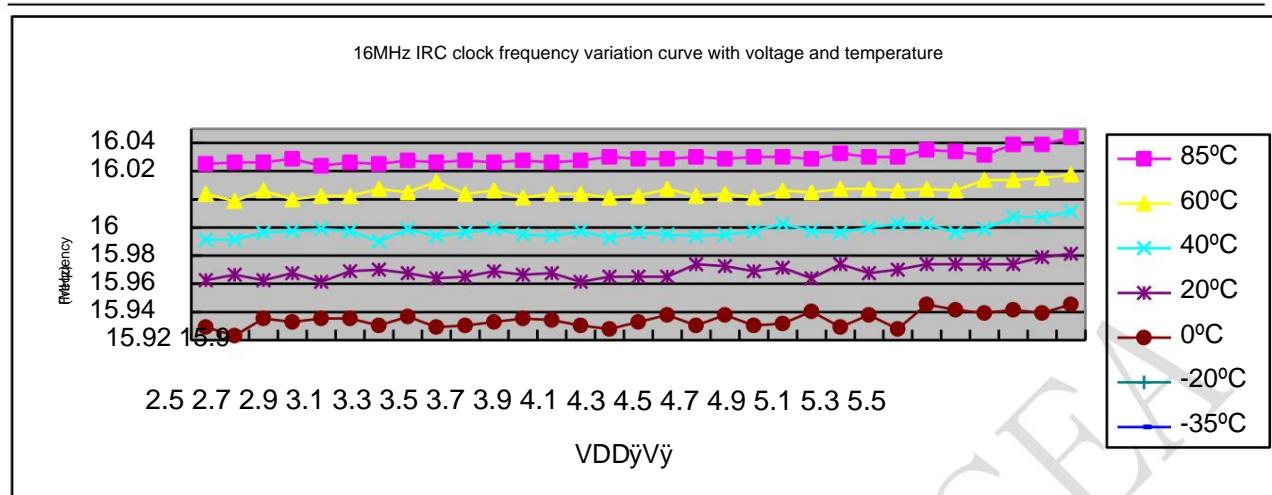


Figure 6-2 Voltage and temperature characteristics of 16MHz RC clock frequency

6.9 8MHz IRC clock frequency characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

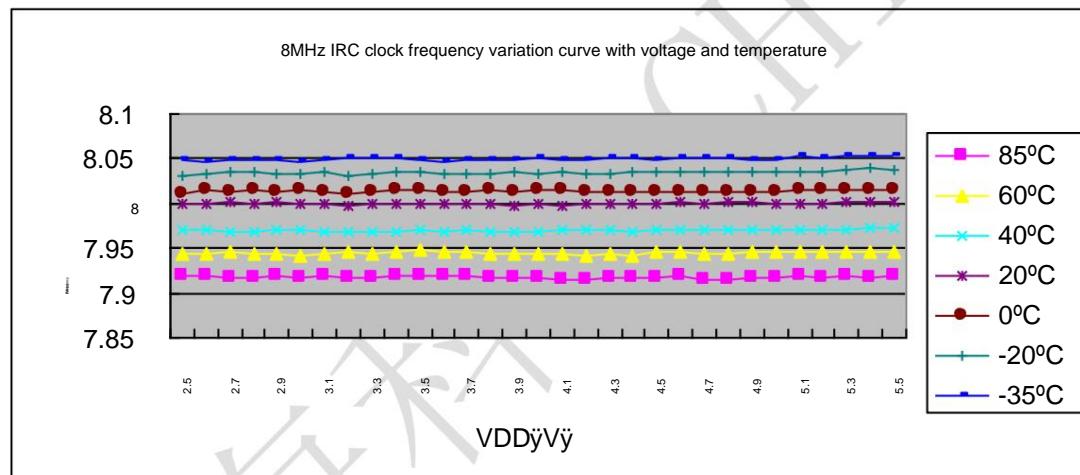


Figure 6-3 Voltage and temperature characteristics of 8MHz RC clock frequency

6.10 WDT Clock Frequency Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

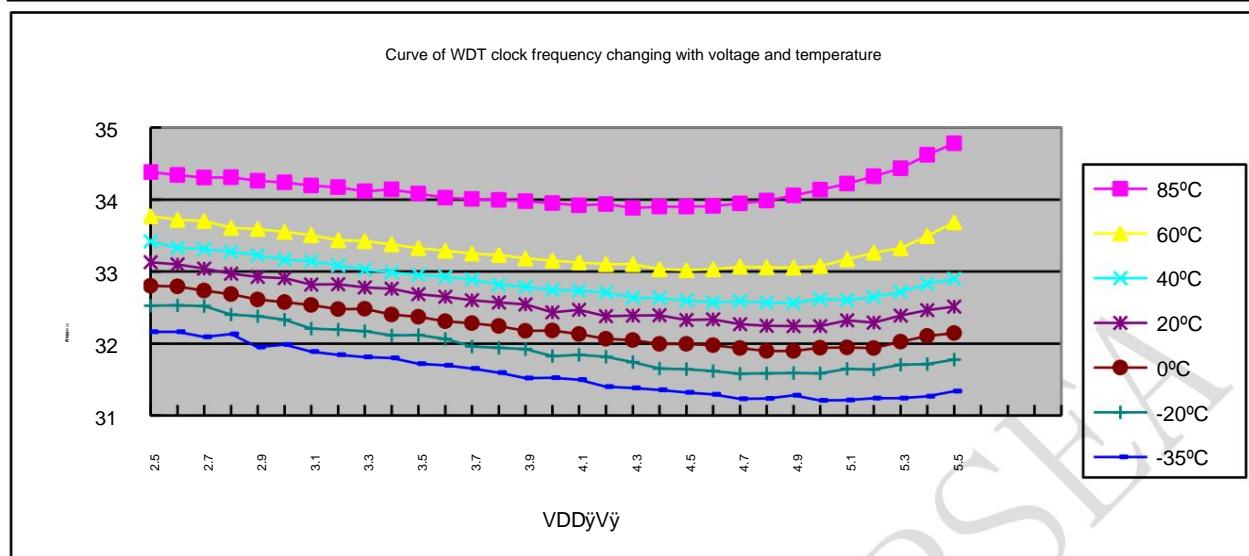


Figure 6-4 Voltage and temperature characteristics of WDT frequency

6.11 2.0V Power-off Reset Temperature Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

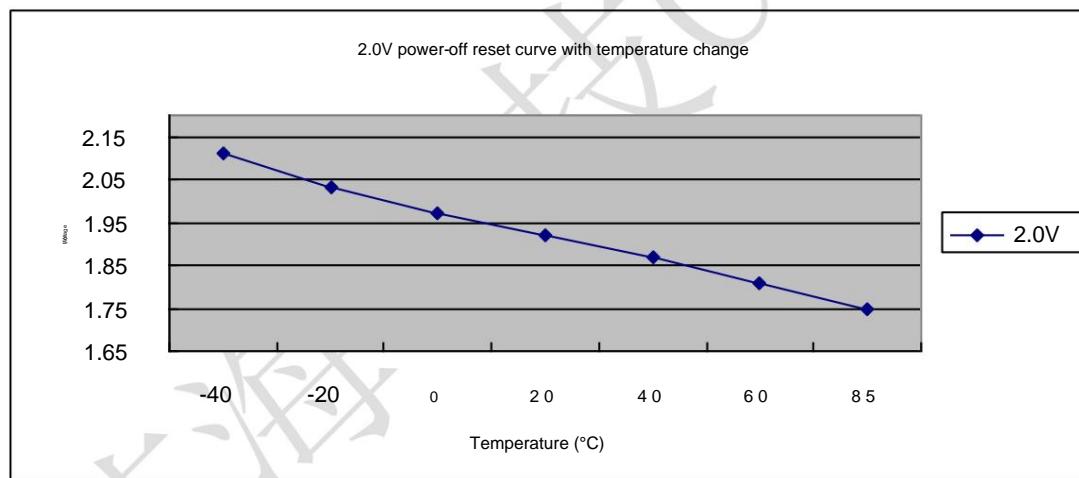


Figure 6-5 2.0V power-off reset temperature characteristics

6.12 2.4V Low Voltage Reset Temperature Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

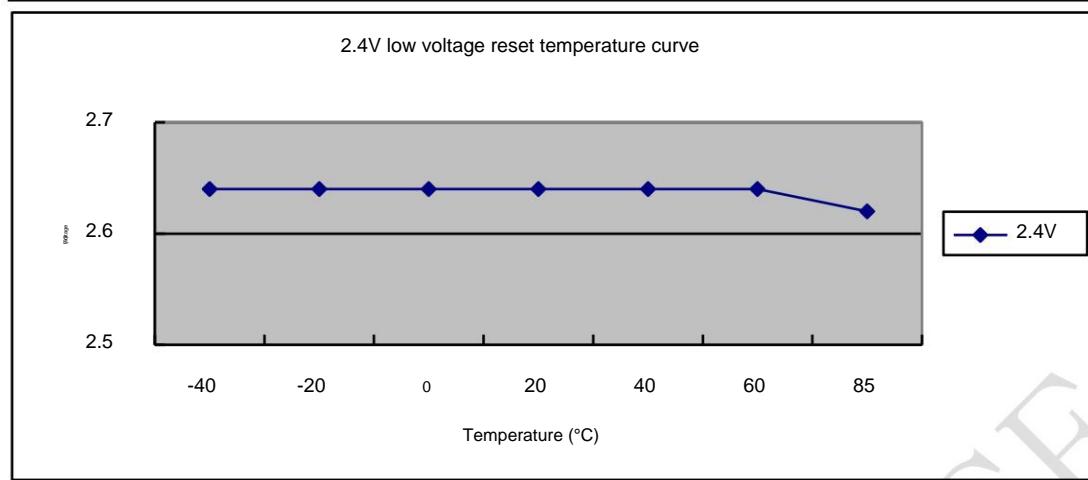


Figure 6-6 2.4V low voltage reset temperature characteristics

6.13 3.6V Low Voltage Reset Temperature Characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

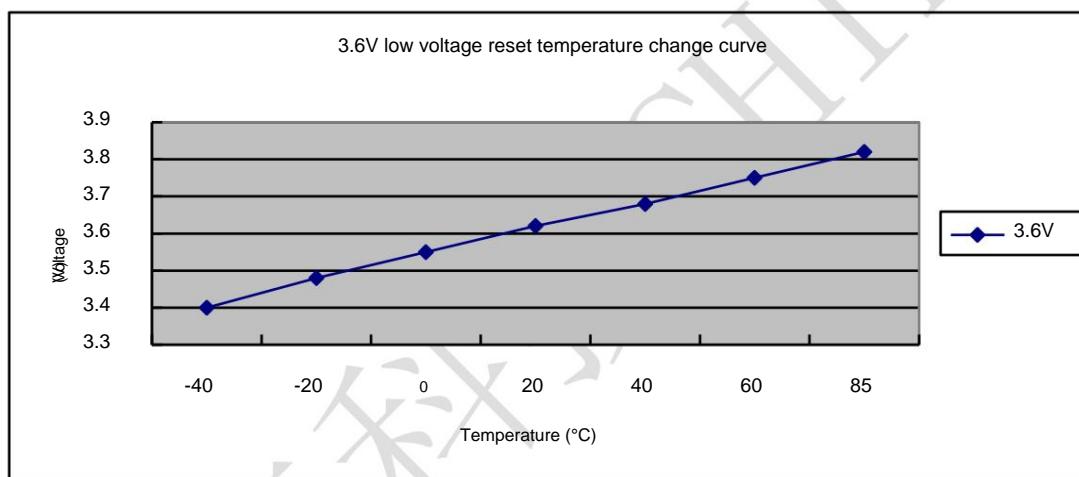


Figure 6-7 3.6V low voltage reset temperature characteristics

6.14 Internal reference voltage 1.4V voltage and temperature characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

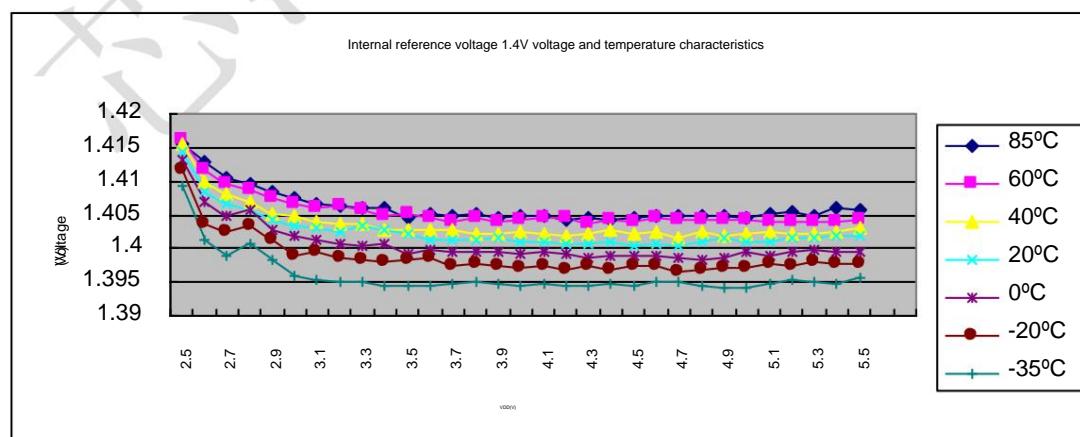


Figure 6-8 Voltage and temperature characteristics of built-in reference voltage 1.4V

6.15 Internal reference voltage 2.0V voltage and temperature characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

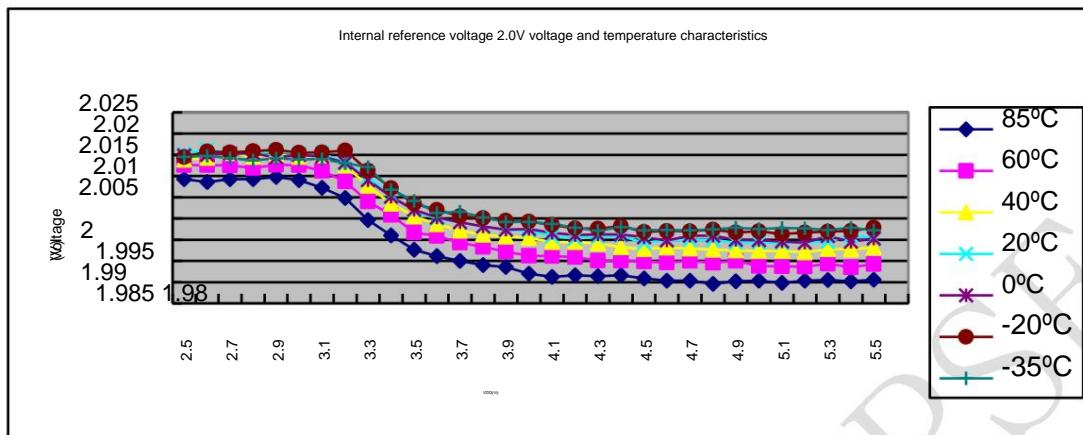


Figure 6-9 Voltage and temperature characteristics of built-in reference voltage 2.0V

6.16 Internal reference voltage 3.0V voltage and temperature characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

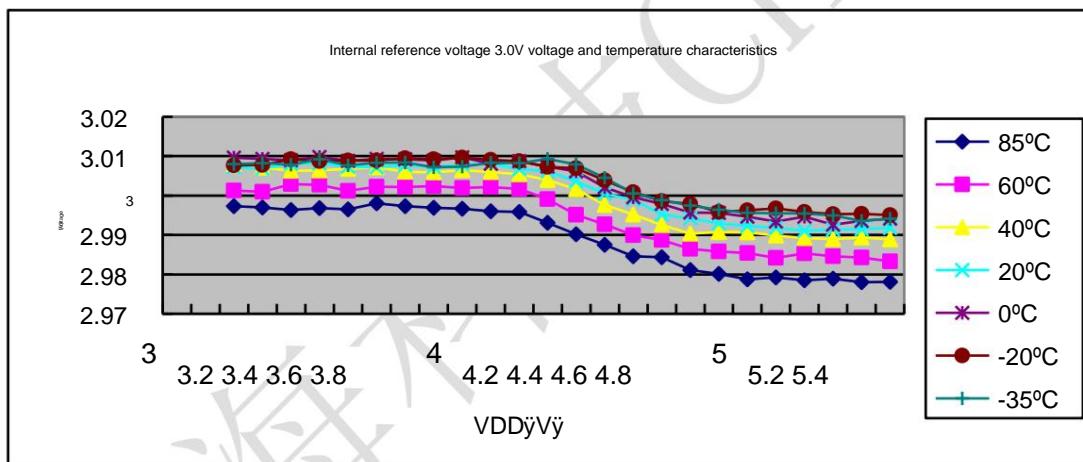


Figure 6-10 Voltage and temperature characteristics of built-in reference voltage 3.0V

6.17 Internal reference voltage 4.0V voltage and temperature characteristics

The figure below shows the test data of the actual chip. Different chips may have slight differences and are for reference only.

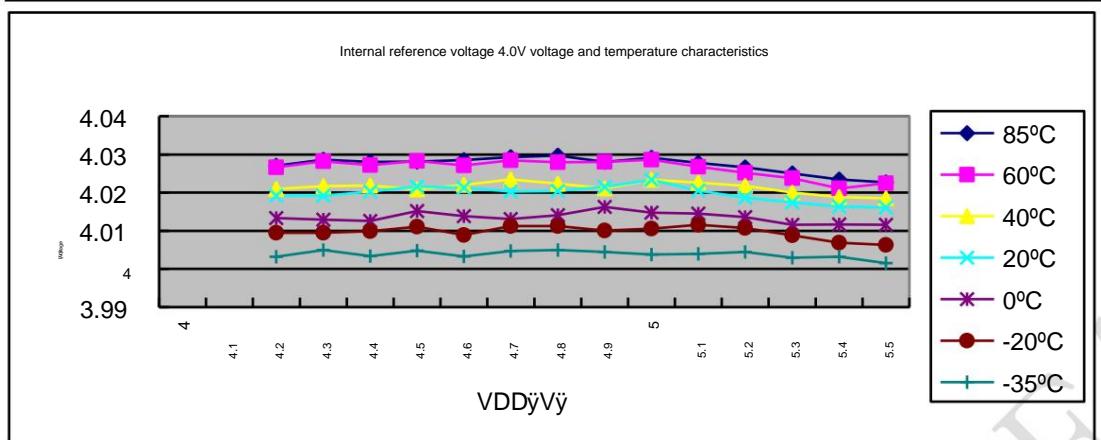


Figure 6-11 Voltage and temperature characteristics of built-in reference voltage 4.0V

6.18 Reliability

6.18.1 ESD characteristics

Symbolic parameters	Test conditions	Level Max	Unit	
VESD(HBM)	HBM model ESD capability at 25 °C, test standard JESD22-A114 VESD(MM)	3A	4000	In
MM model ESD capability at 25 °C, test standard JESD22-A115	The above results are sample	B	200	In

test results, and this test is not performed in mass production.

6.18.2 Latch up

Symbol Parameter	Test conditions	Level Max	Unit	
LU Static Latch up level 25 °C, JEDEC standard N0.78C	The above results are sample	I	600	m.a.

test results, and mass production tests have not been conducted.

7 Package Diagram

7.1 MSOP-10pin

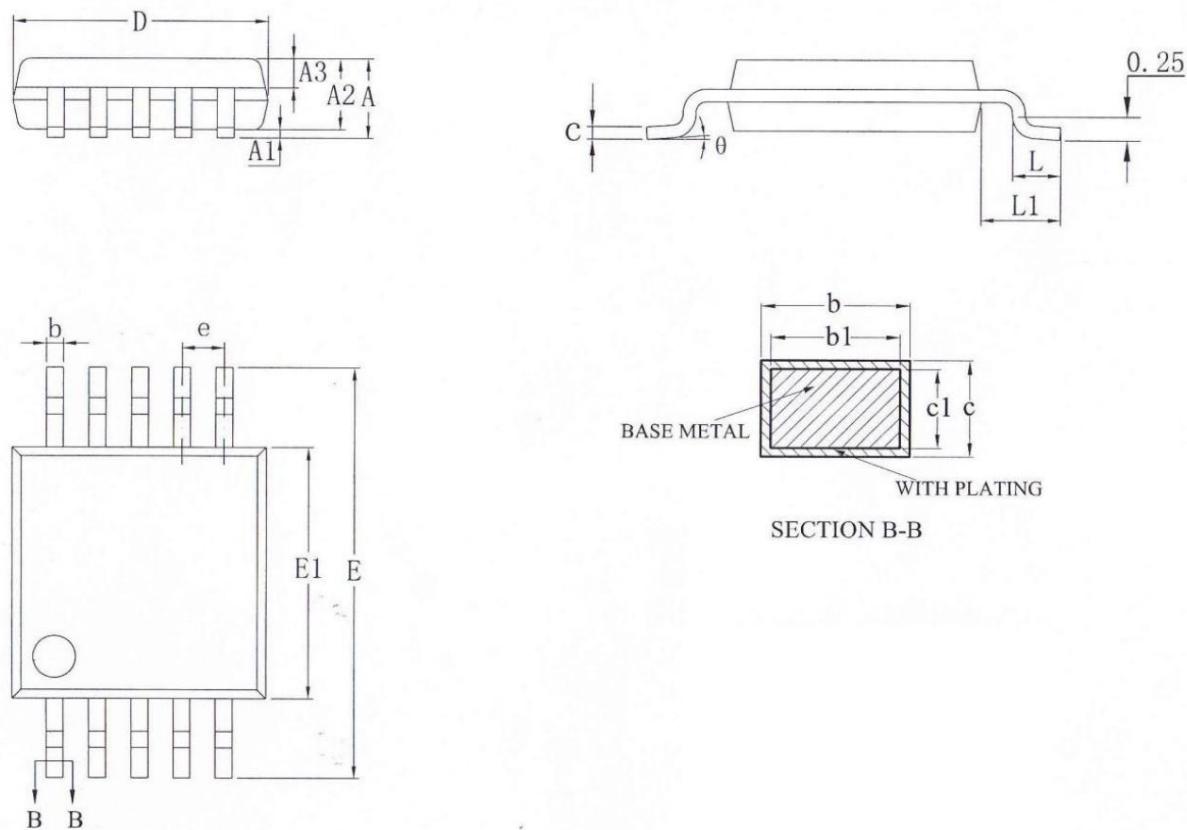


Figure 7-1

Table 7-1

SYMBOLS	MIN	NOR	MAX
(mm)			
A			1.10
A1	0.05		0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18		0.26
b1	0.17	0.20	0.23
c	0.15		0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
and	4.70	4.90	5.10
E1	2.90	3.00	3.10
and	0.50BSC		
L	0.40		0.70
L1	0.95REF		

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Gathering tiny bits of information together to form a vast ocean

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7.2 SOP-16pin

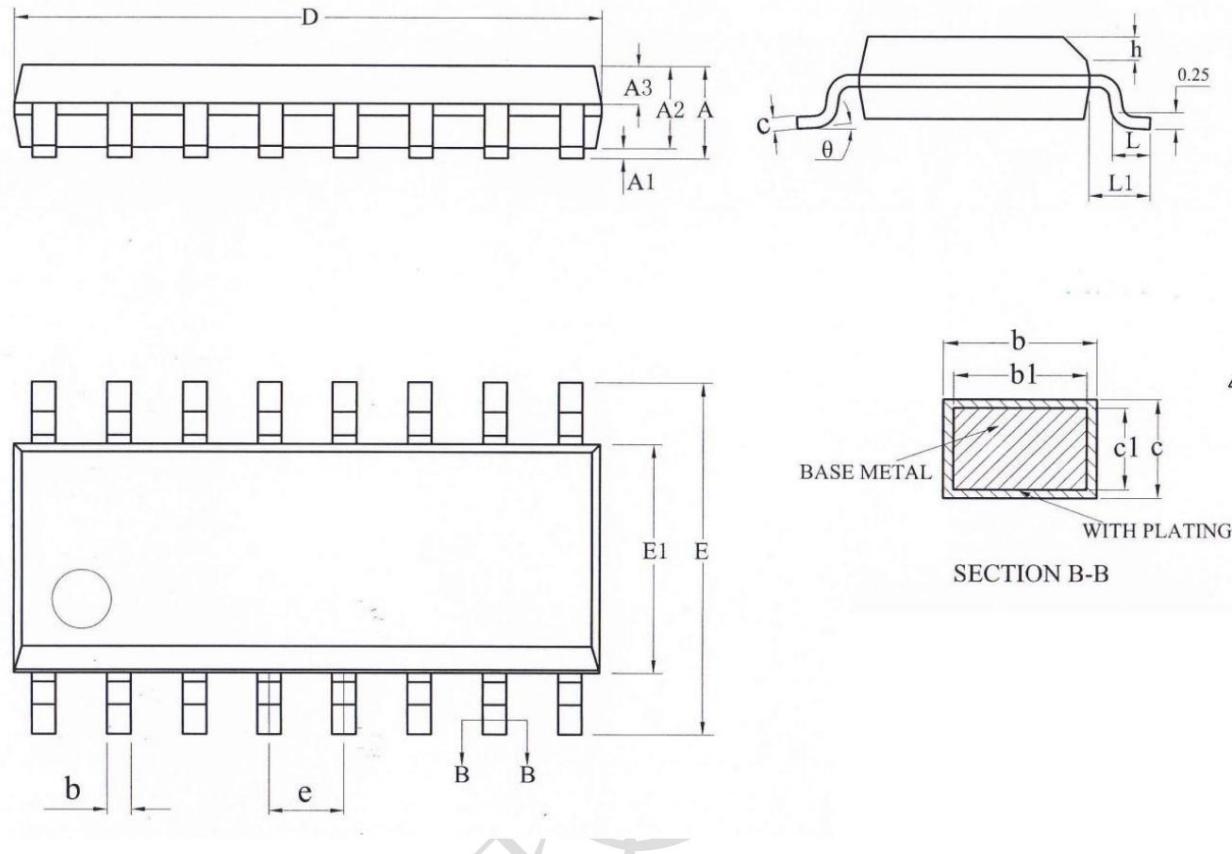


Figure 7-2

Table 7-2

SYMBOLS	MIN	NOR	MAX
	(mm)		
A			1.75
A1	0.10		0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.390		0.470
b1	0.38	0.41	0.44
c	0.20		0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
and	5.80	6.00	6.20
E1	3.80	3.90	4.00
and	1.27BSC		
h	0.25		0.50
L	0.50		0.80
L1	1.05REF		
ÿ°	0°		8°

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7.3 QFN-16pin

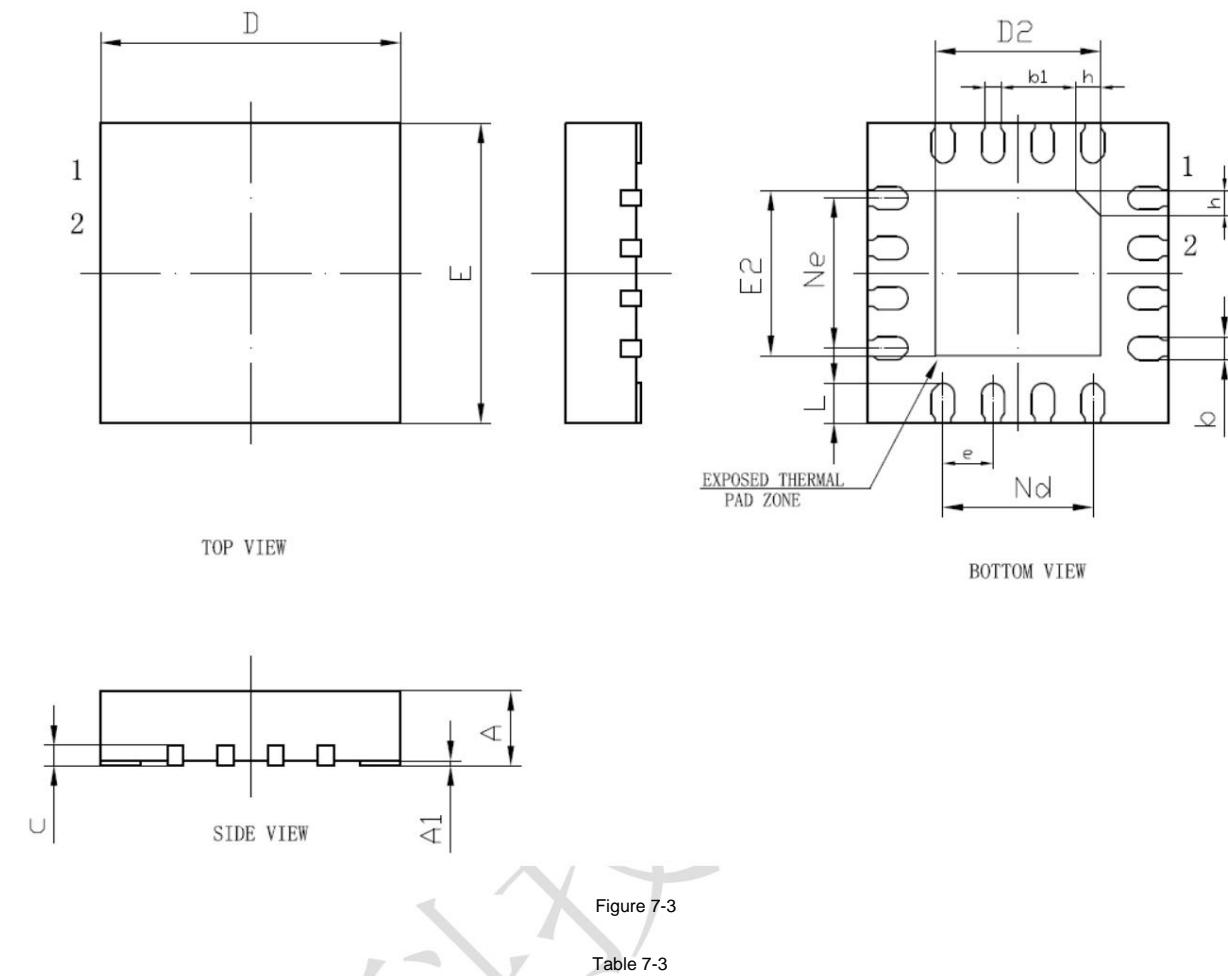


Figure 7-3

Table 7-3

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	0.70	0.75	0.80
A_1	0	0.02	0.05
b	0.18	0.25	0.30
b_1		0.16RFE	
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D_2	1.55	1.65	1.75
and		0.50BSC	
Yes		1.50REF	
N_d		1.50REF	
and	2.90	3.00	3.10
E_2	1.55	1.65	1.75
L	0.35	0.40	0.45
H	0.20	0.25	0.30

8 MCU product naming rules

8.1 Product model description

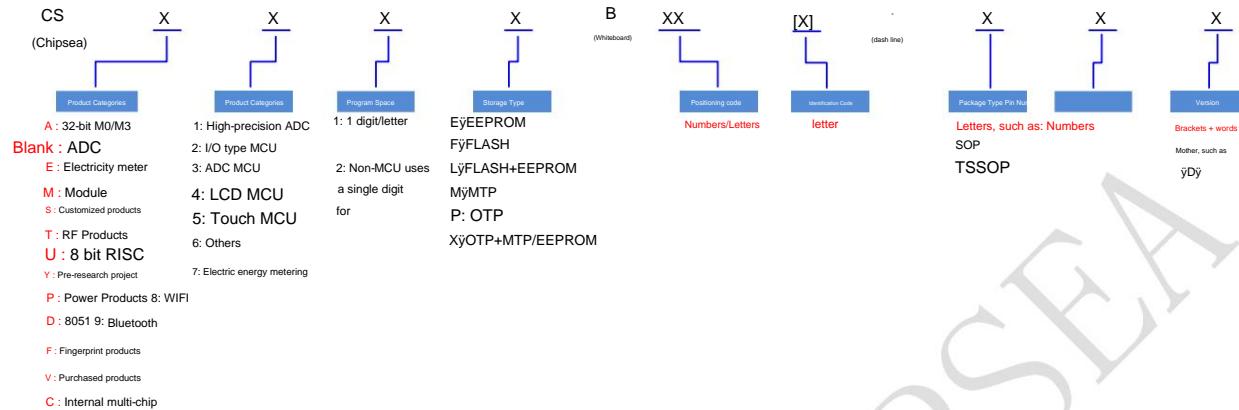


Figure 8-1

Table 8-1 Package abbreviations

Identifier	Package Type
BD	Bonding
FROM	DIP
SD	SDIP
SO	SOP
SS	SSOP
TS	TSSOP
QF	MFF
LQ	LQFP
TQ	TQFP
QN	QFN
MS	MSOP

8.2 Naming Examples

Table 8-2

name	Kernel	ROM kind Type	Functional classification	Product Definition Bit Model	Chip version	Package	Operating temperature range	Packaging materials
CSU32M10-SOP16	8-bit Risc MCU	MTP ADC		20	1st Edition SOP		-40~85 °C	Lead-free package (PB-Free Pack)

8.3 Product Printing Instructions

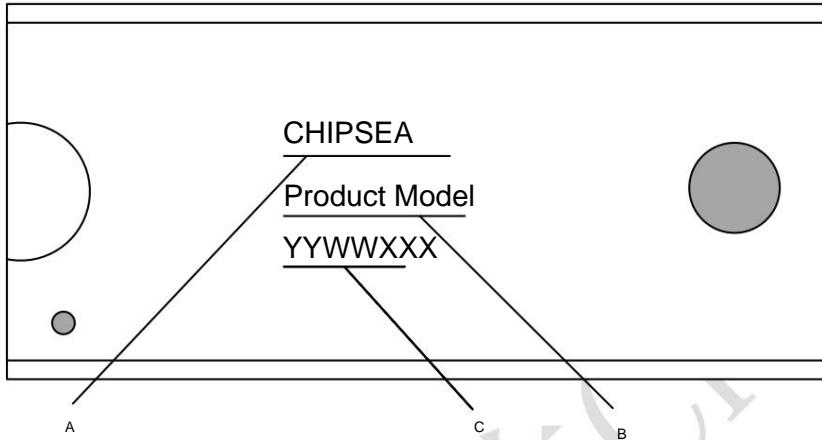


Figure 8-2

There are usually 3 lines of printing on the front of the chip:

The first line is the company name, CHIPSEA.

The second line is the product model. For some small-size packages, the product model will be shortened.

The third line is the date code. Counting from the left, the first two digits are the Gregorian calendar year and the last two digits are the calendar week number of the year.

When the number is two, add 0 on the left; the last three digits are the random product number.

For example, the CSU32M10 is printed as follows:

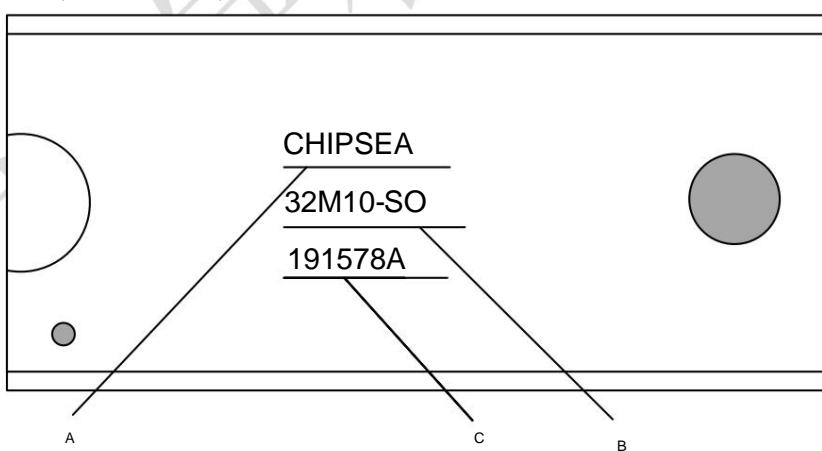


Figure 8-3

9 Ordering information

Table 9-1

Product Model	Encapsulation	Environmentally friendly RoHS	Operating temperature	Package
CSU32M10-MSOP10	MSOP10	Yes	-40 °C ~85 °C Tube	
CSU32M10-SOP16	SOP16	Yes	-40 °C ~85 °C Tube	
CSU32M11-SOP16	SOP16	Yes	-40 °C ~85 °C Tube	
CSU32M10-QFN16	QFN16	Yes	-40 °C ~85 °C Tray packing	

10 Appendix

10.1 How to use CSU32M10 to replace CSU32P20

Step 1: Use IDE_5.4.0 version IDE to open the previous CSU32P20 source program, change the chip model to CSU32M10, and regenerate

For the header file of the corresponding chip, the assembly project replaces the header file with CSU32M10.inc, and the C language project replaces the original program header file with

If the original SysRegDefine.c file is in the root directory of the project, the original file will be automatically copied after the chip model is modified.

SysRegDefine.c file replacement. If the original SysRegDefine.c is in the custom directory, it will be generated in the project root directory after the chip is modified.

New SysRegDefine.c file, which needs to be replaced by the user