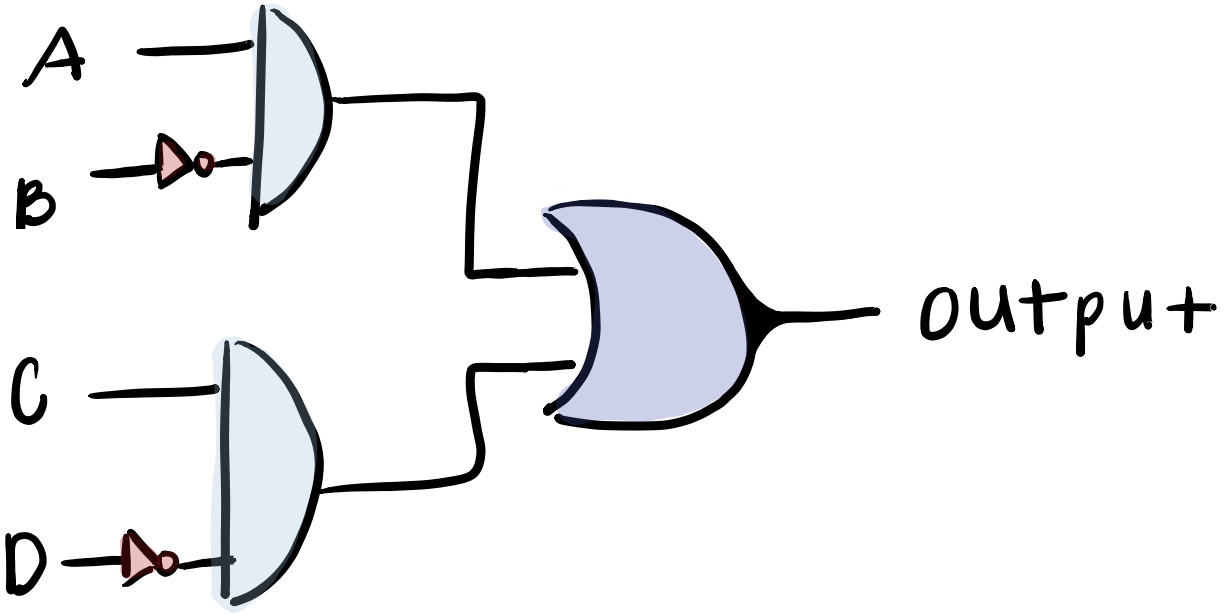
2. Draw a circuit with inputs A, B, C and D

(A && !B) || (C && !D)

NOT AND OR



3. Draw a diagram expressing how the existing how y86-64 architecture could implement a new iaddq instruction to accomplish this functionality:

	iaddq V, rB	
Fetch	icode : ifun	M_1 [PC]
	rA : rB	M_1 [PC + 1]
	val C	M_8 [PC + 2]
	val P	PC + 10
Decode	val B	R [rB]
Execute	val E ← set cc	valC + valB
memory		
write back	R [rB] ←	val E
PC update	PC ←	val P