Alyssa Kelley - Solution Document for Assignment 7

1. [40] Assume that you're given the task of optimizing graphics software that operates in the CMYK (Cyan, Magenta, Yellow, Black) color space. Specifically, you need to determine the efficiency of the following algorithm on a machine with a 4096B cache with 64B blocks and 64 sets (i.e., direct mapped). You are given the following definitions:

```
struct ColorPoint {
    long c;
    long m;
    long y;
    long k;
};

struct ColorPoint points[16][16];
```

Assume the following:

- sizeof(long) == 8.
- points begins at memory address 0.
- The cache is initially empty.
- The only memory accesses are to the entries of the array points. Variables *i*, *j*, and *sum* are stored in registers.

Determine the cache performance of the following code:

```
long sum = 0;
for (int i = 0; i < 16; i++) {
    for (int j = 0; j < 16; j++) {
        sum += square[i][j].c;
        sum += square[i][j].m;
        sum += square[i][j].y;
        sum += square[i][j].k;
    }
}
```

A. (15) What is the total number of memory reads? Why? It may help to think in terms of movq instructions.

B. (15) What is the total number of memory reads that miss in the cache? Why?

C. (10) What is the miss rate?

A. (15) What is the total number of memory reads? Why? It may help to think in terms of movq instructions.

Loop iteration - (for loop #1 = 16) * (for loop #2 = 16)

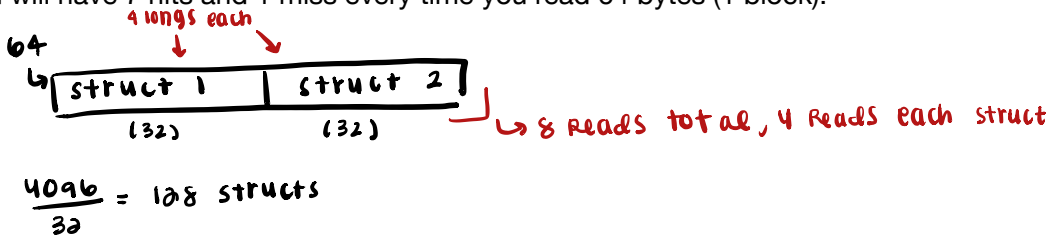
4 memory reads so (4) * (16 * 16) = 1024 total reads

Answer: 1024 total reads.

each instruction = 8 bytes and how many Reads is how many times an instruction

B. (15) What is the total number of memory reads that miss in the cache? Why?

You will have 7 hits and 1 miss every time you read 64 bytes (1 block).



sizeof(colorPoint) = 32 bytes
Each block can hold 2 structs (because it is 64)

Explanation: Since we are reading 1024 total reads and every time we read 64 bytes then we have 1 miss so that would be a total of 16 misses and 112 hits per 1024 reads.

C. (10) What is the miss rate?

-> 16/128 = 1/8 = 12.5% miss rate for 1024 total memory reads.

Notes on Part 1:

-> C = S * E * B

4096 = S * 1 * 64

S = 4096/64 = Cache sets

E = 1 because direct mapped cache
C = 4096 - byte
B = 64 bytes / block

L1

| 9 | | | | | | 16 | * Miss: 1

L2

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | * Hits: 7 +
7 + ...

| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |

8 bytes