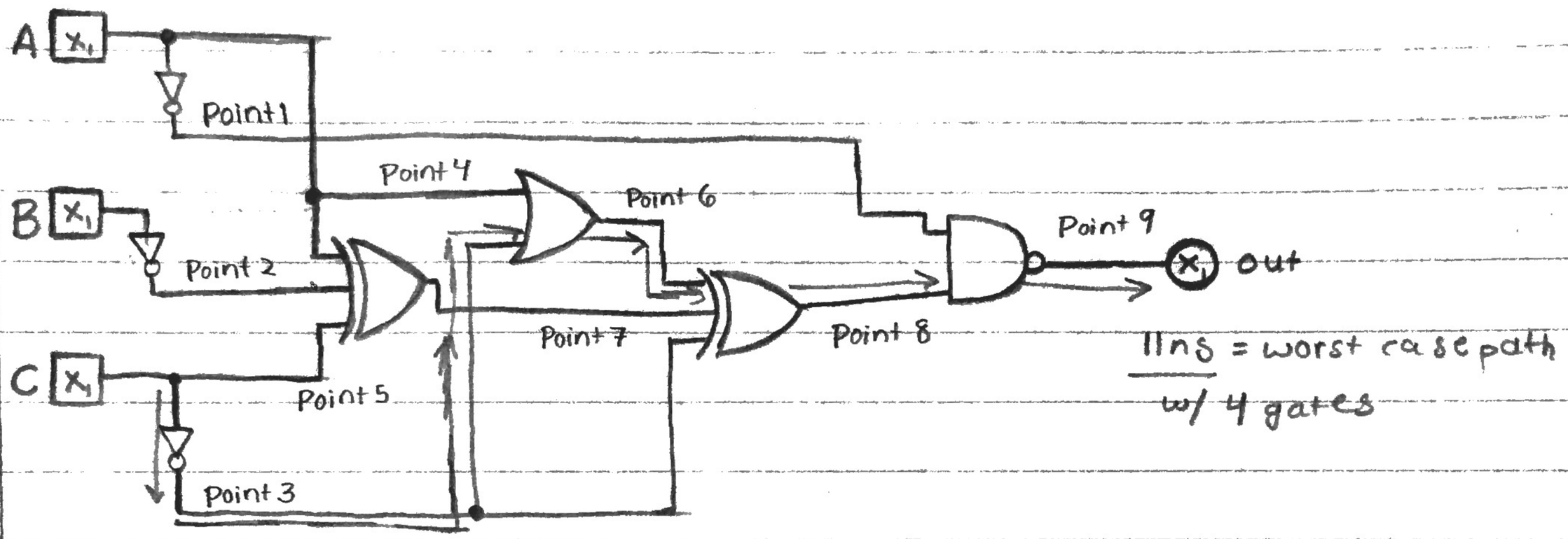
4.) What are the propagation delays at ea. marked point?

Not	1s
OR	5s
XOR	3s
NAND	2s

@ Point 1 = 1ns
@ Point 2 = 1ns
@ Point 3 = 1ns
@ Point 4 = 0ns
@ Point 5 = 0ns
@ Point 6 = 5ns
@ Point 7 = 4ns
@ Point 8 = 9ns
@ Point 9 = 11ns



5.) Given that ea. XOR gate has delay of Ans, ea. AND has delay of Bns, ea. OR gate has delay of Cns, what is propagation delay of worst case path in an N bit ripple carry adder?

XOR	Ans
AND	Bns
OR	Cns

1-bit full adder =

t_{pd} = Ans...XOR + Bns...AND + Cns...OR

* this is worst case path through a Full adder using ripple carry which goes through 3 gates to output.
* Since an N-bit ripple carry adder is made up of (N) full adders, the worst case path propagation delay is : $N(t_{pd})$

$t_{pd} = N(Ans..XOR + Bns...AND + Cns...OR)$

$= N \cdot (Ans + Bns + Cns)$