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ECS 154A
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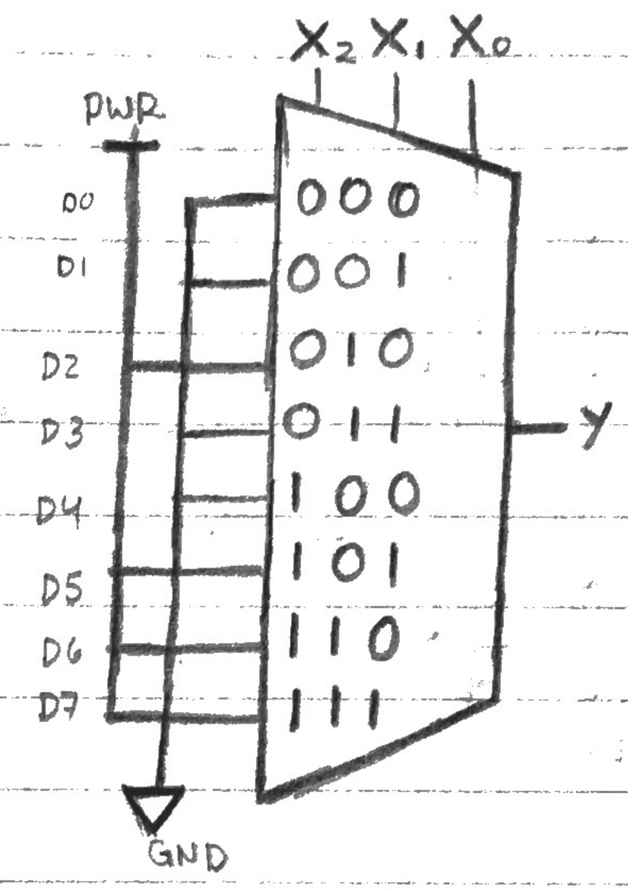
WRITTEN HOMEWORK #2

1.) Given only an 8-1 multiplexer & constants 0 and 1 implement circuit that behaves like $m_2 + m_5 + m_6 + m_7$.
3 input variables $x_2 x_1 x_0$.

	x_2	x_1	x_0	Y
0	0	0	0	0
1	0	0	1	0
→ 2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
→ 5	1	0	1	1
→ 6	1	1	0	1
→ 7	1	1	1	1

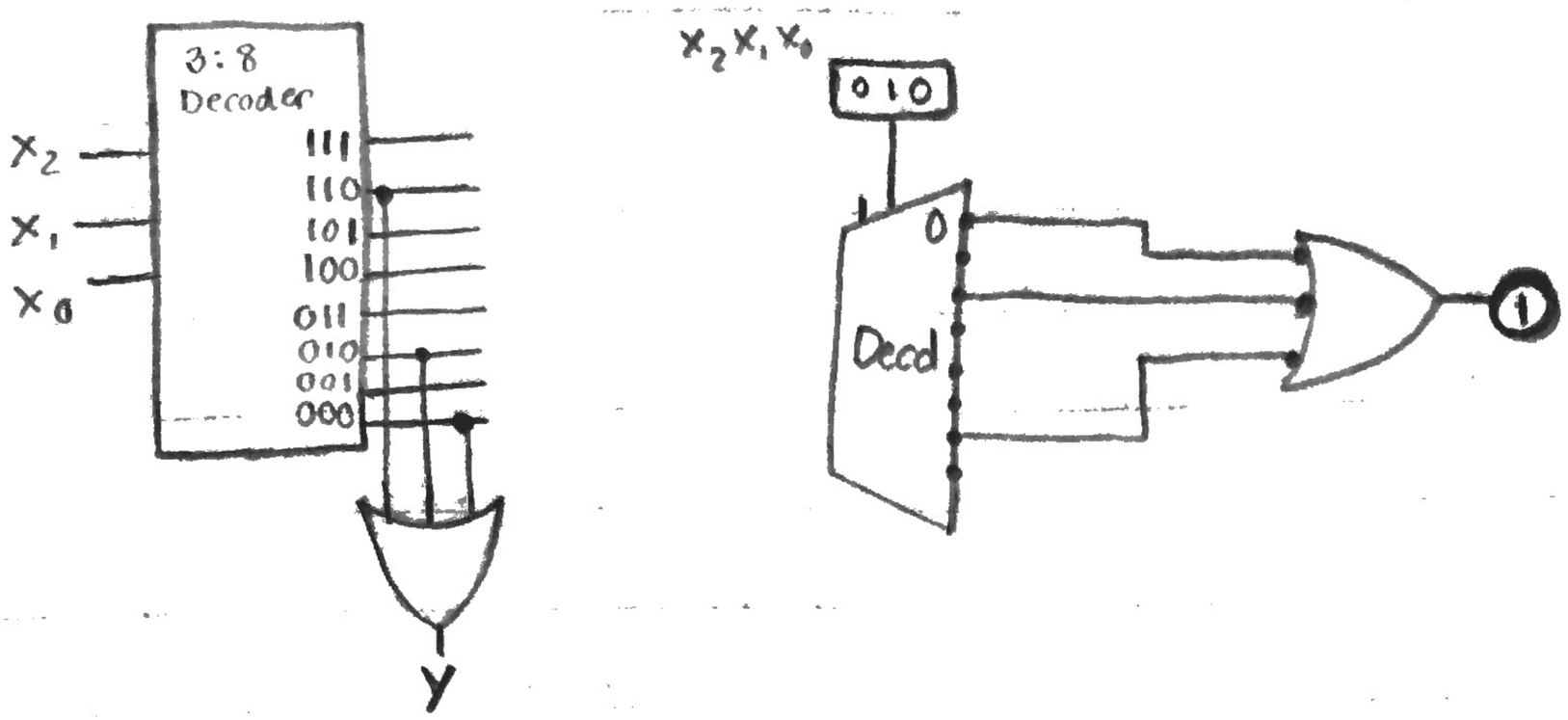
$m_2 + m_5 + m_6 + m_7 =$
$(\overline{x}_2 x_1 \overline{x}_0) + (x_2 \overline{x}_1 x_0) +$
$(x_2 x_1 \overline{x}_0) + (x_2 x_1 x_0)$



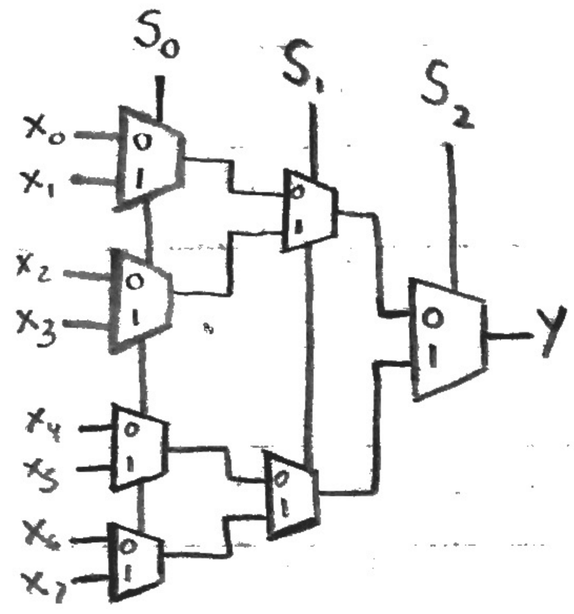
2.) Given only a 3-8 one hot decoder & OR gate, implement circuit that behaves like $m_0 + m_2 + m_6$. Use x_2, x_1, x_0.

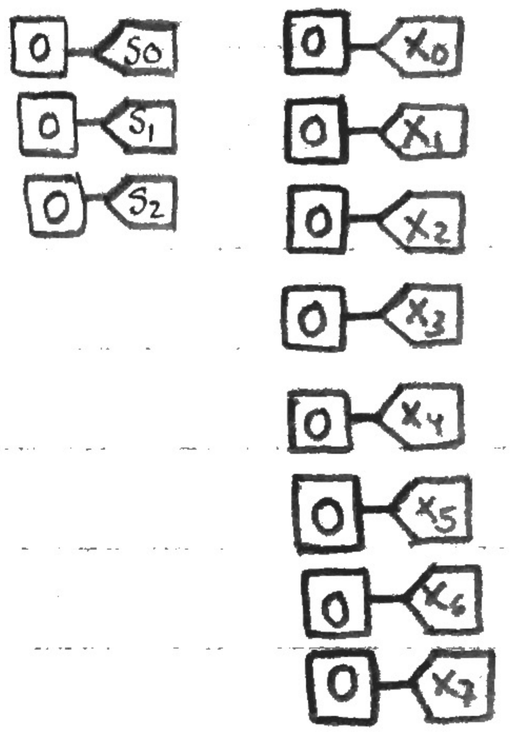
	x_2	x_1	x_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
→ 0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
→ 2	0	1	0	0	0	0	0	0	1	0	0
3	0	1	1	0	0	0	0	1	0	0	0
4	1	0	0	0	0	0	1	0	0	0	0
5	1	0	1	0	0	1	0	0	0	0	0
→ 6	1	1	0	0	1	0	0	0	0	0	0
7	1	1	1	1	0	0	0	0	0	0	0

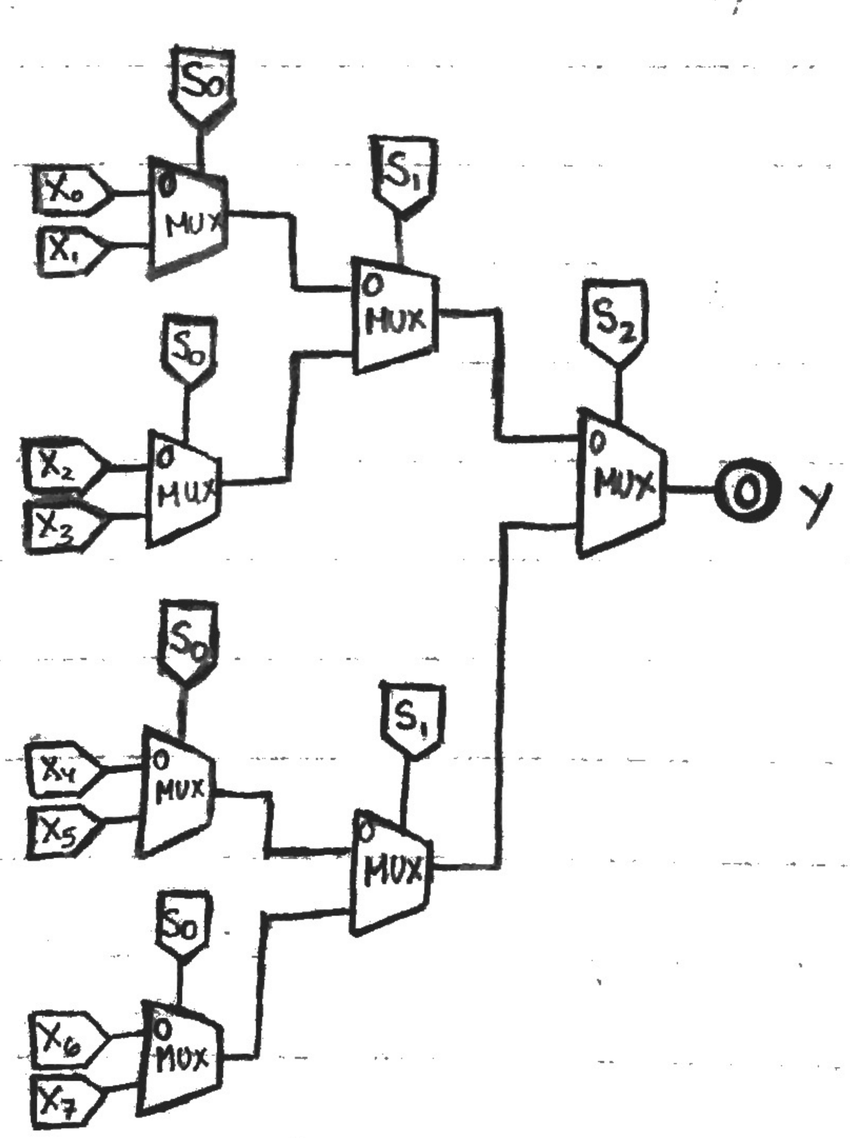
$m_0 + m_2 + m_6 =$
$(\overline{x}_2 \overline{x}_1 \overline{x}_0) + (\overline{x}_2 x_1 \overline{x}_0) +$
$(x_2 x_1 \overline{x}_0)$



3.) Use only 2-1 multiplexers to create 8-1 multiplexer.





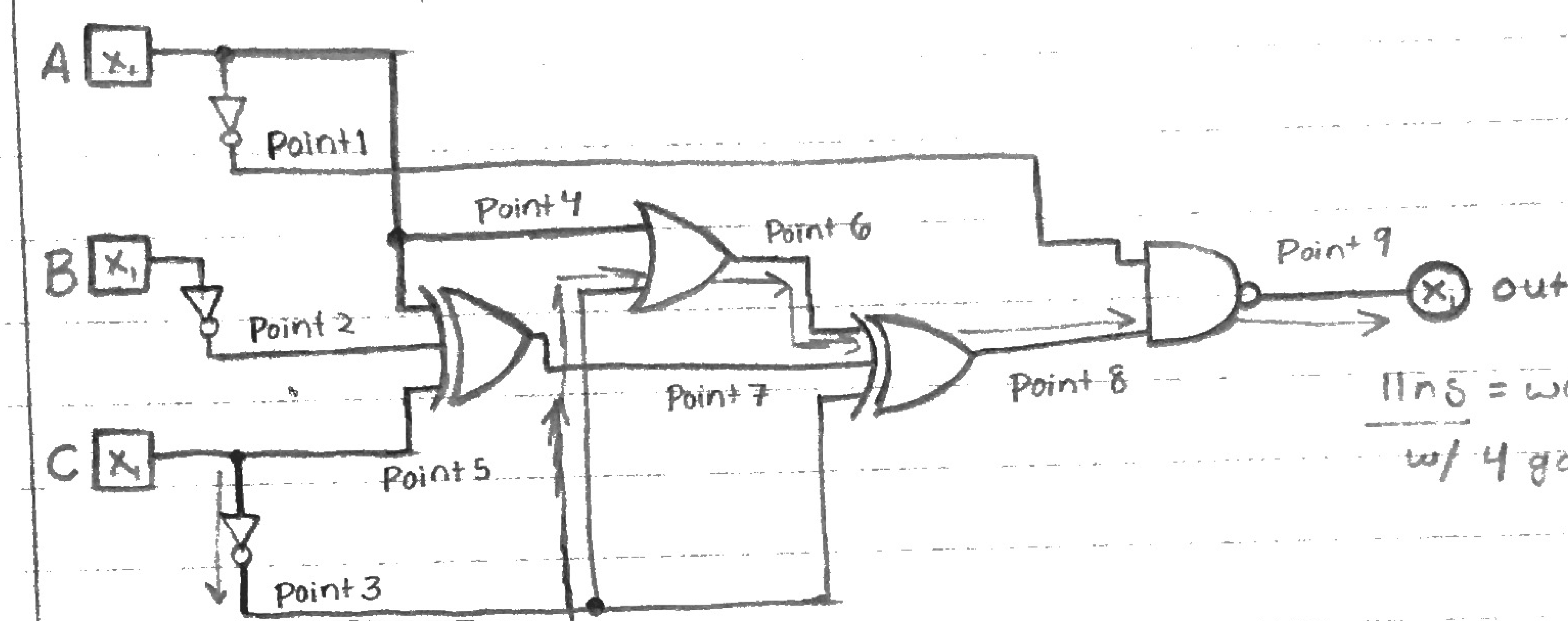


• ... voltage (0V) = ground/GND   ECE 154A Midterm 1

4.) What are the propagation delays at ea. marked point?

Not	1s
OR	5s
XOR	3s
NAND	2s

@ Point 1 = 1ns
@ Point 2 = 1ns
@ Point 3 = 1ns
@ Point 4 = 0ns
@ Point 5 = 0ns
@ Point 6 = 6ns
@ Point 7 = 4ns
@ Point 8 = 9ns
@ Point 9 = 11ns



11ns = worst case path w/ 4 gates

5.) Given that ea. XOR gate has delay of Ans, ea. AND has delay of Bns, ea. OR gate has delay of Cns, what is propagation delay of worst case path in an N bit ripple carry adder?

XOR	Ans
AND	Bns
OR	Cns

1-bit full adder =

tpd = Ans...XOR + Bns...AND + Cns...OR

* this is worst case path through a full adder using ripple carry which goes through 3 gates to output.
* Since an N-bit ripple carry adder is made up of (N) full adders, the worst case path propagation delay is : N(tpd)

tpd = N(Ans...XOR + Bns...AND + Cns...OR)

= N·(Ans + Bns + Cns)

A·(B+C)·n

A + n·(B+C)

A + N*(B+C)