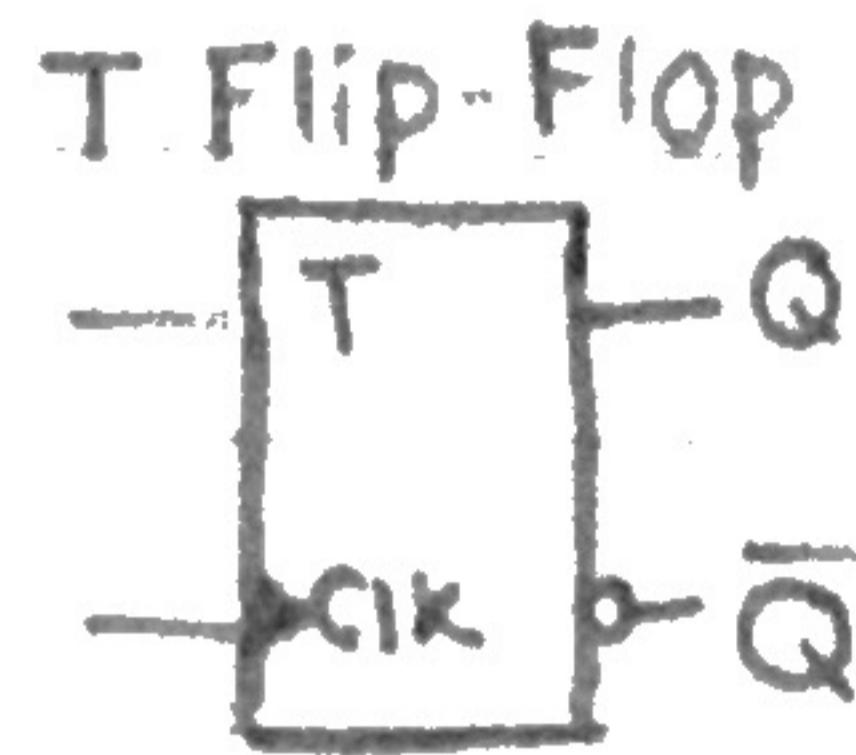
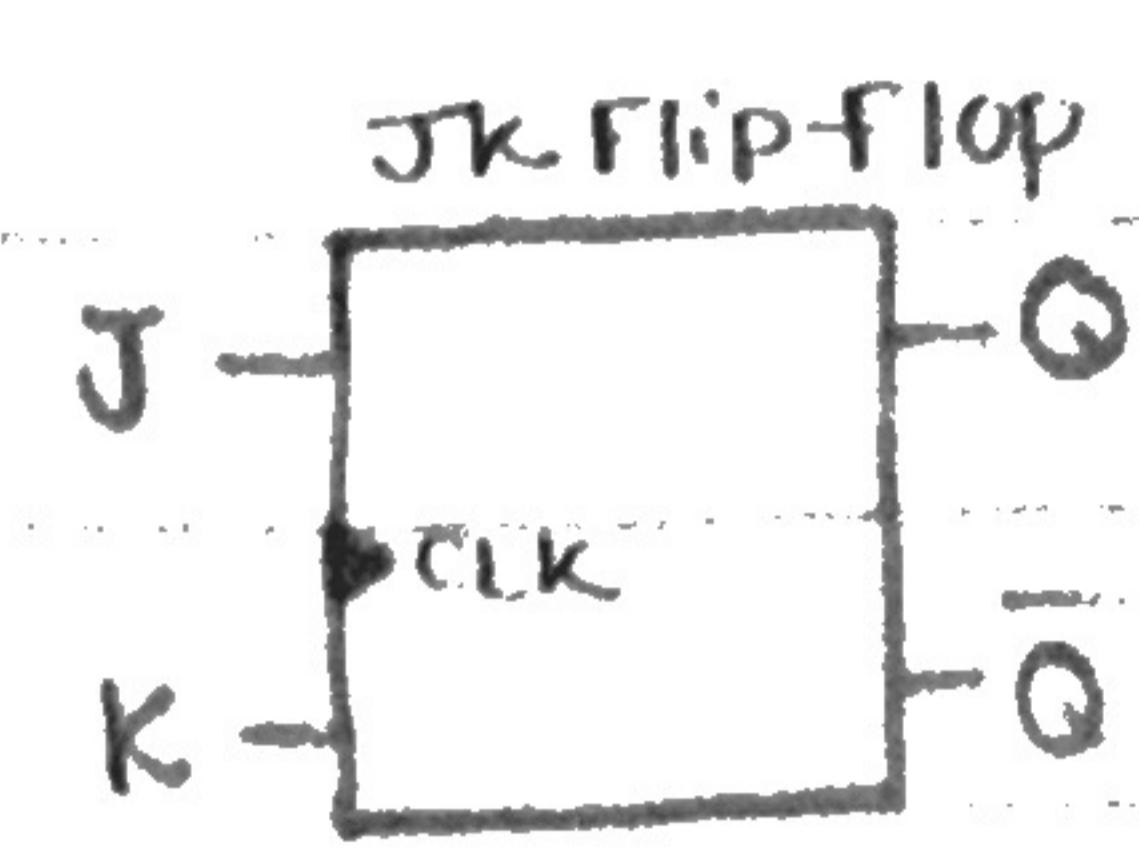


HOMEWORK #3 WRITTEN

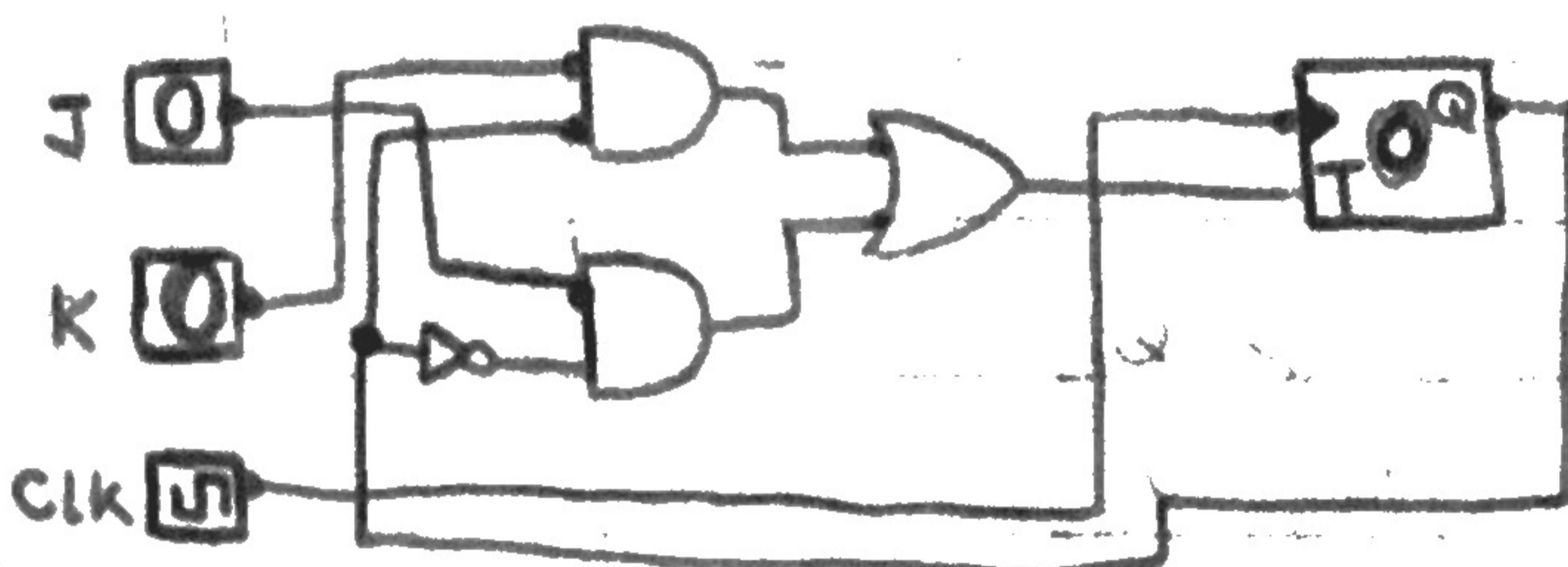
- 1.) JK Flip-Flop using TFlip-Flop and basic logic gates



T	$Q_{next}$
0	$Q_{prev}$
1	$\bar{Q}_{prev}$



JK	Q
00	00
01	01
11	11
10	10



PS	00	01	10	11
0	0	0	1	1
1	1	0	1	0

PS	0	1
0	0x	1x
1	x1	x0

J	K	$Q_{prev}$	$Q_{next}$	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

PS	00	01	11	10
0	0	0	0	1
1	0	1	1	0

$$T = J\bar{Q} + KQ$$

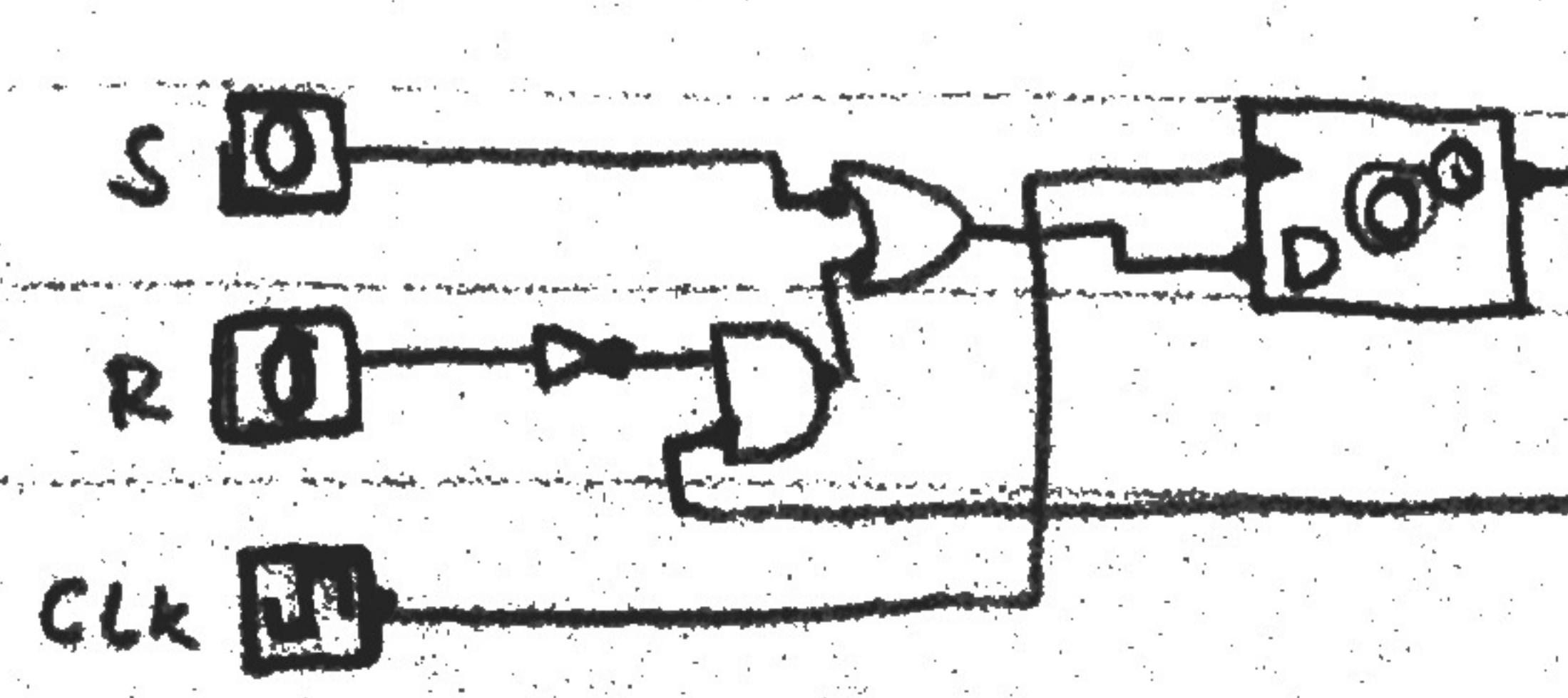
- 2.) SR Flip-Flop using D Flip-Flop

PS	SR	00	01	10	11
0	0	0	0	1	x
1	1	0	1	x	1

PS	S	R	D
0	0	1	1
1	0	0	1

SR	$Q_{prev}$	$Q_{next}$	D
00	0	0	0
01	0	1	1
10	1	0	1
11	x	x	1
11	1	x	0
11	x	1	0

PS	00	01	11	10
0	0	0	x	1
1	1	0	x	1



3.) simplest circuit possible using JK Flip-Flops

<u>Q</u>	<u>Q<sub>n</sub></u>	<u>J K</u>
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0

<u>Q</u>	<u>J K</u>	<u>Q<sub>n</sub></u>
00	00	11
00	01	10
01	10	00
11		

<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>In</u>	<u>A<sub>1</sub>, B<sub>1</sub></u>	<u>Out</u>	<u>J<sub>A</sub></u>	<u>K<sub>A</sub></u>	<u>J<sub>B</sub></u>	<u>K<sub>B</sub></u>
0	0	0	11	1	1	X	1	X
0	0	1	10	0	1	X	0	X
0	1	X	00	0	0	X	X	1
1	0	0	10	0	X	0	0	X
1	0	1	11	0	X	0	1	X
1	1	0	01	1	X	1	X	0
1	1	1	00	1	X	1	X	1



<u>In</u>	<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>00</u>	<u>01</u>	<u>11</u>	<u>10</u>
0	1	0	0	0	X	X
1	1	0	X	X	0	0

$$J_A = \bar{B}_0 \checkmark$$

1<sup>st</sup> Flip Flop  
JK

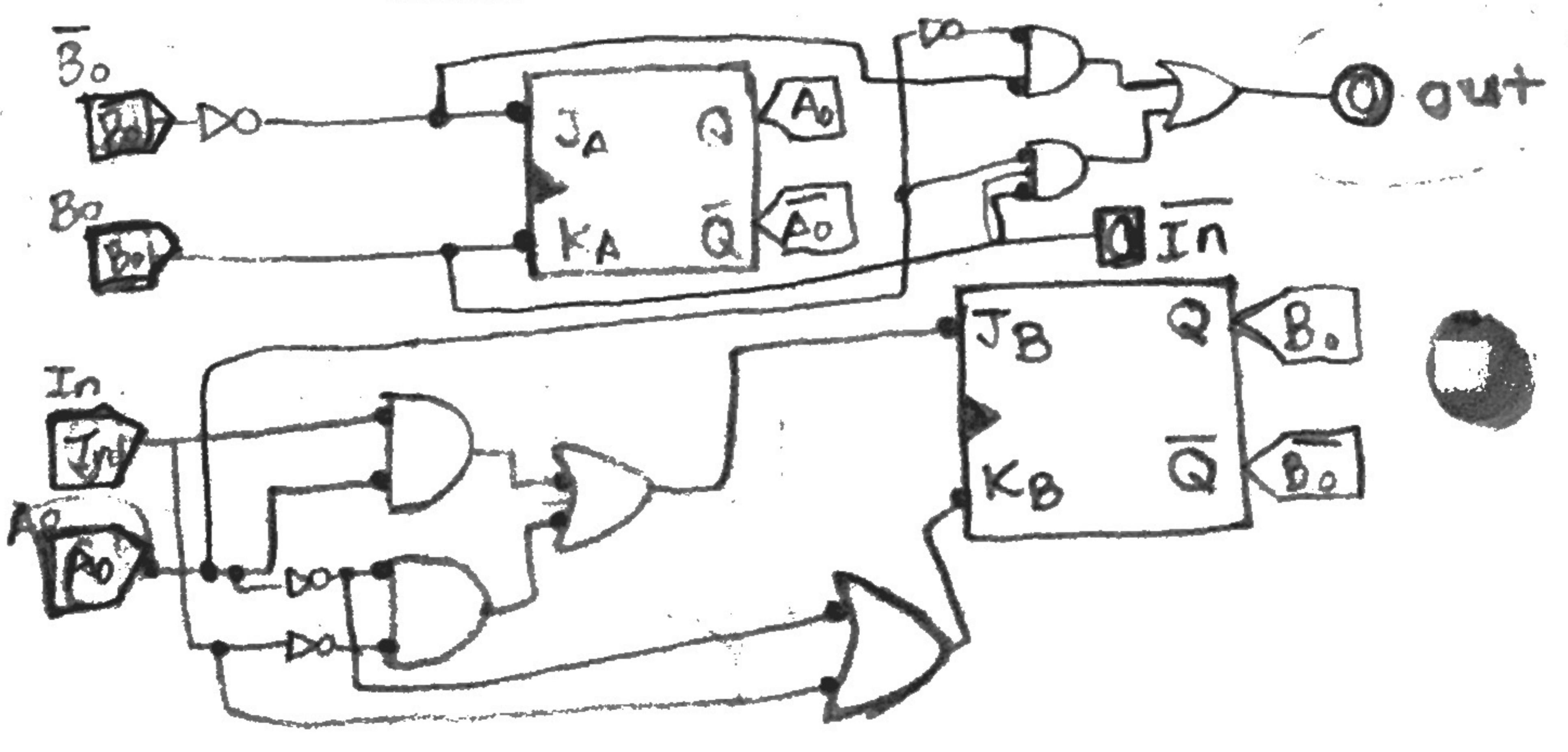
<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>0</u>	<u>1</u>
0	0	1	0
1	0	0	1

$$\text{out} = \bar{A}_0 \bar{B}_0 + A_0 B_0$$

<u>In</u>	<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>00</u>	<u>01</u>	<u>11</u>	<u>10</u>
0	0	X	X	1	0	0
1	X	X	1	X	X	0

$$K_A = B_0 \checkmark$$

Circuit w/ JK FlipFlops



<u>In</u>	<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>00</u>	<u>01</u>	<u>11</u>	<u>10</u>
0	1	X	X	0	0	0
1	0	X	1	X	X	0

$$J_B = \bar{In} \bar{A}_0 + In A_0$$

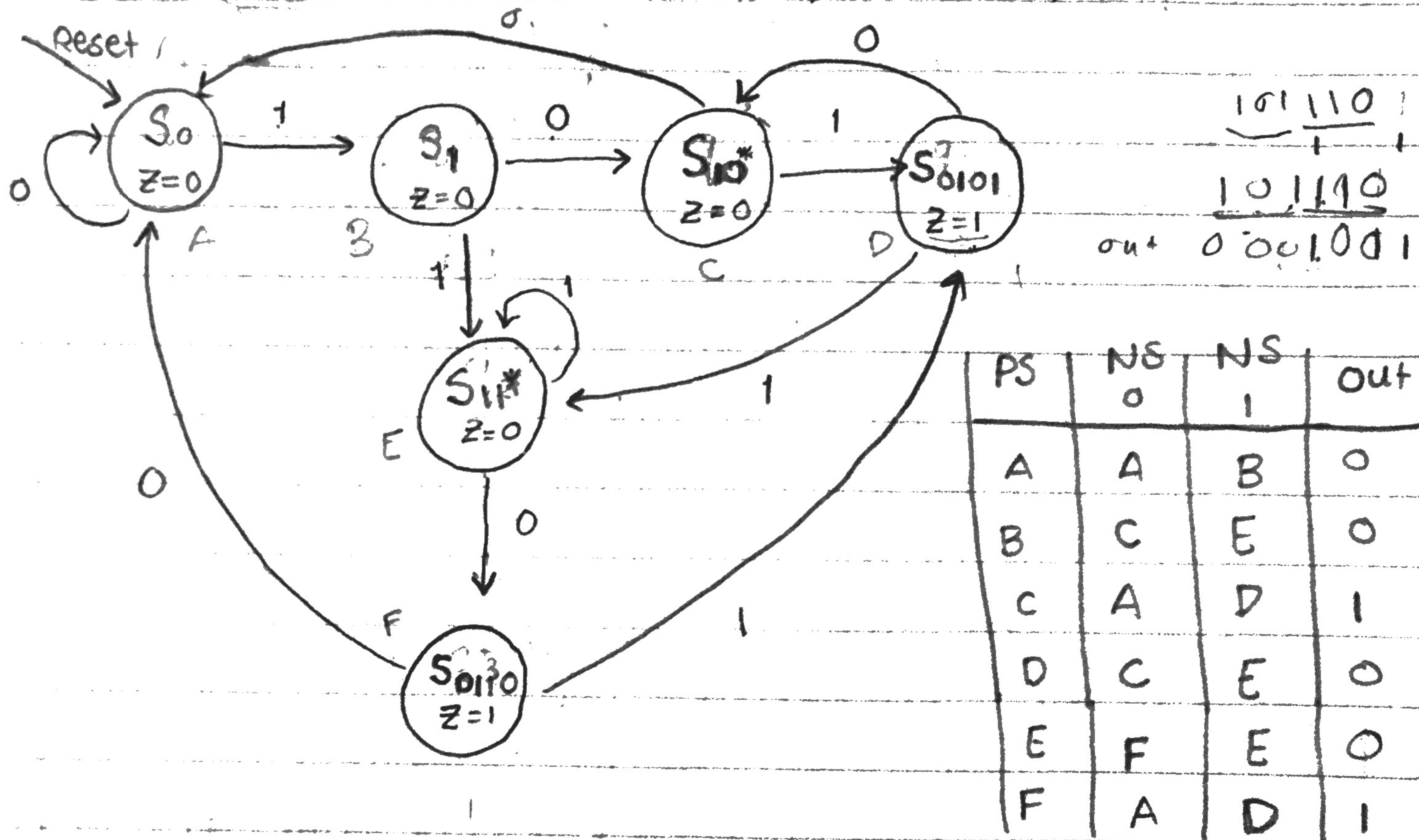
<u>In</u>	<u>A<sub>0</sub></u>	<u>B<sub>0</sub></u>	<u>00</u>	<u>01</u>	<u>11</u>	<u>10</u>
0	X	1	0	0	X	X
1	X	1	X	1	X	0

$$K_B = \bar{A}_0 + In$$

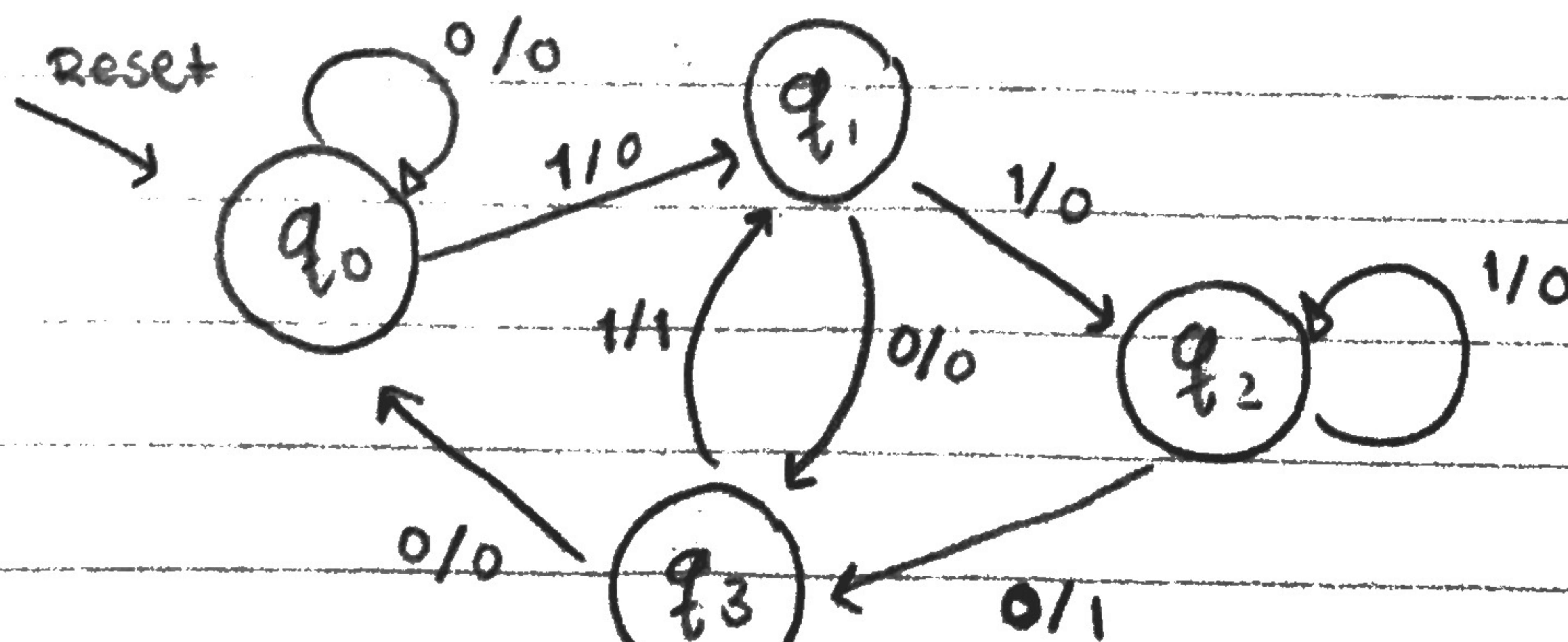
4.) MOORE FSM , detect 110 or 101 in input

States:	out
$q_0 = \emptyset$	0
$q_1 = 1$	0
$q_2 = 11$	0
$q_3 = 110 \rightarrow 1$	
$q_4 = 10$	0
$q_5 = 101 \rightarrow 1$	

Q	$Q_n @_0$	$Q_n @_1$	Out
$S_0$	$S_0$	$S_1$	0
$S_1$	$S_{10}^*$	$S_{11}^*$	0
$S_{11}^*$	$S_{0110}$	$S_{11}^*$	0
$S_{0110}$	$S_0$	$S_{0101}$	1
$S_{10}^*$	$S_0$	$S_{0101}$	0
$S_{0101}$	$S_{10}^*$	$S_A^*$	1

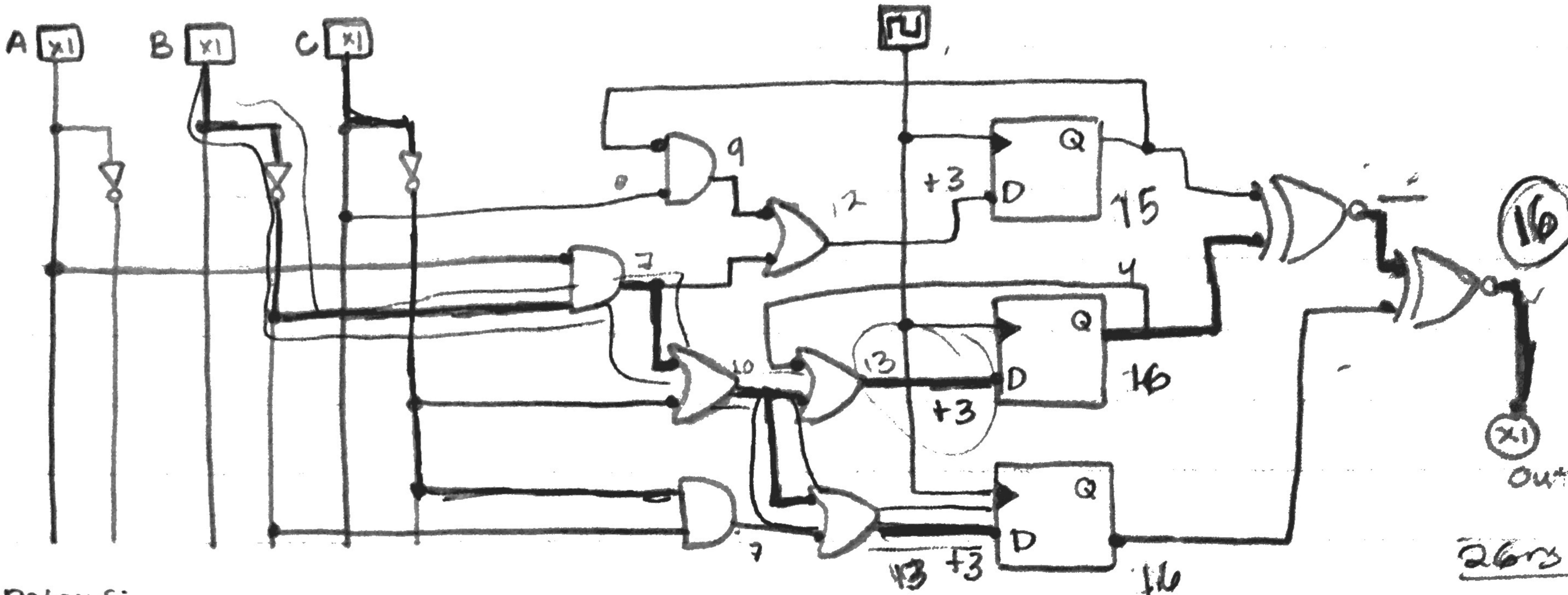


5.) Mealy Model FSM . . . detect 110 or 101 in input



Q	$Q_n @_0$	$Q_n @_1$	out
$q_0$	$q_0$	$q_1$	0 0
$q_1$	$q_3$	$q_2$	0 1
$q_2$	$q_3$	$q_2$	1 0
$q_3$	$q_0$	$q_1$	0 1

6.)

Delays:

$$\begin{array}{lll} \text{AND} - 5\text{ns} & \text{NOT} - 2\text{ns} & \text{DFF} - 4\text{ns} \\ \text{OR} - 3\text{ns} & \text{XNOR} - 6\text{ns} & \text{Setup DFF} = \underline{3\text{ns}} \end{array}$$

max clock frequency:

$$f_{\max} = \frac{1}{\text{propagation delay}} = \frac{1}{16\text{ns}}$$

$$f_{\max} = \frac{1}{28\text{ns}} \text{ or } 0.0357 \text{ Hz} \quad 35.7 \text{ MHz}$$

worst case path:

$$\max(15, 16, 16)$$

$$\max = 16 \text{ ns out}$$

$$\max = 28 \text{ ns to } \overbrace{\hspace{1cm}}$$

$$\begin{aligned} & 16 \text{ ns before DFF} \\ & \text{to output} = \underline{16 \text{ ns}} \end{aligned}$$

$$\begin{aligned} \text{path} = & t_d \text{ NOT} + t_d \text{ AND} + t_d \text{ OR} + t_d \text{ OR} + t_d \text{ setup} + t_d \text{ DFF} \\ & + t_d \text{ XNOR} + t_d \text{ XNOR} = \\ & 2 + 5 + 3 + 3 + 3 + 4 + \underline{6 + 6} \end{aligned}$$