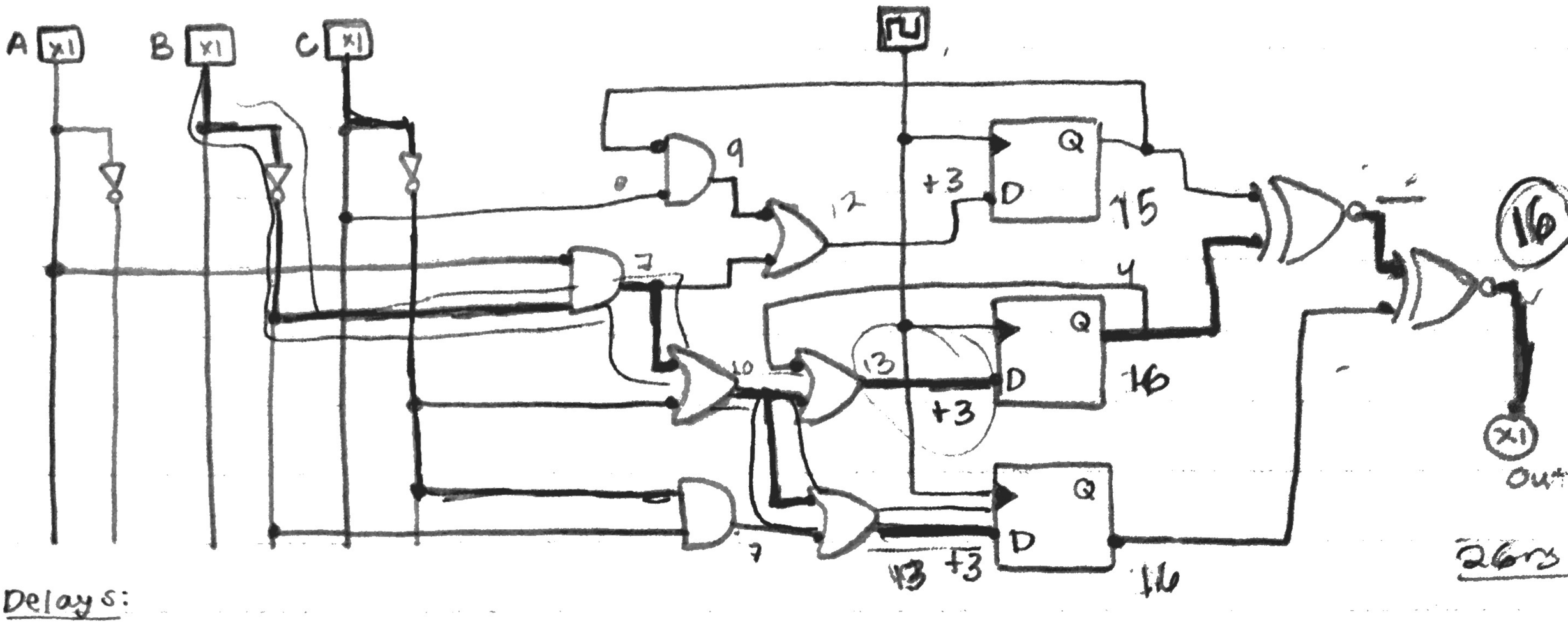
6.)



Delays:

AND - 5ns NOT - 2ns DFF - 4ns

OR - 3ns XNOR - 6ns Setup DFF = 3ns

max clock frequency:

$f_{max} = \frac{1}{\text{propagation delay}} = 1/\text{delay}$

$f_{max} = \frac{1}{28ns}$ or $0.0357\ Hz$ / $35.7\ MHz$

1/16ns

worst case path:

max (15, 16, 16)

max = 16 ns

max = 28 ns → to out

16ns before DFF

to output = 16ns

path = t_d NOT + t_d AND + t_d OR + t_d OR + t_d Setup + t_d DFF

+ t_d XNOR + t_d XNOR =

2 + 5 + 3 + 3 + 3 + 4 + 6 + 6