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WRITTEN HOMEWORK #5

1.) Given Fully Associative cache of size 2^{10} bytes. Line size of 16 bytes, show address of 29 bits is partitioned.

- cache size = 2^{10} = 1024 bytes

10 9 8 7 6 5 4 3 2 1 0
1024 512 256 128 64 32 16 8 4 2 1

- Line size = 2^4 = 16 bytes
- offset size = $\log_2 16$ = 4 bits
- Tag = 29 - $\log_2 16$ = 25 bits

partition →

TAG	offset
Bits 28 - 4	Bits 3 - 0

2) Given Direct Mapped cache of size 2^{12} bytes. Line size of 32 bytes, show Address of 50 bits is partitioned.

- cache size = 2^{12} = 4096 bytes
- Line size = 2^5 = 32 bytes
- set size = $\log_2 4096$ = 12 bits
  - ↳ offset = $\log_2 32$ = 5 bits
- Tag = 50 - 12 - 5 = 33 bits remaining

partition →

TAG	SET	OFFSET
Bits 49-12	Bits 11 - 5	Bits 4 - 0

3.) Given 5-way set Associative cache of size 5242880 bytes with line size of 64 bytes show how an Address of 64 bits would be partitioned

- cache size = 5242880 bytes
- Line size = 2^6 = 64 bytes
- # of sets = 5 → 50 4-0 bits
- set size = 5242880 / 5 = 1,048,576
  - ↳ 1,048,576 = 2^{20} → 20 bits
- offset = 2^6 = 64 bytes 6 bits

partition →

TAG	SET	OFFSET
Bits 63 - 20	Bits 19 - 6	Bits 5 - 0