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Detection of Limited Magnitude Errors in Emerging Multilevel Cell Memories by One-Bit Parity (OBP) or Two-Bit Parity (TBP)

SHANSHAN LIU^{ID}, (Member, IEEE), PEDRO REVIRIEGO^{ID}, (Senior Member, IEEE),
AND FABRIZIO LOMBARDI^{ID}, (Fellow, IEEE)

S. Liu and F. Lombardi are with the Dept. of ECE, Northeastern University, Boston MA 02115, USA.
P. Reviriego is with the Universidad Carlos III de Madrid, Av. Universidad 30, Leganés Madrid, Spain.

CORRESPONDING AUTHOR: S LIU (ssliu@coe.neu.edu.)

ABSTRACT Emerging memory technologies rely on Multilevel Cells (MLC) to achieve high density; the use of multiple levels per cell allows storage of multiple bits, but it also reduces the margins and makes it error prone. Error control codes (including error correction and detection codes) can be used to protect MLC memories from errors; however, most existing coding schemes have been designed for traditional binary memories (so storing a single bit). In MLC memories, errors cause a change from a level to an adjacent level or to the next one (depending on the employed technology), so they are often referred to as limited magnitude errors. For a binary coding of levels to bits, these limited magnitude errors can corrupt several bits making traditional coding schemes inefficient. In this paper, error detection of MLC memories is considered when a binary encoding of levels to bits is used and two new schemes are proposed: One-Bit Parity (OBP) and Two-Bit Parity (TBP). The first scheme targets errors of magnitude-1 for detection using a single parity bit that checks only one bit per cell. The second scheme detects both magnitude-1 and -2 errors using only two parity bits. Both schemes are compared to existing alternatives, namely Gray coding combined with a single parity bit (GP) for OBP and Interleaved Parity (IP) for TBP. The results show that OBP reduces the encoding and error detection circuitry complexity and delay, while TBP additionally reduces the number of parity bits for some configurations. Therefore, OBP and TBP can be efficient alternatives for detection of limited magnitude errors in MLC memories that use a binary encoding of levels to bits.

INDEX TERMS Multilevel cell memories, error control codes, limited magnitude errors

I. INTRODUCTION

Most emerging memory technologies utilize multilevel cells (MLCs) to achieve higher integration and density [1]–[3]. Technologies such as phase change (PC), magneto-electric (ME) and memristor are mostly based on phenomena that occur in resistive and magnetic materials by which a feature of the storage medium (e.g., resistance or memristance) is changed. MLC memories can store multiple bits in each cell, for example, PC memories rely on the reversible thermally-assisted phase transformation of the chalcogenide alloy $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), as occurring between the amorphous phase with a high resistivity and the poly-crystalline phase with a low resistivity. The large resistance margin between those two phases makes possible that several states can be stored in different levels [4]; octal PCM cells (so storing 3 bits) are already commercially available.

Due to benefits such as high density, non-volatility and byte-addressable, MLC memories have become an attractive alternative to traditional binary memory solutions (e.g., DRAM, and cache [5], [6]). As in the case of traditional binary memories, errors also pose a serious data integrity challenge in MLC memories. However, different from the random bit flips in a SRAM due to a transient event upset, MLC memories are prone to physical phenomena that lead to permanent errors. The error is usually identified by the levels of the MLC memory; for example, if such defective phenomenon changes the level for bit storage, then this (limited) error results in a change of magnitude in the stored bits, hence it is referred to as a magnitude error. For example, the resistance of a PC material tends to drift over time [7], and therefore the margin between adjacent levels degrades, leading to state changes. Experimental results show that limited

magnitude errors in PCM are unidirectional (i.e., they occur in only one direction) [8]; over time and as function of programming a PCM cell, the drift may exceed (overlap) the adjacent level and if no monitoring or corrective circuit are provided [7], [9], a magnitude-2 error may occur (of a bidirectional nature), particularly if the levels are very near in resistance values with no monitoring circuits. For memristor-based memories, the change in resistance is a function of the number of switching cycles [10]; for these memories, both the highest and lowest resistive values can substantially change [11]. In theory, errors can be extending over the entire resistive range, but in practice over a normal lifetime they are typically limited to $-/+ 2$ levels [9], [12].

Error correction and detection coding schemes have been extensively used in traditional and emerging memory systems [13]–[16]. Additional redundancy parity bits are stored together with the data bits in each memory word. For a write operation, the encoder calculates the parity bits based on the data bits to generate a codeword that is then stored in the memory word. As for the errors on the codeword, the decoder can detect or correct them and output an error detection signal or the correct data for the read operation. In general, an error correction code (ECC) will require more parity bits to provide distinguishable syndromes for error correction, as well as a higher decoding complexity than an error detection code (EDC) under the same number of errors. Therefore, EDCs are more attractive in applications, in which fast detection of errors in memories is first performed; detection triggers the exception handler in the system to perform correction (if possible) for the errors or reconfiguration in a hierarchical manner if needed [17], [18].

Coding schemes for limited magnitude errors in MLC memories have been proposed in recent years [19]–[22]. However, most of them are ECCs that focus on error correction relying for example on the use of non-binary codes. This leads to a significant overhead both in terms of parity check bits and decoder complexity. In [19], asymmetric errors of magnitude one are corrected by noting that for a binary encoded value, a magnitude one error will always affect the lowest bit. Based on that observation, a Hamming code that protects the lowest bit of each cell is used to detect the erroneous cell and the error is then corrected by adding one to the stored value. In [21], Orthogonal Latin Square (OLS) codes are used to protect the lower bits and combined with Single Error Correction (SEC) codes to provide magnitude one/two correction for symmetric errors using a similar approach.

For error detection, a single parity check is typically used to detect any single bit error on data. However, it is insufficient as limited magnitude errors can cause multiple bit flips (this will be discussed in detail in the next section). An obvious approach would be to use interleaved parity (IP) bits to detect multiple bit errors in a single memory cell [23]. This can be done for example, when the number of parity bits is the same as the number of bits stored in a cell. If the different levels per cell are mapped to Gray coding, all limited magnitude errors affecting the adjacent level in either direction can

cause only one bit flip. In this case, Gray coding combined with a single parity bit (GP) can be used to detect limited magnitude-1 errors, which can be an attractive alternative to the IP scheme due to the low redundancy requirement. Some ECCs can also be exploited to detect errors. For example, a Single Error Correction Double Error Detection (SEC-DED) code can be used to detect up to triple bit errors, because it has a minimum distance of four. This however, is not efficient for MLC memories, because the number of parity bits would be larger than for an interleaved parity protection [24].

In this paper, we propose two error detection schemes for limited magnitude errors in MLC memories that use a binary encoding of levels to bits: the One-Bit Parity (OBP) scheme for magnitude-1 error detection and the Two-Bit Parity (TBP) scheme for both magnitude-1 and magnitude-2 error detection. The OBP scheme only uses one parity check bit regardless of the number of bits stored in the memory cell, while the TBP scheme only uses two. This makes them more efficient than traditional schemes. Additionally, the encoding and error detection circuitry are also simpler and faster.

The rest of the paper is organized as follows. In Section II, the relationship between limited magnitude errors in memory states and multiple bit errors on data is discussed. The interleaved parity scheme and the single parity scheme combined with Gray coding that can detect such errors, are also described. In Section III, limited magnitude error patterns are analyzed first, and then based on the provided analysis, the OBP and TBP schemes are proposed. Section IV compares the proposed schemes with traditional schemes in terms of memory overhead and the complexity of the encoder/decoder circuitry. Finally, Section V presents the conclusion of this paper.

II. PRELIMINARIES

A. LIMITED MAGNITUDE ERRORS IN MLC MEMORIES

MLC memories consist of cells with 2^b levels, so that 2^b states (corresponding to b data bits in binary coding) can be stored in a single cell. As discussed in the introduction, MLC memories exhibit limited magnitude errors. The errors are caused by the shift in states stored in the levels due to phenomena such as drifting or deterioration of the level definition (in most cases given by the resistance). Consider a PC memory (PCM) as an example; Figure 1 shows the basic principles of the resistance drift in a cell. The resistance at each level varies according to a Gaussian distribution and accounts for less (more) drift when the PCM is in the crystalline (amorphous) phase. After a PCM cell is programmed, the resistance of each level changes at T (Figure 1); selection of the so-called threshold resistances (as separating the levels) as either fixed or variable values can be used. However, endurance due to multiple programming times is rather weak, so the resistance of the cell changes. If no monitoring is provided [12] overlapping of levels may exist and an erroneous output will be provided following a read operation [8]. As the resistance in a PCM cell increases with time, drift causes the occurrence of errors of a positive magnitude, but only in one direction (unidirectional) [7], [12]. Overlapping

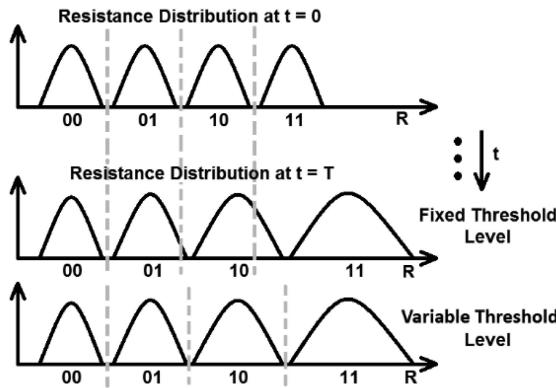


FIGURE 1. PCM resistance distribution over time subject to drift [7].

levels are likely to be encountered when the resistance range is limited and multiple states are present in the MLC cell. While variable threshold levels may partially alleviate the erroneous effects of drift, they also cause a significant increase in peripheral/supporting circuitry [12].

A different case of magnitude errors occurs in memristor-based memories. Experimental results show that after a number of switching cycles, a memristor degrades significantly and ultimately, its behavior resembles a stuck-at fault [10], [25]. Figure 2 shows the deterioration of the resistance of a memristor. Resistance changes in both directions (the on-resistance increases, while the off-resistance decreases) as function of the number of switching cycles; as result of the resistance deterioration, the switching behavior causes the resistances of the SET and RESET states to change, hence causing (bidirectional) errors of limited magnitude greater than 1.

As a general consideration, the mapping of levels to bits is a function of the data stored in a cell; therefore, when limited magnitude errors occur, they cause multiple bits to flip in a memory cell. Figure 3 shows the binary mapping from bits to states in a 3-bit MLC memory cell (i.e., 8 levels). When for example the state shift between the 4th and 5th levels (so a magnitude-1 error and the state changes by $+/- 1$ levels) occurs, a triple bit error with a pattern of "111" (i.e., affecting all three data bits) is manifested. Instead, for a shift between the 5th and 7th levels (so a magnitude-2 error as the

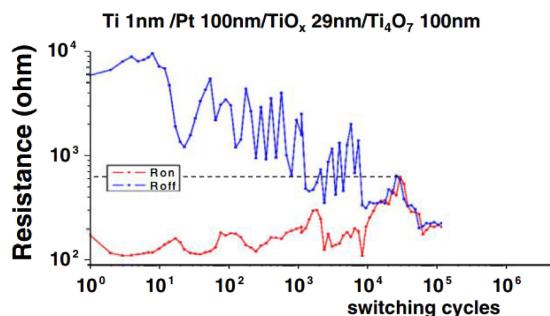


FIGURE 2. Memristor endurance experiment (resistance vs number of switching cycles) [10].

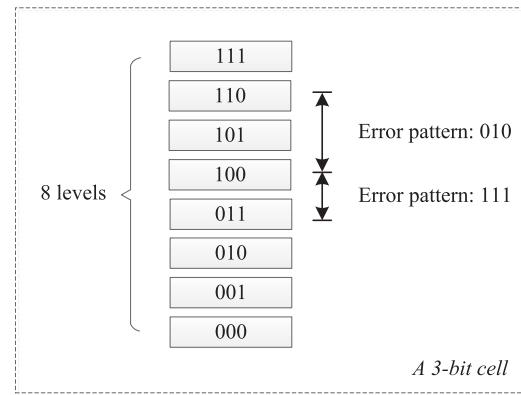


FIGURE 3. A 3-bit MLC memory cell with binary mapping.

state changes by $+/- 2$ levels), this would cause a single bit error of "010" (i.e., affecting only the second lowest bit).

B. INTERLEAVED PARITY SCHEME (IP)

Interleaved parity (IP) bits are widely used to detect soft errors in traditional (binary) memories, but they can also be used to detect limited magnitude errors in MLC memories. Consider a word stored in k cells and each of b bits. Denote the bits in the word as d_{ij} , where i is the index of the cell (from 1 to k) and j is the index of the bit (from 1 to b) in the cell. As the errors can affect any bit in the cell, b interleaved parity bits are needed to detect all errors and they are given as follows:

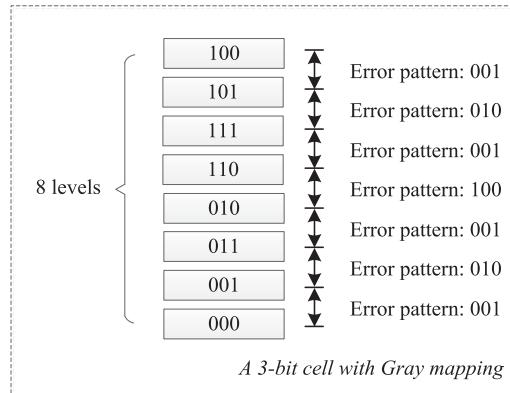
$$p_j = d_{1,j} \oplus d_{2,j} \oplus \dots \oplus d_{k-1,j} \oplus d_{k,j}, \quad (1)$$

where \oplus is the addition operation in $GF(2)$ and can be implemented by using an *xor* logic gate. An error detection signal can be generated by checking the b parity computations. To cover all data bits, one additional cell storing the parity bits is needed in each memory word. For a 3-bit cell, the encoder includes three parity computations to generate p_1, p_2 and p_3 . In the error detector circuit, the parity bits are recomputed using the same logic, but based on the stored data and then compared with the stored parity bits to generate the syndrome bits s_1, s_2 and s_3 . If there is a match in each comparison, the value of the syndrome bits is "0". Otherwise, any of the syndrome bits taking a value of "1" will trigger the error detection signal e , i.e., there is an error in the memory word and is flagged out.

This method can detect any error that affects a single memory cell; however, the number of parity bits increases with the number of bits stored in a cell.

C. GRAY CODING WITH SINGLE BIT PARITY SCHEME (GP)

Gray coding is widely used for error correction in digital communication systems. Two successive values in Gray coding differ in only one binary digit. Consider limited magnitude errors in MLC memories; if the states stored in each cell are mapped to Gray coding, magnitude-1 errors affecting the

**FIGURE 4.** A 3-bit MLC memory cell with Gray mapping.

states in adjacent levels will cause only single bit errors (i.e., one bit flipped in a cell) instead of multiple bit errors. The mapping of a 3-bit MLC memory cell is shown in Figure 4 for Gray mapping of levels to bits; all magnitude-1 errors have only a single “1” in the pattern, so they can be detected by using a single bit parity that covers all data bits:

$$p = d_{1,1} \oplus d_{2,1} \oplus \dots \oplus d_{k,1} \dots \oplus d_{1,b} \oplus d_{2,b} \oplus \dots \oplus d_{k,b}. \quad (2)$$

Therefore, to detect magnitude-1 errors in a single MLC memory cell, Gray coding combined with a single parity bit (GP) is an attractive alternative to the IP scheme, because it reduces the number of parity bits. The additional cell for the parity bits needed by the IP scheme is not required when one or more spare bits are available in a cell (note that differently from previous works like [26] that use spare cells added to correct manufacturing defects, in our case spare bits are due to a mismatch between the word size and the number of bits stored per cell). The encoder and error detector are also simpler, because only the computation logic for a single parity is needed. This scheme however, is not able to detect magnitude-2 errors because they affect two bits.

III. PROPOSED SCHEMES

Limited magnitude errors in adjacent levels are revealed as error patterns on the bits when employing binary coding for mapping between bits and states in each MLC cell. This is analyzed next and then used to design the proposed error detection schemes: One-Bit Parity (OBP) and Two-Bit Parity (TBP). The OBP (TBP) scheme provides the same error detection capability as the existing GP (IP) scheme. The error detection capabilities of existing and proposed schemes are presented in Table 1.

A. LIMITED MAGNITUDE ERROR PATTERNS

As an example, consider a MLC memory with 3-bit cells of Figure 3 for all possible limited magnitude-1 and magnitude-2 errors in either direction (i.e., bidirectional limited magnitude errors). So, it is possible to find all error patterns in a 3-bit memory cell, in which:

TABLE 1. Computation of error detection capability.

Scheme	Error detection capability
GP	Magnitude-1 errors
Proposed OBP	Magnitude-1 errors
IP	Magnitude-2 errors
Proposed TBP	Magnitude-2 errors

- All magnitude-1 errors include a total of three patterns: 001, 011, 111.
- All magnitude-2 errors include a total of two patterns: 010, 110.

Magnitude-1 errors will always affect the lowest bit stored in the cell, while magnitude-2 errors will always affect the second lowest bit [19], [21]. This feature of the error patterns is also applicable to other size of MLC cells as the states stored in all levels are mapped by binary coding (the difference between each two states at adjacent levels is “1” while the difference in levels in the other case is “10”). Another observation on the error pattern is that except for errors affecting only the lowest bit generating “0…01” and the second lowest bit generating “0…010”, all of the other possible patterns are composed of consecutive bits and include the all ‘1’ pattern, such as “0…011”, “0…0111”, …, “11…1” for magnitude 1 errors and “0…0110”, “0…01110”, …, “11…10” for magnitude 2 errors. This is due to the carry effect in the binary addition operation between states in two adjacent or distance of two levels. For example, from the state “011” stored in the 4th level to “100” stored in the 5th level, the binary value of “001” is added (i.e., 011 + 001 = 100). There is a carry for the highest bit, so that all three bits flip, causing consecutive bits of ‘1’ in the pattern.

The first feature of limited magnitude error patterns in MLC memories leads to two efficient error detection schemes by using only one or two parity bits (the OBP and the TBP schemes) as discussed next. The second feature of the patterns is used to prove that the TBP scheme is optimal in terms of parity bits.

B. ONE-BIT PARITY SCHEME (OBP)

As all magnitude-1 errors always affect the lowest bit stored in the cell, the so-called One-Bit Parity (OBP) scheme is proposed to detect all such errors. OBP uses a single parity bit that checks only the last bit in each cell. For a word storing k cells (and each of b bits), the single parity bit p is given as follows:

$$p = d_{1,1} \oplus d_{2,1} \oplus \dots \oplus d_{k-1,1} \oplus d_{k,1}. \quad (3)$$

Based on equation (3), parity computation is implemented using several *xor* logic gates. In the error detector circuit, only one syndrome bit is checked by computing the parity bit with the received data bits.

Note that the introduced parity bit needs to be stored on the lowest bit in a memory cell, because errors on the parity bit also need to be taken into account. Moreover, parity computation can be optimized when there is one or more spare bits in

TABLE 2. Number of inputs in parity computation circuit.

Data size	# bits /cell	# inputs		# parity bits	
		GP	Proposed OBP	GP	Proposed OBP
8 bits	2	8	4	1	1
	3	8	2	1	1
	4	8	2	1	1
	5	8	1	1	1
16 bits	2	16	8	1	1
	3	16	5	1	1
	4	16	4	1	1
	5	16	3	1	1
32 bits	2	32	16	1	1
	3	32	10	1	1
	4	32	8	1	1
	5	32	6	1	1
64 bits	2	64	32	1	1
	3	64	21	1	1
	4	64	16	1	1
	5	64	12	1	1

the data cells. Data bits can be stored on the higher positions and the parity bit can be stored on the lowest position in the same cell. In this case, equation (3) can be rewritten as:

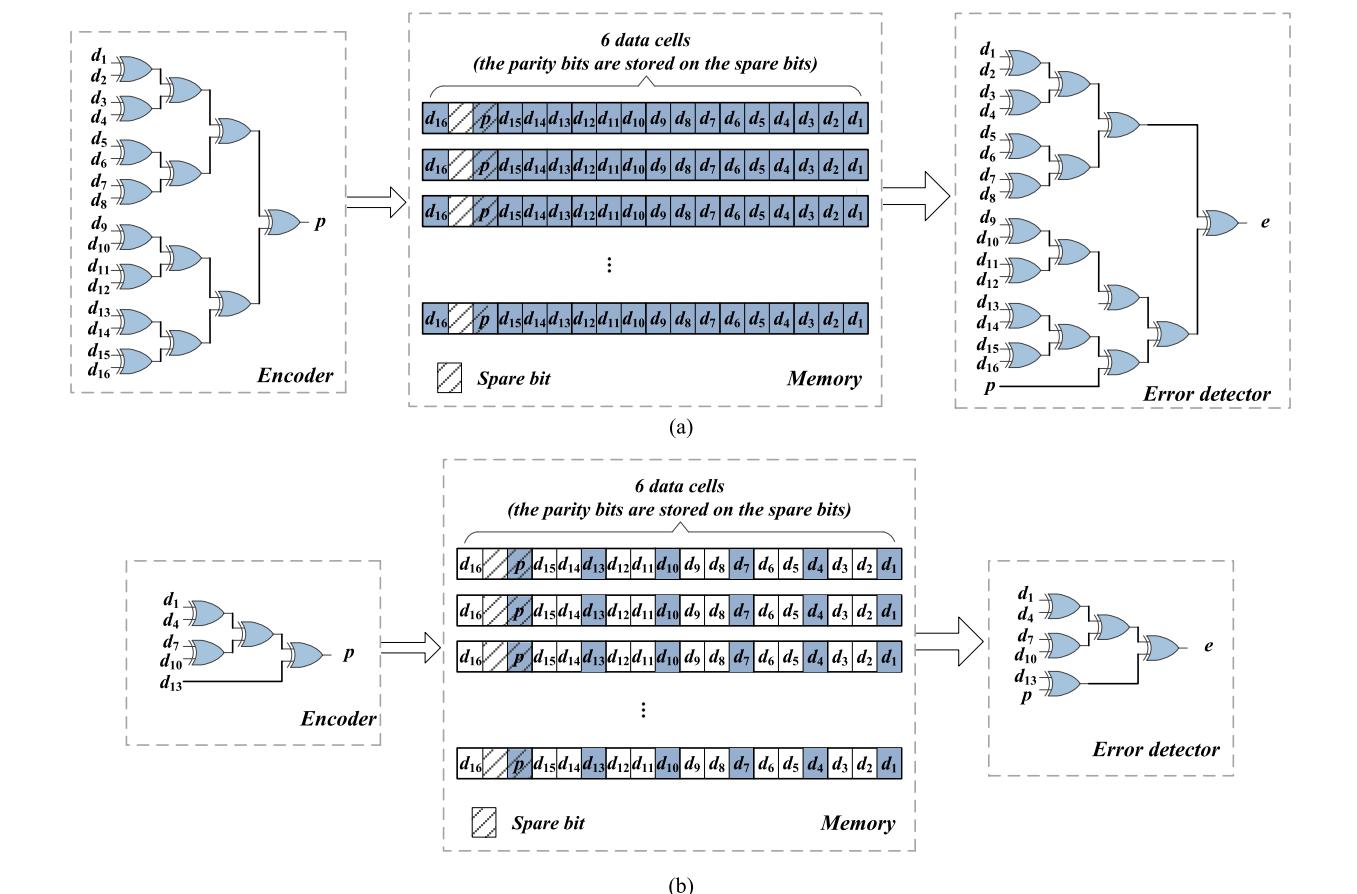


FIGURE 5. Implementation of different schemes to protect a 16-bit MLC memory with 3-bit cells: (a) the GP scheme; (b) the proposed OBP scheme.

$$p = d_{1,1} \oplus d_{2,1} \oplus \dots \oplus d_{k-1,1}. \quad (4)$$

Using equation (4), the parity bit does not check any data bits of the last cell; however, magnitude-1 errors affecting that cell can also be detected, because the parity bit is stored on the lowest position and is included in the syndrome generation process.

Compared to Gray coding combined with a single parity bit scheme (GP), the proposed OBP scheme requires a simpler parity check computation circuit. Table 2 shows the comparison for the number of inputs in the parity computation logic circuit, as well as the number of parity bits needed by different schemes when protecting memories for various data size and number of bits/cell configurations. Even though the two schemes use only one parity bit, the proposed OBP scheme saves 50-87.5 percent of the inputs, so reducing the hardware overhead of the encoder/error detector circuit implementations. The implementations of protecting a 16-bit MLC memory with 3-bit cells by using a traditional GP scheme and the proposed OBP scheme are shown in Figure 5; evaluation of the required circuitry is presented in Section IV.

C. TWO-BIT PARITY SCHEME (TBP)

The so-called Two-Bit Parity (TBP) scheme is proposed when targeting detection for both magnitude-1 and magnitude-2

TABLE 3. Number of inputs in the parity computation logic.

Data size	# bits /cell	# inputs		# parity bits	
		IP	Proposed TBP	IP	Proposed TBP
8 bits	2	4	4	2	2
	3	2 or 3	2 or 3	3	2
	4	2	2	4	2
	5	1 or 2	1	5	2
16 bits	2	8	8	2	2
	3	5 or 6	5	3	2
	4	4	4	4	2
	5	3 or 4	3	5	2
32 bits	2	16	16	2	2
	3	10 or 11	10 or 11	3	2
	4	8	8	4	2
	5	6 or 7	6	5	2
64 bits	2	32	32	2	2
	3	21 or 22	21	3	2
	4	16	16	4	2
	5	12 or 13	12 or 13	5	2

errors. The TBP scheme uses two parity bits p_1 and p_2 that cover the lowest and the second lowest bits in the cells respectively. p_1 is calculated per equation (3) or (4), as used for detecting all magnitude-1 errors in the memory cell; p_2 is given by:

$$p_2 = d_{1,2} \oplus d_{2,2} \oplus \dots \oplus d_{k-1,2} \oplus d_{k,2}. \quad (5)$$

Equation (5) is used for detecting all magnitude-2 errors. The proposed two parity checks can also be implemented using several *xor* gates. Also in this case, proper storing of the parity bits is required, i.e., to detect errors on the two parity bits, they need to be stored on the lowest and second lowest bits of a memory cell. It can be proved that at least two parity check bits are needed to detect all errors affecting a cell and therefore, the TBP scheme is optimal in terms of parity bits, i.e., a single parity check cannot detect all errors and thus at least two are needed. Consider a single parity check bit; the patterns to be considered are composed of consecutive bits and include the all ‘1’ pattern. Therefore, to detect them with a single parity check, it must check an odd number of bits (otherwise, the all ‘1’ pattern would not be detected). For example, a single parity check covers all three bits for pattern “111”. However, there are also detectable patterns that include all those bits except for several leftmost/rightmost bits such as the leftmost one (e.g., pattern “011”). For those patterns there is an even number of bits set in the parity check, which will not be detected. Therefore, the only option would be that a single bit is present on all detectable patterns; since this is not the case, at least two parity check bits are needed. Therefore, the TBP scheme is optimal in terms of parity check bits.

Compared to the IP scheme, the proposed TBP scheme has the following advantages.

- A smaller number of parity bits is needed for MLC memories with $b \geq 3$;

- A simpler *or* logic is used to generate the error detection signal.
- The implementation of the parity check circuit is simpler.

These features make the encoder and error detector circuits of the TBP scheme simpler than for the IP scheme. The first advantage results in a simpler parity computation circuit when the number of bits in each memory cell is equal or larger than 3 ($b \geq 3$), hence the overhead of the encoder/error detector can be reduced by using the proposed scheme. Table 3 shows the comparison for the number of inputs in the parity computation circuit and the number of parity bits needed by the different schemes. Evaluation for the circuitry implementation is provided in the next section. Moreover, this advantage may result in no overhead in terms of introducing additional memory cells for the parity bits for the case in which there are two or more spare bits in a cell (this aspect will also be analyzed in Section IV). The second and third advantages can further reduce the hardware overhead when implementing the error detection circuitry.

Figure 6 shows the implementation of protecting a 16-bit MLC memory with 3-bit cells by using the traditional IP scheme and the proposed TBP scheme; as just an example, the TBP scheme uses a smaller word length in the memory, as well as simpler encoder and error detection circuits.

Finally, it is worth noticing that the OBP (TBP) scheme can detect catastrophic faults only when they change the lowest (two lowest) bit(s).

IV. EVALUATION

The evaluation of the proposed OBP and TBP schemes is considered in this section; it consists of two parts: the overhead for memory and the encoder and error detector circuits. Data words of 8, 16, 32, 64-bit stored in MLC memories with 2, 3, 4, 5-bit cells are considered in the evaluation.

A. MEMORY OVERHEAD

In this subsection, the memory overhead in terms of word length (including the cells required by the proposed scheme to store the parity bits) is initially assessed and compared with the interleaved parity scheme. Tables 4 and 5 show the comparison results for the memory word lengths when utilizing different error detection schemes for MLC memories at different level configurations. For detecting magnitude-1 errors, the proposed OBP scheme has the same number of memory cells as the GP scheme. For detecting both magnitude-1 and magnitude-2 errors, the results in bold form are the cases in which the proposed TBP scheme incurs in no memory overhead because it saves one cell per word compared to the IP scheme. For example, when protecting 16-bit data stored in 3-bit cells, 6 cells are needed and two bits in the last cell are spare (as $16/3 = 5 + 1/3$). Therefore, no additional cell is needed by the TBP scheme, because the two parity bits can be stored in the positions of the spare two bits (whereas one additional cell is required by the IP scheme to store the three parity bits). In the other cases, the two

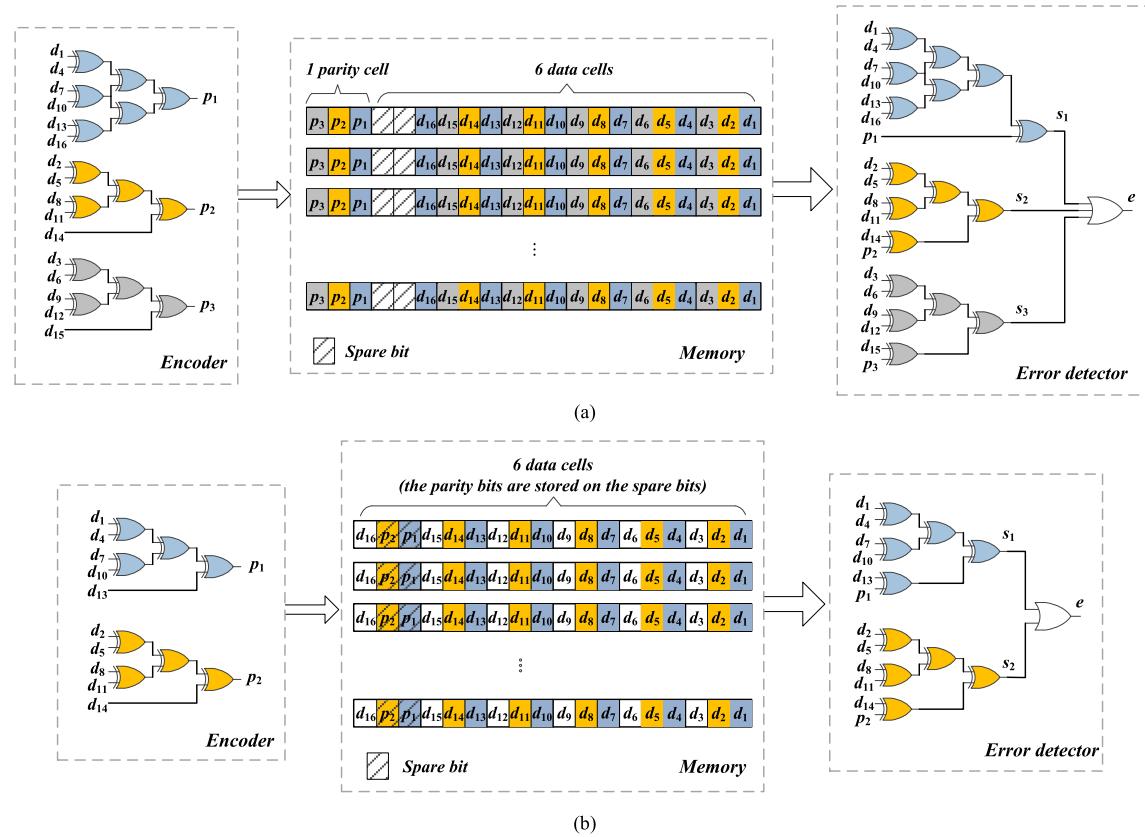


FIGURE 6. Implementation of different schemes to protect a 16-bit MLC memory with 3-bit cells: (a) the IP scheme; (b) the proposed TBP scheme.

schemes have the same memory overhead. This is a key advantage because in many cases, the memory has a large size and thus the provision of having additional cells on each word has a direct impact on the area and power consumption.

TABLE 4. Number of cells for different word sizes (magnitude-1 schemes).

Data size	# bits /cell	Word length (cells)	
		GP	Proposed OBP
8 bits	2	5	5
	3	3	3
	4	3	3
	5	2	2
16 bits	2	9	9
	3	6	6
	4	5	5
	5	4	4
32 bits	2	17	17
	3	11	11
	4	9	9
	5	7	7
64 bits	2	33	33
	3	22	22
	4	17	17
	5	13	13

B. ENCODER AND ERROR DETECTOR

As discussed previously, the proposed OBP and TBP schemes have a simpler encoder and error detection circuitry. This has been verified by implementing the two schemes and

TABLE 5. Number of cells for different word sizes (magnitude-2 schemes).

Data size	# bits /cell	Word length (cells)	
		IP	Proposed TBP
8 bits	2	5	5
	3	4	4
	4	3	3
	5	3	2
16 bits	2	9	9
	3	7	6
	4	5	5
	5	5	4
32 bits	2	17	17
	3	12	12
	4	9	9
	5	8	7
64 bits	2	33	33
	3	23	22
	4	17	17
	5	14	14

TABLE 6. Synthesis results for the encoder (magnitude-1 schemes).

Data size	# bits /cell	Area (μm^2)			Delay (ns)			Power (μW)		
		GP	Proposed OBP	Saving	GP	Proposed OBP	Saving	GP	Proposed OBP	Saving
8 bits	2	40.0	24.4	39.0%	0.28	0.21	25.0%	27.2	15.0	44.9%
	3	40.0	16.8	58.0%	0.28	0.14	50.0%	27.2	10.0	63.2%
	4	40.0	16.8	58.0%	0.28	0.14	50.0%	27.2	10.0	63.2%
	5	40.0	14.4	64.0%	0.28	0.11	60.7%	27.2	8.8	67.6%
16 bits	2	83.2	52.8	36.5%	0.39	0.27	30.8%	65.3	35.1	46.2%
	3	83.2	40.8	51.0%	0.39	0.25	35.9%	65.3	27.7	57.6%
	4	83.2	37.2	55.3%	0.39	0.21	46.2%	65.3	22.9	64.9%
	5	83.2	33.2	60.1%	0.39	0.20	48.7%	65.3	19.8	69.7%
32 bits	2	170.0	108.8	36.0%	0.41	0.39	4.9%	159.7	81.1	49.2%
	3	170.0	86.0	49.4%	0.41	0.33	19.5%	159.7	68.9	56.9%
	4	170.0	78.4	53.9%	0.41	0.27	34.1%	159.7	50.8	68.2%
	5	170.0	70.4	58.6%	0.41	0.26	36.6%	159.7	43.8	72.6%
64 bits	2	344.0	221.2	35.7%	0.48	0.42	12.5%	334.9	190.9	43.0%
	3	344.0	179.6	47.8%	0.48	0.39	18.8%	334.9	163.2	51.3%
	4	344.0	160.0	53.5%	0.48	0.38	20.8%	334.9	112.4	66.4%
	5	344.0	94.8	72.4%	0.48	0.33	31.3%	334.9	75.4	77.5%

TABLE 7. Synthesis results for the error detector (magnitude-1 schemes).

Data size	# bits /cell	Area (μm^2)			Delay (ns)			Power (μW)		
		GP	Proposed OBP	Saving	GP	Proposed OBP	Saving	GP	Proposed OBP	Saving
8 bits	2	43.6	28.0	35.8%	0.33	0.25	24.2%	29.9	17.8	40.5%
	3	43.6	20.4	53.2%	0.33	0.2	39.4%	29.9	11.9	60.2%
	4	43.6	20.4	53.2%	0.33	0.2	39.4%	29.9	11.9	60.2%
	5	43.6	16.8	61.5%	0.33	0.14	57.6%	29.9	10.0	66.6%
16 bits	2	87.2	56.4	35.3%	0.39	0.33	15.4%	68.8	37.8	45.1%
	3	87.2	44.8	48.6%	0.39	0.26	33.3%	68.8	30.1	56.3%
	4	87.2	40.8	53.2%	0.39	0.25	35.9%	68.8	27.7	59.7%
	5	87.2	37.2	57.3%	0.39	0.21	46.2%	68.8	22.8	66.9%
32 bits	2	174.0	112.8	35.2%	0.42	0.39	7.1%	161.2	84.4	47.6%
	3	174.0	89.6	48.5%	0.42	0.33	21.4%	161.2	70.4	56.3%
	4	174.0	82.0	52.9%	0.42	0.33	21.4%	161.2	53.5	66.8%
	5	174.0	74.4	57.2%	0.42	0.27	35.7%	161.2	46.4	71.2%
64 bits	2	347.6	225.2	35.2%	0.54	0.43	20.4%	349.0	180.6	48.3%
	3	347.6	183.2	47.3%	0.54	0.41	24.1%	349.0	132.9	61.9%
	4	347.6	160.0	54.0%	0.54	0.39	27.8%	349.0	112.4	67.8%
	5	347.6	148.8	57.2%	0.54	0.33	38.9%	349.0	97.2	72.1%

the GP and IP schemes in HDL and mapping the designs to a 65 nm library from TSMC using the Synopsis Design Compiler. The synthesis tool has been set to area and delay optimization in the circuitry to obtain the best results for these metrics. The synthesis results for the encoders and the error detectors of the proposed OBP and the GP schemes are given in Tables 6 and 7; the results for the proposed TBP and the IP schemes are given in Tables 8 and 9.

As in the previous results for the number of parity check bits of Tables 2 and 3, the synthesis results also show that the proposed schemes have the simplest encoder and error detection circuitry. From Tables 6 and 7, when targeting error

detection for magnitude-1 errors, the proposed OBP scheme can significantly reduce the overhead of the encoder and error detector in all cases. For example, in the case of 8-bit data stored in 3-bit cells, the OBP scheme can save 58.0 percent of the area, 50.0 percent of the delay and 63.2 percent of the power consumption in the encoder circuitry, and 53.2 percent of the area, 39.4 percent of the delay and 60.2 percent of the power consumption in the error detector circuitry. Figures 7 and 8 plot the area and PDP (i.e., the Power Delay Product) reductions of the proposed OBP scheme to the GP scheme for different memories. When targeting error detection for both magnitude-1 and

TABLE 8. Synthesis results for the encoder (magnitude-2 schemes)

Data size	# bits /cell	Area (μm^2)			Delay (ns)			Power (μW)		
		IP	Proposed TBP	Saving	IP	Proposed TBP	Saving	IP	Proposed TBP	Saving
8 bits	2	36.0	36.0	0.0%	0.22	0.22	0.0%	22.1	22.1	0.0%
	3	32.0	24.4	23.8%	0.20	0.20	0.0%	18.1	14.6	19.3%
	4	28.8	20.8	27.8%	0.14	0.14	0.0%	16.3	12.1	25.8%
	5	28.0	16.0	42.9%	0.14	0.11	21.4%	16.2	9.8	39.5%
16 bits	2	80.0	80.0	0.0%	0.27	0.27	0.0%	54.3	54.3	0.0%
	3	75.2	56.0	25.5%	0.26	0.25	3.8%	48.1	35.7	25.8%
	4	72.0	48.8	32.2%	0.22	0.22	0.0%	44.1	31.9	27.7%
	5	67.6	40.8	39.6%	0.22	0.20	9.1%	39.5	27.8	29.6%
32 bits	2	166.4	166.4	0.0%	0.39	0.39	0.0%	130.3	130.3	0.0%
	3	162.8	124.4	23.6%	0.33	0.33	0.0%	119.8	87.9	26.6%
	4	160.0	105.6	34.0%	0.27	0.27	0.0%	108.5	79.0	27.2%
	5	155.2	89.6	42.3%	0.27	0.26	3.7%	98.3	69.2	29.6%
64 bits	2	340.0	340.0	0.0%	0.46	0.46	0.0%	319.4	319.4	0.0%
	3	334.0	256.8	23.1%	0.44	0.43	2.3%	246.3	193.5	21.4%
	4	332.8	217.6	34.6%	0.39	0.39	0.0%	245.1	181.9	25.8%
	5	330.4	191.2	42.1%	0.39	0.38	2.6%	243.2	176.1	27.6%

TABLE 9. Synthesis results for the error detector (magnitude-2 schemes)

Data size	# bits /cell	Area (μm^2)			Delay (ns)			Power (μW)		
		IP	Proposed TBP	Saving	IP	Proposed TBP	Saving	IP	Proposed TBP	Saving
8 bits	2	44.8	44.8	0.0%	0.30	0.30	0.0%	30.1	30.1	0.0%
	3	46.0	33.6	27.0%	0.25	0.25	0.0%	30.5	20.7	32.1%
	4	46.0	29.6	35.7%	0.26	0.23	11.5%	30.5	17.5	42.6%
	5	48.0	22.4	53.3%	0.27	0.19	29.6%	34.6	13.2	61.8%
16 bits	2	88.8	88.8	0.0%	0.36	0.36	0.0%	69.9	69.9	0.0%
	3	89.6	65.6	26.8%	0.31	0.30	3.2%	70.7	42.9	39.3%
	4	89.2	57.6	35.4%	0.33	0.27	18.2%	70.5	37.0	47.5%
	5	91.6	50.4	45.0%	0.34	0.25	26.5%	70.4	31.8	54.8%
32 bits	2	176.0	176.0	0.0%	0.44	0.44	0.0%	163.4	163.4	0.0%
	3	176.8	133.6	24.4%	0.38	0.36	5.3%	165.1	99.6	39.7%
	4	177.2	114.4	35.4%	0.41	0.34	17.1%	167.8	88.6	47.2%
	5	179.6	99.2	44.8%	0.42	0.31	26.2%	170.0	75.8	55.4%
64 bits	2	349.6	349.6	0.0%	0.50	0.50	0.0%	354.8	354.8	0.0%
	3	347.2	265.6	23.5%	0.46	0.44	4.3%	345.3	203.8	41.0%
	4	351.6	227.2	35.4%	0.43	0.40	7.0%	370.9	195.7	47.2%
	5	354.8	200.8	43.4%	0.44	0.38	13.6%	388.6	188.8	51.4%

magnitude-2 errors, from Tables 8 and 9 the TBP scheme is significantly better than the IP scheme when applied to MLC memories with $b \geq 3$. For example, when the TBP scheme is used for an 8-bit data word stored in 5-bit cells, 42.9 percent of the area, 21.4 percent of the delay and 39.5 percent of the power consumption can be reduced in the encoder circuitry, and 53.3 percent of the area, 29.6 percent of the delay and 61.8 percent of the power consumption can be reduced in the decoder circuitry. Moreover, the parity computation circuit for the proposed TBP scheme is simpler in some cases due to the fewer number of data bits. For example, in the case of 16-bit data with 5-bit cells, each parity bit of the proposed

scheme just covers three data bits, while one parity bit of the IP scheme covers four, thus resulting in a larger critical path in the circuitry. Figures 9 and 10 plot the area and PDP reductions of the proposed TBP scheme to the IP scheme for different memories.

Savings in terms of the encoder and error detection overhead increase significantly with a larger value of b . The causes are twofold: (a) the number of inputs in the parity computation logic needed for the proposed OBP reduces while for the GP scheme it remains constant; (b) the number of parity bits needed for the proposed TBP scheme is the same (i.e., only two), but it increases for the IP scheme.

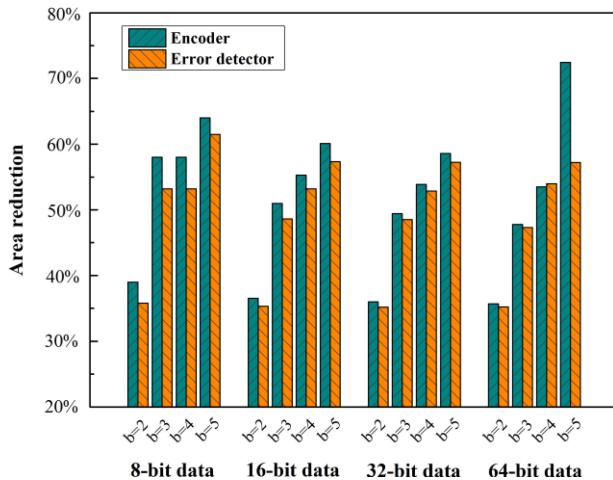


FIGURE 7. Area reduction for the encoder and error detector of the magnitude-1 schemes (GP vs proposed OBP).

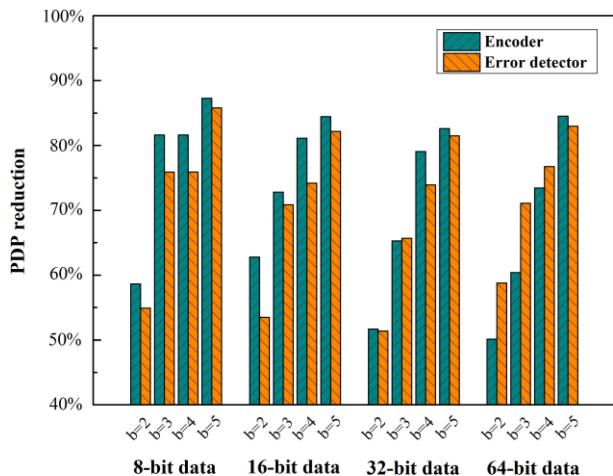


FIGURE 8. PDP reduction for the encoder and error detector of the magnitude-1 schemes (GP vs proposed OBP).

Overall, the proposed two schemes can efficiently detect limited magnitude errors in a single cell for MLC memories; they introduce a significant lower overhead in terms of area, delay and power consumption than for traditional schemes.

V. CONCLUSION

In this paper, two new schemes, namely One-Bit Parity (OBP) and Two-Bit Parity (TBP), have been presented to accomplish limited magnitude error detection in Multilevel Cell memories (with a binary mapping of levels to bits) using emerging technologies. The proposed schemes exploit the bit error patterns introduced by the limited magnitude errors to simplify the error detection circuitry and in the case of the TBP scheme also reduce the number of parity check bits in some configurations. The proposed schemes have been implemented and compared to existing schemes. For the OBP scheme, the comparison has been made against a single parity check combined with a Gray coding mapping of levels to bits. The results have shown that the OBP scheme significantly reduces the encoding and detection circuitry in terms of area, power and delay. For the TBP

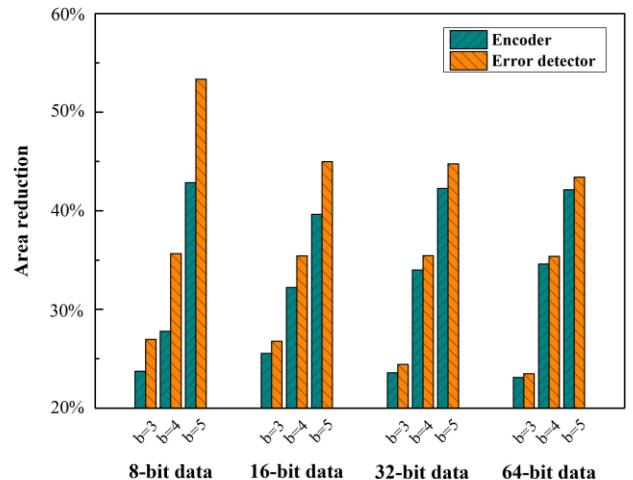


FIGURE 9. Area reduction for the encoder and error detector of the magnitude-2 schemes (IP vs proposed TBP).

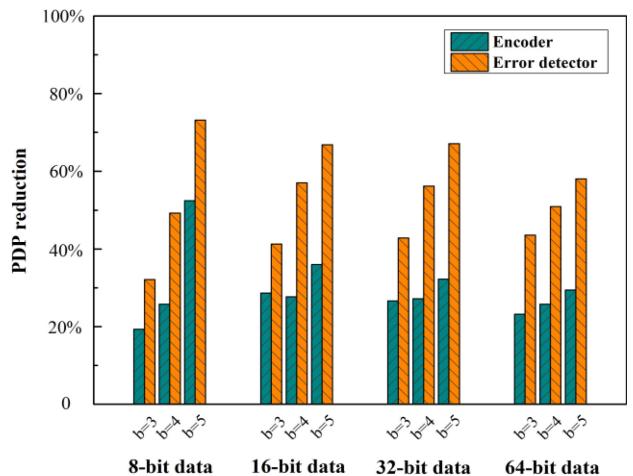


FIGURE 10. PDP reduction for the encoder and error detector of the magnitude-2 schemes (IP vs proposed TBP).

scheme, an interleaved parity has been used as the reference implementation. In this case, the TBP scheme not only reduces the encoding and detection circuitry but in some configurations, it also needs a smaller number of parity check bits. This leads to savings in the number of memory cells per word for some commonly used data word lengths. Therefore, the OBP and TBP schemes are an attractive option to perform detection of limited magnitude errors in emerging MLC memories.

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SHANSHAN LIU (M'19) received the MS and PhD degrees in microelectronics and solid-state electronics from the Harbin Institute of Technology, Harbin, China, in 2012 and 2018, respectively. She is currently a post-doctoral researcher with the Department of Electrical and Computer Engineering, Northeastern University, Boston, US. Her current research interests include fault tolerant design in high performance computer systems. She is a member of the IEEE.



PEDRO REVIRIEGO (M'04-SM'15) received the MSc and PhD degrees in telecommunications engineering from the Technical University of Madrid, Madrid, Spain, in 1994 and 1997, respectively. From 1997 to 2000, he was an R&D Engineer with Teldat, Madrid, working on router implementation. In 2000, he joined Massana to work on the development of 1000BaseT transceivers. From 2004 to 2007, he was a distinguished member of Technical Staff with the LSI Corporation, working on the development of Ethernet transceivers. From 2007 to 2018 he was with Nebrija University. He is currently with Universidad Carlos III de Madrid working on high speed packet processing and fault tolerant electronics. He is a senior member of the IEEE.



FABRIZIO LOMBARDI (M'81-SM'02-F'09) received the BSc degree (Hons.) in electronic engineering from the University of Essex, United Kingdom, in 1977, the master's degree in microwaves and modern optics and the diploma degree in microwave engineering from the Microwave Research Unit, University College London, in 1978, and the PhD degree from the University of London, in 1982. He is currently the International Test Conference (ITC) Endowed Chair Professorship with Northeastern University, Boston, USA. His research interests are bio-inspired and nano manufacturing/computing, VLSI design, testing, and fault/defect tolerance of digital systems. He has extensively published in these areas and coauthored/edited seven books. He was the editor-in-chief of the *IEEE TRANSACTIONS ON COMPUTERS* from 2007 to 2010 and the inaugural editor-in-chief of the *IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING* from 2013 to 2017. He is the editor-in-chief of the *IEEE TRANSACTIONS ON NANOTECHNOLOGY*.