BENNETT UNIVERSITY
A TIMES GROUP INITIATIVE

ECSE108L Digital Design

Lecture 1

Course Overview

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Administration

- Faculty: Dr. Vipul Mishra, Dr. Tanmay, Dr. Akash Yadav
- Web site: LMS
- Lecture and lecture slides
  - Available the same day after lecture
- Discussion Time: Anytime except when we have class or laboratory (prior email is preferable).
- Easiest way to get a good grade in ECSE104 is to attend the class and pay attention.
- Minimum 35 Marks are required to pass this course.

Course Grading (Evaluation Component)

- Midterm-1: 20%
- End-term: 35%
- Quiz: 15%
- Home Assignment- 10%
- Lab Continuous Evaluation: 10%
- Lab Viva: 10%

Course Structures

Week	Content	Week	Content
1	Data Representation	8	Counters
2	Truth Table	9	Design of state machines
3	K-Map	10	Read-only Memory
4	Multiplexers	11	PLA's and its applications
5	ALU Design Examples	12	Introduction to different logic families;
6	Sequential Circuits	13	Advanced Topics
7	Flip-Flops	14	Advanced Topics

Textbook: **Digital Design: with an Introduction to the Verilog HDL – 2014 by M. Morris Mano**

References:	**1. Digital Design and Computer Architecture, 2nd ed.," by D. M. Harris and S. L. Harris (Morgan Kaufmann, 2012).** **2. Verilog HDL: A Guide to Digital Design and Synthesis, 2nd ed.," by S. Palnitkar (Prentice Hall, 2003)**

Laboratory

- In this course students will start with basic digital components such as Arithmetic and logical operation, Memory etc. Then finally design soft IP.
- Language: Verilog
- Laboratory Evaluation (20%)
  - Continuous Evaluation
  - Viva (2)

WhatsApp

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https://chat.whatsapp.com/DDzYoxZbGKsERKncyttqvX

Join my WhatsApp group.

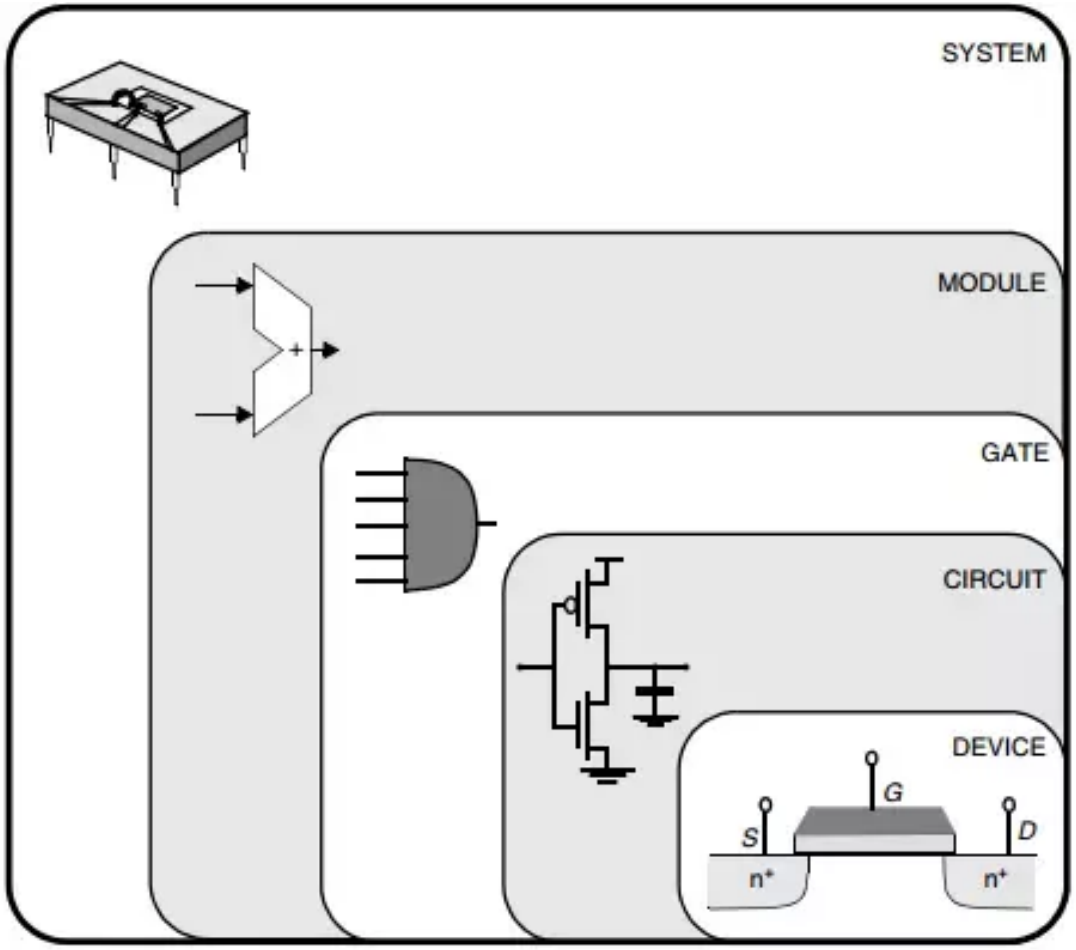
https://chat.whatsapp.com/G2NV4AM8oO636lnHafaDOM

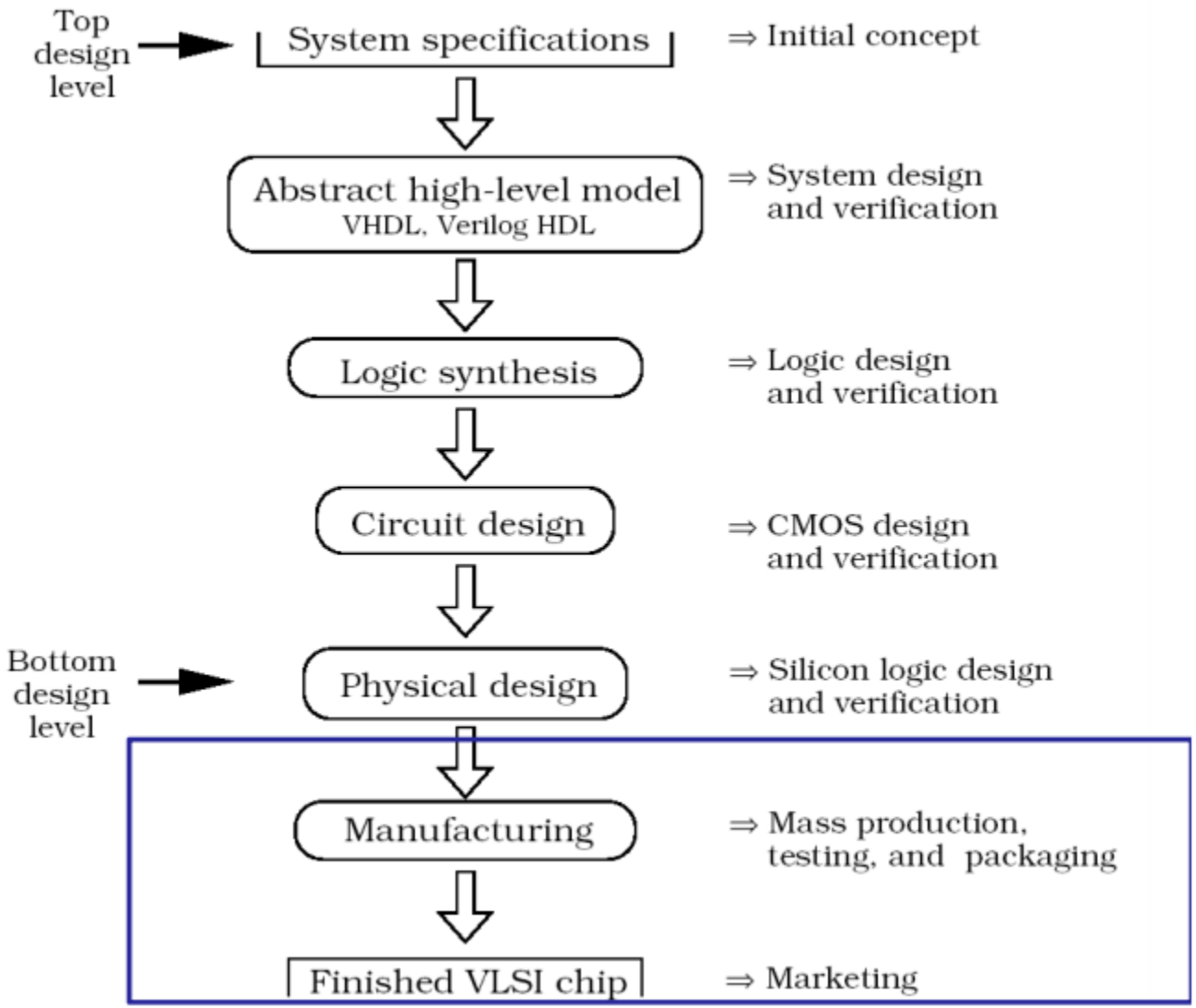
Digital System

Benefit of Digital over Analog

- Lesser Loss in transmission
- Lesser costly

System Design Levels




Top design level
System specifications
⇒ Initial concept
Abstract high-level model
VHDL, Verilog HDL
⇒ System design and verification
Logic synthesis
⇒ Logic design and verification
Circuit design
⇒ CMOS design and verification
Bottom design level
Physical design
⇒ Silicon logic design and verification
Manufacturing
⇒ Mass production, testing, and packaging
Finished VLSI chip
⇒ Marketing