ECSE108L - Digital Design

Course Type - Core L-T-P Format 3-0-2 Credits - 4

COURSE SUMMARY

This course explains the elements of digital system abstractions such as digital representations of information, digital logic, Boolean algebra, state elements and finite state machine (FSMs). Design basic components of digital systems which includes combinational and sequential circuits. Utilize these basic components to design digital systems using tools like Quartus, Xilinx ISE and implement in FPGA.

COURSE-SPECIFIC LEARNING OUTCOMES (CO)

CO1: Understand and examine the structure of various number systems and its application in digital design.

CO2: Create the appropriate truth table and gate level implementation from a description of a combinational logic function.

CO3: Draw a circuit diagram for a sequential logic circuit and analyze its timing properties (input setup and hold times, minimum clock period, output propagation delays).

Detailed Syllabus

Module 1 (Contact hours: 12)

Digital Systems; Data representation and coding; Logic circuits, integrated circuits; Analysis, design and implementation of digital systems; Introduction of CAD tools. Application of electric circuits, analog and digital electronics; Number system; Representation of signed numbers; Fixed and floating-point numbers; BCD; Gray codes; parity check codes and Hamming code; Definition and specification; Truth table; Basic logic operation and logic gates. Basic Boolean algebra; Standard representation and simplification of logic functions - K-map and tabular methods. Decoders, encoders, multiplexers, de multiplexers and their applications; Parity circuits and comparators.

Module 2 (Contact hours: 12)

Arithmetic modules-adders, CLA, multiplier, subtractors ALU Design examples. Definition of state machines, state machine as a sequential controller; Basic sequential circuits- latches and flip-flops: SR-latch, D-latch, Edge trigger and level trigger; D flip-flop, JK flip-flop, T flip-flop; Timing hazards and races; Analysis of state machines using D flip-flops and JK flip-flops; Multi-bit latches and registers, counters, shift register, application examples.

Module 3 (Contact hours: 9)

Design of state machines - state table, state assignment, transition/excitation table, excitation maps and equations, logic realization; Read-only memory, PROM, read/write memory - SRAM and DRAM PLAs, PALs and their applications; Sequential PLDs and their applications.

Module 4 (Contact hours: 9)

Designing state machine using ASM charts; Designing state machine using state diagram; Design examples State-machine design with sequential PLDs; Introduction to different logic families; TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation; propagation delay, transition time, power consumption and power-delay product.

STUDIO WORK / LABORATORY EXPERIMENTS:

In this course students will start with basic digital components such as Arithmetic and logical operation, Memory etc. Then finally design soft IP. The Lab will use Altera Quartus prime Lite tool for design and FPGA Altera DEII utilize for physical implementation.

TEXTBOOKS/LEARNING RESOURCES:

a) M. Morris Mano, Digital Design: with an Introduction to the Verilog HDL, VHDL and System VErilog (6^{th} ed.), Pearson, 2018. ISBN 978-0134549897.

b) Materials, videos and instructions will be provided by instructors.

REFERENCE BOOKS/LEARNING RESOURCES:

a) D. M. Harris and S. L. Harris, Digital Design and Computer Architecture (2^{nd} ed.), Morgan Kaufmann, 2012. ISBN 978-0123944245.

b) S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis (2^{nd} ed.), Prentice Hall, 2003. ISBN 978-0132599702.