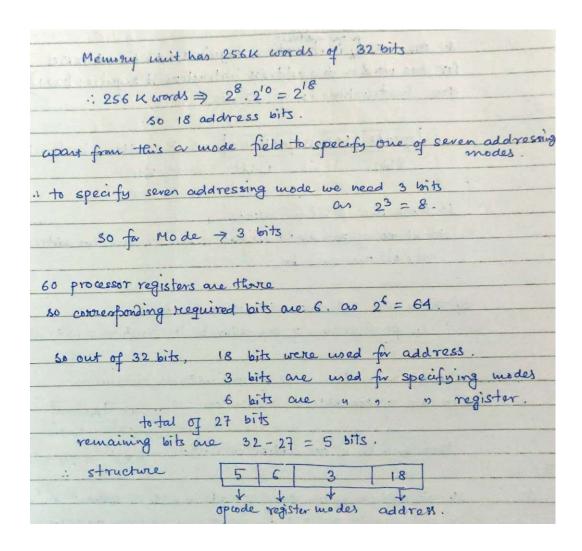
Practice Set 02

1. The memory unit of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields: an operational code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.



- 2. A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
 - a. How many bits are there in the tag, index, block, and word fields of the address format?
 - b. How many bits are there in each word of cache including a valid bit?
 - c. How many blocks can the cache accommodate?

Ma	2 morey unit of 64K × 16.
	≥ 2 ⁶ ·2 ¹⁰ × 16
	> 216 × 16
	so 16 bit address, 16 bit data
	cache uses direct mapping of block size of four words.
A .	for four words address bit required 2[22=4].
	cache memory size = 1 K = 210.
a.	to total address lines = 10.
	so total address lines = 10. for words, address lines = 2.
	: for block, address lines = 10-2=8.
	111 11mgs limes = 16.
	total address lines = 16.
	so no. of hits for tag field = 16 - (2+8) = 6.
	so memory structure tag block word
	6 8 2
	Index = 8+2=10
Ь.	there are 6 bits for tag
	1 bit for valid bit valid tag datar
	1 bit for valid bit Valid tag datar 16 bit of datar 1 6 16=23
	so there are 23 bits in each word of cache.
	= block c ON 28 = 256.
٥.	cache can accommodate no of blocks as $2^8 = 256$.
	256 blocks of four words each.