

Practice Set 02

1. The memory unit of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields: an operational code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.

Memory unit has 256K words of 32 bits.

$\therefore 256 \text{ K words} \Rightarrow 2^8 \cdot 2^{10} = 2^{18}$
So 18 address bits.

apart from this a mode field to specify one of seven addressing modes.

\therefore to specify seven addressing mode we need 3 bits
as $2^3 = 8$.

So for Mode $\rightarrow 3$ bits.

60 processor registers are there
so corresponding required bits are 6. as $2^6 = 64$.

So out of 32 bits, 18 bits were used for address.
3 bits are used for specifying modes
6 bits are " " " register.

total of 27 bits
remaining bits are $32 - 27 = 5$ bits.

\therefore structure

5	6	3	18
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opcode register modes address.

2. A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

- How many bits are there in the tag, index, block, and word fields of the address format?
- How many bits are there in each word of cache including a valid bit?
- How many blocks can the cache accommodate?

Memory unit of $64K \times 16$
 $\Rightarrow 2^6 \cdot 2^{10} \times 16$
 $\Rightarrow 2^{16} \times 16$
 so 16 bit address, 16 bit data
 cache uses direct mapping of block size of four words.
 for four words address bit required $2[2^2=4]$

a. cache memory size = $1K = 2^{10}$.
 so total address lines = 10.
 for words, address lines = 2.
 \therefore for block, address lines = $10 - 2 = 8$.
 total address lines = 16.
 so no. of bits for tag field = $16 - (2+8) = 6$.

so memory structure

tag	block	word
6	8	2

Index = $8+2=10$

b. there are 6 bits for tag
 1 bit for valid bit
 16 bit of data

valid	tag	data
1	6	16

$1+6+16=23$
 so there are 23 bits in each word of cache.

c. cache can accommodate no. of blocks as $2^8 = 256$.
 256 blocks of four words each.