Dept. of CSE, Bennett University

ECSE217L – Microprocessor and Computer Architecture Lab

Assignment – 1

In this lab, you will learn how Logisim works and will simulate some sample blocks.This will help you learn more about digital system design.

Logisim is an educational tool for designing and simulating digital logic circuits. It is simple enough to assist understanding the most basic principles connected to logic circuits, with its simple toolbar interface and simulation of circuits as you design them. In the previous sem, you implemented the digital design circuits using Verilog programming, Logisim will help you to give a design view.

Logisim (http://www.cburch.com/logisim/) is a Java application, it can be obtained from http://sourceforge.net/projects/circuit/.

Simply download and run it (tutorial is available help->tutorial).

Learn the interface of the software and learn how basic gates works, how to giveinput and output signals.

1. Suppose the equation **Y = ABC' + BD' + C** represents a combinational circuit with 4 inputs and one output. Implement the following combinational circuit using basic gates and verify the outputwith a truth table. Truth Table can be generated using tool itself.

2. Implement the following Product of Sum expression using basic gates in Logisim and verify the functionality using truth table.

    - **Y = ((A+B).(C+D+E))'**

3. Use basic logic gates to design a 4:1 MUX using Logisim and verify with truth table.
4. Implement XOR gate using any universal gate representation.
5. Implement XNOR gate using basic gates as well as universal gates.

[note: Don't use same universal gate In Q4 and Q5]

Submission Instructions:

- Submit your .circ file from LMS within given timeline. Save all the filesas per the format RollNo_Lab#_QuestionNo.circ (Example: E19CSE632_Lab1_Q2.circ). Make a .zip file and upload.
- Write your Name and Roll No in the design itself. Without this you will scorezero for that particular question.
- Provide label for all the input and output.
- Late submission will lead to penalty.