Practice Set 3

1. What is RISC Pipeline? Explain Delayed Load for the following four instruction:

   LOAD: R1<- M[Address1]

   LOAD: R2<- M[Address2]

   ADD: R3<- R1 + R2

   STORE: M[Address3] <- R3

   Explain Delayed Branch for the following set of instructions:

   LOAD from Memory to R1

   Increment R2

   Add R3 to R4

   Subtract R5 from R6

   Branch to address X

   Next instruction in X

2. Consider the following four instructions in the following program. Suppose that the first instruction starts from step 1. Specify the operations that will be performed in the four segments (consider you are using four-segment instruction pipeline) during step 4.

   LOAD R1<- M[321]

   ADD R2<-R2+M[313]

   INC R3<-R3+1

   STORE M[314]<-R3

3. Show how the increment operation from the above instructions can create data hazards in the three segment RISC pipeline.

4. Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40 ns. How long will it take to perform 400 floating point operations? Is there a difference if the same 400 operations are carried out using a single pipeline processor with a cycle time of 10 ns?

5. A weather forecasting computation requires 250 billion floating-point operations. The problem is processed in a supercomputer that can perform 100 megaflops. How long will it take to these calculations?