Practice Set – Pipeline 1

1. In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i = 1 through 6.

2. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

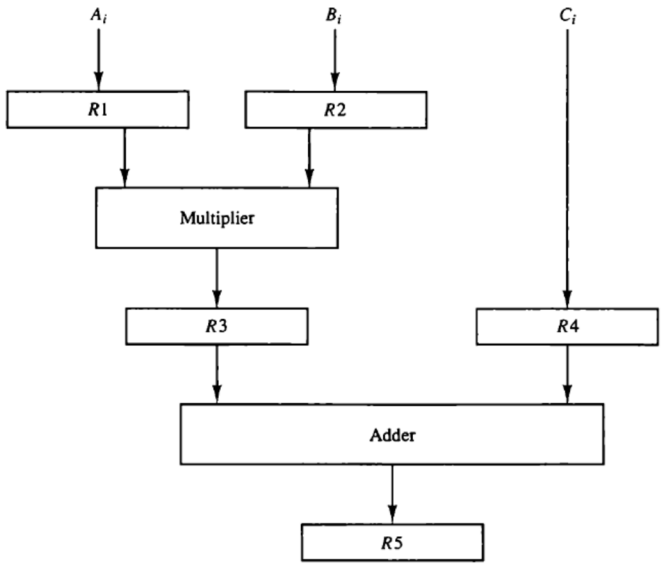
3. Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.

4. A nonpipelined system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns.

   a. Determine the speedup ratio of the pipeline for 100 tasks.

   b. What is the maximum speedup that can be achieved?

5. The pipeline of following figure has the following propagation times: 40 ns for the operands to be read from memory into registers R1 and R2, 45 ns for the signal to propagate through the multiplier, 5 ns for the transfer into R3, and 15 ns to add the two numbers into R5. Consider there are 3 segments for pipelined unit.



   a. What is the minimum clock cycle time that can be used?

   b. A nonpipelined system can perform the same operation by removing R3 and R4. How long will it take to multiply and add the operands without using the pipeline?

   c. Calculate the speedup of the pipeline for 10 tasks and again for 100 tasks.

   d. What is maximum speedup that can be achieved?

6. The time delay of a four-segment pipelined unit are as follows: t_1 = 50 ns, t_2 = 30 ns, t_3 = 95 ns, and t_4 = 45 ns. The interface register's delay time t_r = 5 ns. How long would it take to complete 100 tasks in the pipeline?