COURSE PLAN

For

Microprocessor and Computer Architecture (ECSE217L)

Faculty Name : Tanmay Bhowmik, Ishan Budhiraja, Bishwajit Roy

Course Type : Core

Semester and Year: III Semester and II Year

L-T-P : 3-0-2

Credits : 4

Department : Computer Science Engineering

Course Level : UG

SCHOOL OF ENGINEERING AND APPLIED SCIENCES

Department of Computer Science Engineering

Bennett University

Greater Noida, Uttar Pradesh

COURSE CONTEXT

SCHOOL	**SEAS**	**VERSION NO. OF CURRICULUM/SYLLABUS THAT THIS COURSE IS A PART OF**	**Version 2**
DEPARTMENT	**CSE**	**DATE THIS COURSE WILL BE EFFECTIVE FROM**	**Jul-Dec, 2020**
DEGREE	**B. Tech.**	**VERSION NUMBER OF THIS COURSE**	**Version 1**

COURSE BRIEF

COURSE TITLE	**Microprocessor and Computer Architecture**	**PRE-REQUISITES**	**NA**
COURSE CODE	**ECSE217L**	**TOTAL CREDITS**	**4**
COURSE TYPE	**Core**	**L-T-P FORMAT**	**3-0-2**

COURSE SUMMARY

ALU, Instruction set, CPU design, Micro-operation and their RTL specification, CPU-memory interaction, I/O processing, Programmed controlled I/O transfer, Interrupt controlled I/O transfer, DMA controller, RISC and CISC paradigm, to pipelining and pipeline hazards, design issues of pipeline architecture, interconnection networks, Multiprocessors and its characteristics, models of memory consistency Architecture of Microprocessors, Overview of microprocessor, Signals and pins of microprocessor, Assembly language and interfacing with microprocessor.

COURSE-SPECIFIC LEARNING OUTCOMES (CO)

By the end of this program, students should have the following knowledge, skills and values:

CO1: Understand about modern architecture and microprocessors and the design techniques used to increase their performance.

CO2: Evaluate various design alternative of computer architecture based on CPU performance, memory, I/O.

CO3: Create new designs at the register-transfer-level.

How are the above COs aligned with the Program-Specific Objectives (POs) of the degree?

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Detailed Syllabus

Module 1 (Contact hours: 12)

Arithmetic and Logic Unit, Introduction to memory Unit, control unit and Instruction Set, working with an ALU, Various addressing modes and designing of an Instruction set, Concepts of subroutine and subroutine call. Introduction to CPU design, Instruction interpretation and execution, Micro-operation and their RTL specification; Concepts of semiconductor memory, CPU- memory interaction, organization of memory modules.

Module 2 (Contact hours: 12)

Cache memory and related mapping and replacement policies, Virtual memory Introduction to input/output processing, working with video display unit and keyboard and routine to control them, programmed controlled I/O transfer Interrupt controlled I/O transfer, DMA controller, Secondary storage and type of storage devices, Introduction to buses and connecting I/O devices to CPU and memory; Introduction to RISC and CISC paradigm, Design issues of a RISC processor and example of an existing RISC processor, introduction to pipelining and pipeline hazards.

Module 3 (Contact hours: 9)

Design issues of pipeline architecture, Instruction level parallelism and advanced issues Introduction to interconnection network and practical issues., Examples of interconnection networks; Multiprocessors and its characteristics, Memory organization for multiprocessors systems, synchronization and models of memory consistency, Issues of deadlock and scheduling in multiprocessor systems.

Module 4 (Contact hours: 9)

Cache in multiprocessor systems and related problems, Cache coherence protocols, Parallel processing concepts, Parallelism algorithm for multiprocessor systems; General definitions of mini computers, microprocessors, micro controllers and digital signal processors, Overview of microprocessor, Signals and pins of microprocessor; Overview of microprocessor, Signals and pins of microprocessor.

STUDIO WORK / LABORATORY EXPERIMENTS:

In this course students will start with basic components of CPU such as ALU, Memory etc. Then finally combine all components and develop a processor. The Lab will use Logisim for design. MIPS for assembly programming.

TEXTBOOKS/LEARNING RESOURCES:

1. J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach* (5th ed.), Morgan Kaufmann, 2012. ISBN 978-9381269220.

2. William Stallings, *Computer Organization and Architecture* (9th Edition), Pearson, 2012. ISBN- 978-0132936330.

3. Morris Mano, *Computer System Architecture* (3rd Edition), Pearson, 2017, ISBN-13: 978-9332585607

REFERENCE BOOKS/LEARNING RESOURCES:

1. D. M. Harris and S. L. Harris, *Digital Design and Computer Architecture* (2nd Edition), Morgan Kaufmann, 2012. ISBN-978-0123944245.
2. M. Morris Mano, *Digital Design: with an Introduction to the Verilog Hdl* (5th Edition), Pearson Education, 2014. ISBN-978-9332535763.
3. S. Palnitkar, Verilog HDL: *A Guide to Digital Design and Synthesis* (2nd Edition), Prentice Hall, 2003. ISBN- 978-0132599702.
4. Andrew N. Sloss, ARM System Developer's Guide, Morgan Kaufmann publications (2004).

MOOC COURSE:

1. https://www.coursera.org/learn/comparch
2. https://www.edx.org/course/computer-architecture?index=product&queryID=fc0b5539ef8a0c814810877ad4718991&position=1

EVALUATION POLICY:

Components of Course Evaluation	Percentage
Quiz	20
Mid Term Examination	15
End Term Examination	35
Project Demonstration	10
End Term Lab Exam	20

Lecture Wise Plan:

Lecture No.	Content Planned
1	Overview of microprocessor, Signals and pins of microprocessor
2	Description of Instructions
3	Assembly directives
4	Various addressing modes
5	Designing of an Instruction set
6	Assembly software programs with algorithms
7	Concepts of subroutine and subroutine call
8	Introduction to CPU design
9	Instruction interpretation and execution
10	Micro-operation and their RTL specification
11	Concepts of memory
12	CPU- memory interaction,
13	Memory organization
Quiz 1	
14	Cache memory and related mapping
15	replacement policies
16	Virtual memory

17	Introduction to input/output processing
18	working with video display unit and keyboard and routine to control them,
19	Programmed controlled I/O transfer
20	Interrupt controlled I/O transfer
Mid Term Exam	
21	Overview of Processors used in 5G and 6G smartphones
22	Qualcomm Snapdragon: Snapdragon Family Series
23	Apple, Exynos, Mediatek
24	DMA controller (Self Study)
25	Introduction to buses and connecting I/O devices to CPU and memory
26	Introduction to RISC and CISC paradigm
27	Design issues of a RISC processor and example of an existing RISC processor
28	introduction to pipelining and pipeline hazards
29	Design issues of pipeline architecture
30	Instruction level parallelism
31	Introduction to interconnection network and practical issues
32	Multiprocessors and its characteristics (Self Study)
Quiz 2	
33	Memory organization for multiprocessors systems
34	synchronization and models of memory consistency
35	Cache in multiprocessor systems and related problems
36	Cache coherence protocols, Parallel processing concepts
37	General definitions of mini computers, microprocessors, micro controllers and digital signal processors
38	Introduction to memory Unit, control unit and Instruction Set,
39	Working with an ALU
40	Interfacing with RAMs, ROMs
41	Interfacing with peripheral ICs
42	Interfacing with key boards, LEDs, LCDs, ADCs, and DACs
End Term Exam	

Lab Plan

Lab No.	Content Planned
1	Familiarise with Logisim and simulate some blocks
2	Designing of combinational logic circuits using Logisim
3	Designing of sequential logic circuits using Logisim
4	Introduction to Assembly Language programming with MIPS Simulator
5	Implementation of different Arithmetic operations in MIPS Simulator
6	MIPS Logical, Conditional Instructions
7	Conditional and Unconditional branch instructions
8	Project Demonstration
9	Taking User Input in Assembly code
10	Assembly loop control structure, Array Declaration in MIPS Simulator
11	ARM instruction set and Thumb Instruction set.
12	ARM Programming
13	Designing of memory and CPU circuits using Logisim,

14	End Term Lab Exam

7. Suggest at least 3 innovations how this will enhance learning outcome of the course.

(i) Apart from the regular syllabus, some latest microprocessor chips, like qualcomm snapdragon, apple, Exynos, Mediatek will be taught thus students get familiarize with the latest microprocessor chips which are used in widely used smartphones and other electronic gadgets.

(ii) Three different tools will be introduced in Lab thus students gain idea on basic assembly programming as well as the latest techniques in relevant area.

(iii) One short project purely on microcontroller programming will be done by the students as project competition which will increase their hands-on experience on assembly programming.

8. Tentative Date for hackathon/longathon.

Second Week of November

9. Tentative date/speaker for industry talk.

First Week of October

10. List tools (teaching and lab) that can be used in course.

Acadly

Mentimeter

11. Make a 2-5 min video to introduce your course (overall what you will teach, why this course is important, industrial application, how this course will be support students' future plans i.e. placement, business setup, others), make a YouTube playlist where first video will be your introductory video of the course. Share the playlist link. Record every lecture and upload in this playlist.

https://youtu.be/CriNRJp6fI4