Practice Set Pipeline 2

1. The time delay of a pipelined unit with four phases are as follows: t_1 = 50 ns, t_2 = 60 ns, t_3 = 90 ns, and t_4 = 80 ns. The interface register's delay time t_r = 10 ns. Calculate the following:

    a. Pipeline time for 1000 task completion

    b. Sequential time for 1000 task completion

    c. Throughput

2. A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to process 1000 data items on the pipeline will be (choose the correct alternate)-

    a. 120.4 microseconds

    b. 160.5 microseconds

    c. 165.5 microseconds

    d. 590.0 microseconds

3. The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. Calculate the throughput increase (in %).

4. You have been given 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?

5. Consider the following procedures. Assume that the pipeline registers have zero latency.

P1: 4-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns

P2: 4-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns

P3: 5-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns

P4: 5-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns

Which procedure has the highest peak clock frequency?