Control words for each stage

Opcode	Fetch	Decode	Execute	Mem Access	WB
Add SUB SLL SLTU XOR SRL SRA OR AND		Rs1 Rs2 Rd	Rd_rt = rd Alu_op = alu Alu_mux_sel1 = Rs1 Alu_mux_sel2 = Rs2		Data_or_alu = alu Load_reg_file = 1
ADDI SLTI SLTIU XORI ORI ANDI SLTI SLTIU XORI ORI ANDI SLLI SRLI SRAI		Rs1 Rd	Rd_rt = rd Alu_op = alu Alu_mux_sel1 = Rs1 Alu_mux_sel2 = i_imm		Data_or_alu = alu Load_reg_file = 1
SB SH SW		Rs1 Rs2	Rd_rt = rt Alu_op = add Alu_mux_sel1 = Rs1 Alu_mux_sel2 = s_imm	Mem_write = 1 Mem_address = alu_out Mem_wdata = rs2	
LB LH LW LBU LHU		Rs1 Rd	Rd_rt = rd Alu_op = add Alu_mux_sel1 = Rs1 Alu_mux_sel2 = s_imm	Mem_read = 1 Mem_address = alu_out	Data_or_alu = data Load_reg_file = 1
BEQ BNE BLT BGE		Pass Pc to adder Branch or			

BLTU BGEU		jal=branch Rs1 Rs2			
JALR		Rs1 Rd Jalr = 1	Rd_rt = rd		Data_or_alu = pcPlus4 Load_reg_file = 1
JAL		Rd Pass Pc to adder branch or jal = jal	Rd_rt = rd		Data_or_alu = pcPlus4 Load_reg_file = 1
AUIPC		Rd	Alu_op = add Alu_mux_sel1 = pc Alu_mux_sel2 = u_imm		Data_or_alu = alu Load_reg_file = 1
LUI		Rd			Data_or_alu = u_imm Load_reg_file = 1