11/30/22

Progress

Wrapped up debugging our CP3 and implemented three advanced design options—parameterized cache, branch prediction, and strided prefetching. Cache has a parameterized number of sets and is implemented as a 4 way cache. We implemented branch prediction as the tournament branch predictor, with accuracies of 90%, 97%, and 97.5% for the local, global, and tournament branch predictions. Strided prefetch implemented as d-cache data address prefetch. Prefetch stride calculated based on current data address minus previous data address, and prefetch is initiated whenever pmem_read and pmem_write in arbiter is free and when we perform a load instruction.

Distribution of Work

Jing: Parameterized cache, branch prediction
Albert: Strided prefetch
Justin: Branch prediction

Testing Strategy

Debugged CP3 by comparing to correct old register values in MP3, and continuously ensured that CP1 and CP2 were still working after each change. Also implemented RVFI monitor to help us keep track of shadow memory values and easier for future debugging.

After debugging CP3, designed and tested advanced features on individual branches to ensure modules functioning independently from each other.

Timing and Area

The timing report gives a slack (MET) of 4.02, indicating that the design is synthesizable. The area report gives a combinational area of 32852 and non-combinational area of 28593.

Roadmap

Continue to test and debug competition code, ensure all of our advanced designs work properly on competition code. Potentially continue improving our advanced features, such as parameterizing the RPT tag entries in the prefetch option.