80386 Microprocessor

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Lecture References:

Book:

- Microprocessors and Interfacing: Programming and Hardware, Chapter # 15, Author: Douglas V. Hall
- The Intel Microprocessor 8086...Arch. Prog, Interfacing.
 Author: Bary, Bray
- Microprocessor and Microcomputer Based System Design,
 Author: Mohamed Rafiquzzaman
- Lecture Materials:
 - M.A. Sattar, BUET, Dhaka, Bangladesh.

Limitations of 80286

- ▶ 16-bit ALU.
- ▶ 64K segment size for the programs and 16K descriptors for each of the programs
- ▶ Hence, 64KxI6K = I GB of virtual memory
- Cannot be easily switched back and forth between real and protected mode
 - To come back to the **real mode** from **protected mode**, it is needed to switched off the 80286.

80386 Overcomes 80286 Limitations

- It has 32 bit ALU.
- Segment size can be as large as 4GB
 - A program can have as many as 16K segments
 - So, a program has access to 4Gx16K=64TB of virtual memory
- ▶ 80386 has a **virtual 86 mode** which allows easy switching between **real** and **protected modes**.

80386: Salient Features

- ▶ Alternatively referred to as a 386 or the i386
- Intel introduced the first 32-bit chip, 80386, in October 1985 as an upgrade to the 80286 processor
- ▶ Intel stopped producing 386 since September 2007.
- ▶ 386 incorporates 275,000 transistor
- ▶ 386 was capable of performing more than five million instructions every second (MIPS)
- ▶ 386 was available in clock speeds between 12 and
- 5 **40MHZ.** CSE-4503: Microprocessors and Assembly Language Islamic University of Technology (IUT)

Versions of 80386

- ▶ Two versions were commonly available:
 - I) 80386 DX
 - 2) 80386 SX
- The original 80386 processor was renamed as 80386DX or 386DX after introducing 386SX.
- ▶ 80386SX was introduced in 1988 as a low cost solution alternative to the original 80386.
- ▶ 80386SX was developed after the DX, for the application that didn't require the full 32-bit capabilities.

Versions of 80386

- It is found in many PCs where it uses the same basic mother board design as the 80286.
- Most application need less than the 16MB of memory, so the SX is popular and less costly version of the 80386 microprocessor.
- ► The 80386SX lacked a math coprocessor but still featured the 32-bit architecture and built-in multitasking.
- The chip was available in clock speeds of 16MHz, 20MHz, 25MHz, and 33MHz.

80386DX Vs. 80386SX

80386DX	80386SX
32 bit address bus	24 bit address bus
32 bit data bus	16 bit data bus
Packaged in 132 pin	100 pin flat package
Address 4GB of memory	16 MB of memory

- Both have the same internal architecture.
- Lower cost package and the ease of interfacing to 8bit and 16-bit memory and peripherals make SX suitable for use in low cost systems.

80386 Data Bus

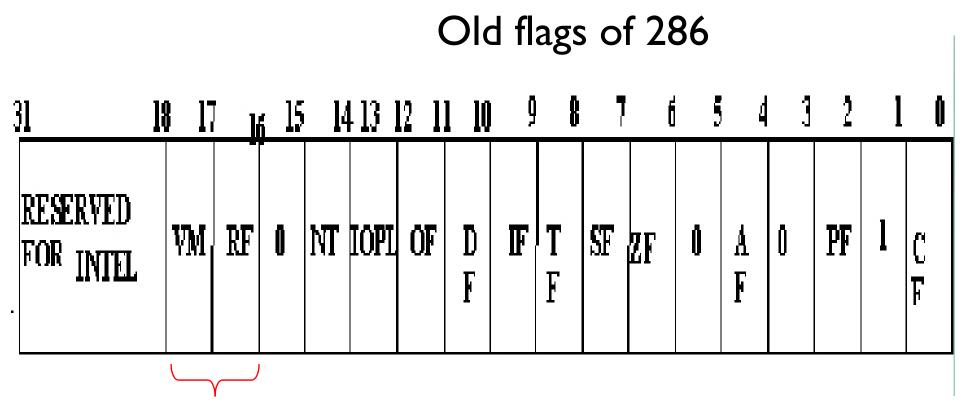
- ▶ 32-bit data bus
- ▶ D0 through D31 (Data Bus)
- ▶ Bi-Directional

80386 Address Bus

- Address bus consists of A2 to A31 address lines and BE0 to BE3 byte/bank enable lines
- No A0 & A1 address lines are available in 386
 - they are internally decoded to produce BE0 to BE3 signals
- ▶ BE0 through BE3
 - Byte (Bank???) Enable lines
 - Memory are arranged in 4 Banks
- BE0-BE3 also allow 386 to transfer byte, word and double word

Flag Register:

- ▶ The Flag register of 80386 is a 32 bit register.
- Out of the 32 bits, Intel has reserved bits D18 to D31, D5 and D3 and set to 0.
- While DI is always set at 1.
- Two extra new flags are added to the 80286 flag to derive the flag register of 80386.
- They are VM and RF flags.



New flags for 386

- > VM Virtual Mode Flag in Flag Register
- If this flag is set to 1, the 80386 enters the virtual 8086 mode within the protection mode.
- When VM bit is 0, 386 operates in protected mode
- This is to be set only when the 80386 is in protected mode.

- Resume Flag (RF) in Flag Register
- ▶ If RF=1, then 80386 ignores debug faults
 - Does not take another exception so that an instruction can be restarted after a normal debug exception.
- ▶ If RF=0, then 80386 takes another debug exception to service debug faults
- This flag is used with the debug register breakpoints.

Resume Flag (RF) in Flag Register

- It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle.
- The RF is automatically reset after successful execution of every instruction, except for IRET and POPF instructions.
- Also, it is not automatically cleared after the successful execution of JMP, CALL and INT instruction causing a task switch.
- These instruction are used to set the RF to the value specified by the memory data available at the stack.

Thank You!!

