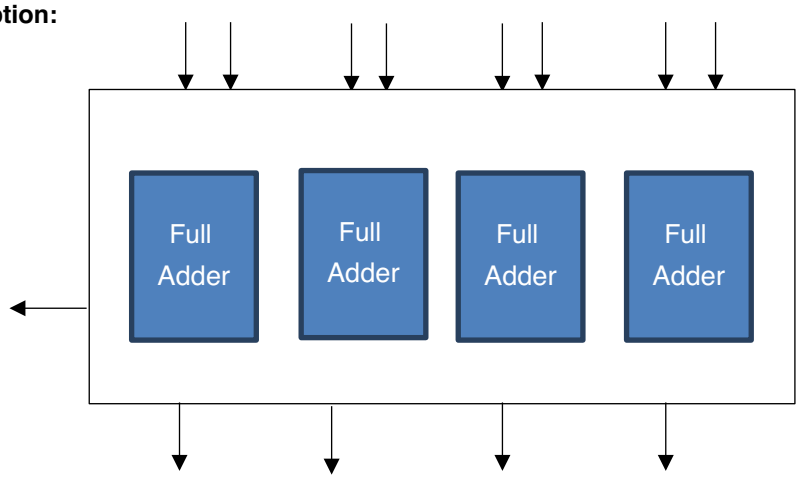
Adder

Purpose:

1. Learn to construct circuits hierarchically

2. Implement a 4-bit adder using Verilog and FPGA

System description:



Procedure:

1. Create a Full Adder module using structural modeling
2. Create a Full Adder module using behavioral modeling
3. Compare the resulting schematic of the two
4. Construct a 4-bit adder using the Full Adder module developed above (either structural or behavioral)
5. Conduct an **8-bit adder** using the same approach