

# Moiré Ferroelectrics and Neuromorphic Computing Applications

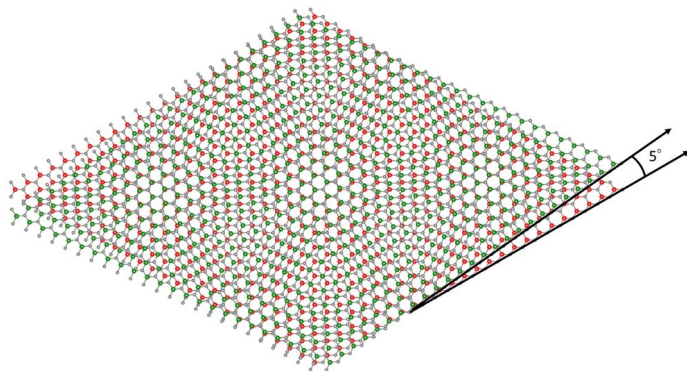
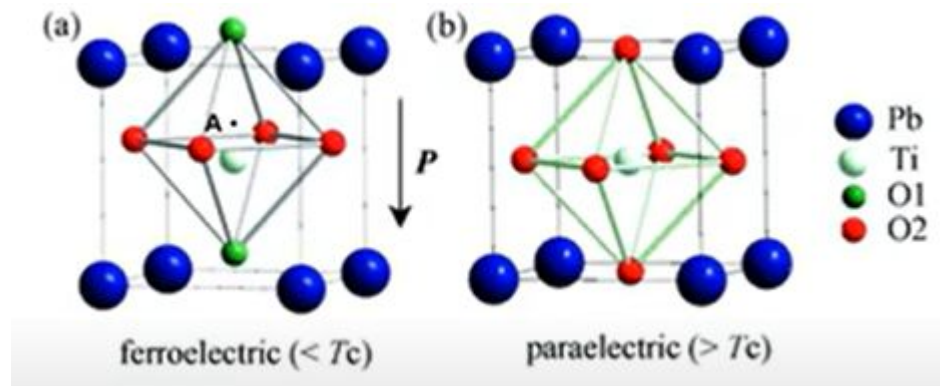
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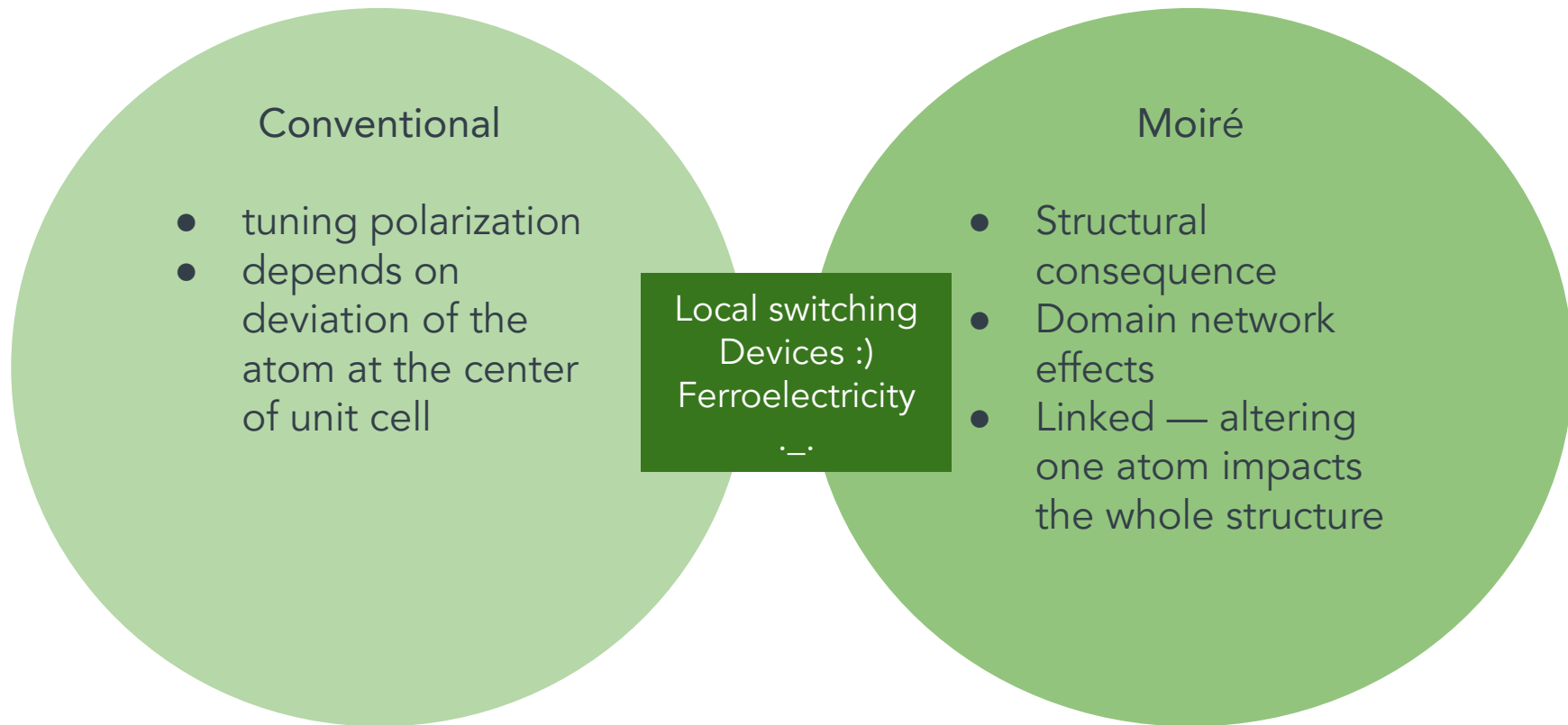
# Moiré vs. Conventional Ferroelectrics

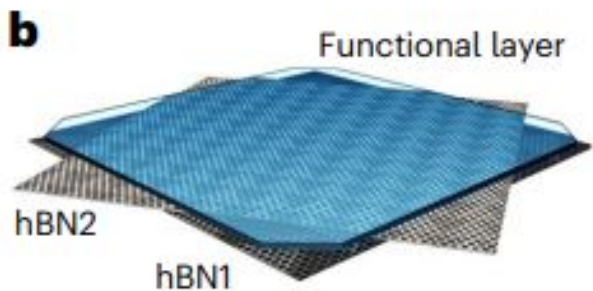
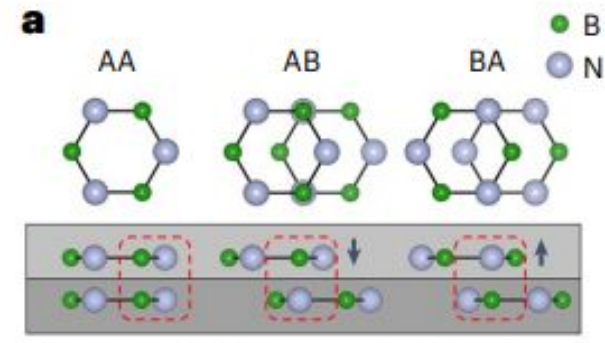
Ferroelectrics: Materials with spontaneous polarization; can be manipulated via external electric field

Moiré Materials: Stacked 2D materials with twist angle; generates new properties

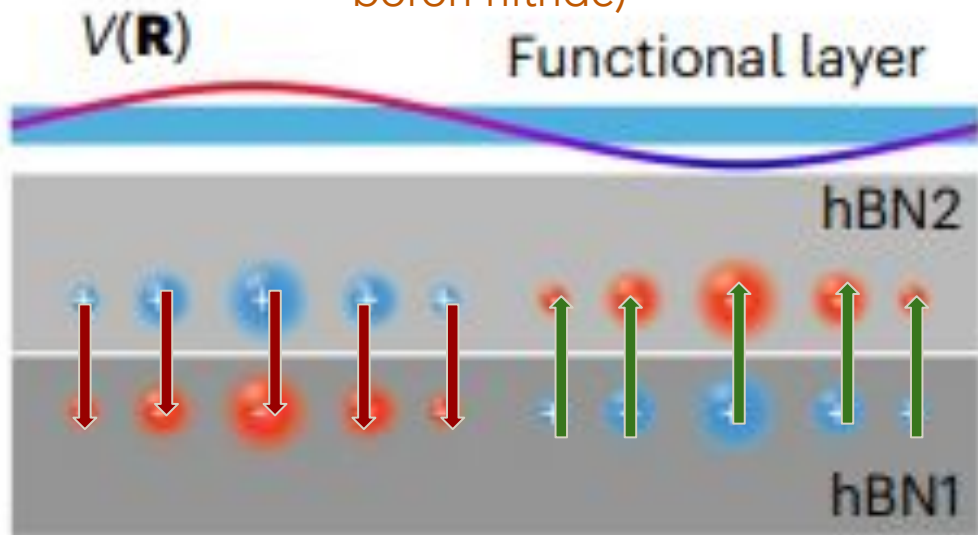


# Moiré vs. Conventional Ferroelectrics





t-hBN  
(twisted hexagonal  
boron nitride)

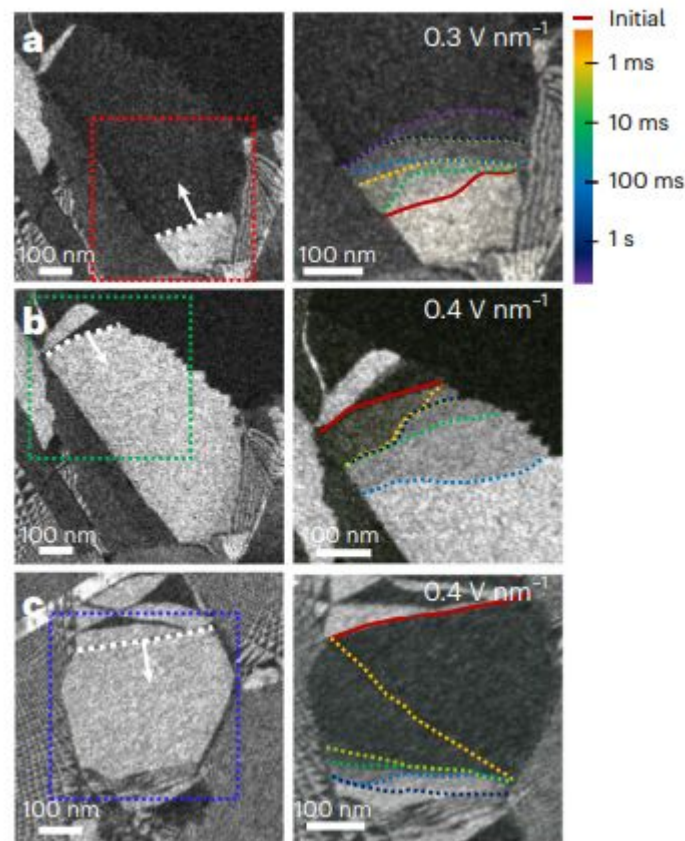
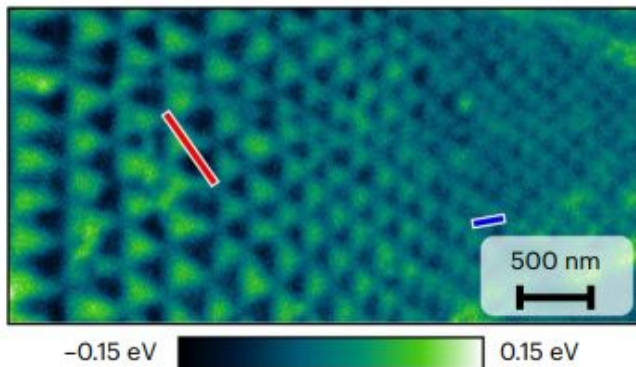


Net dipole  
moment for  
regions!



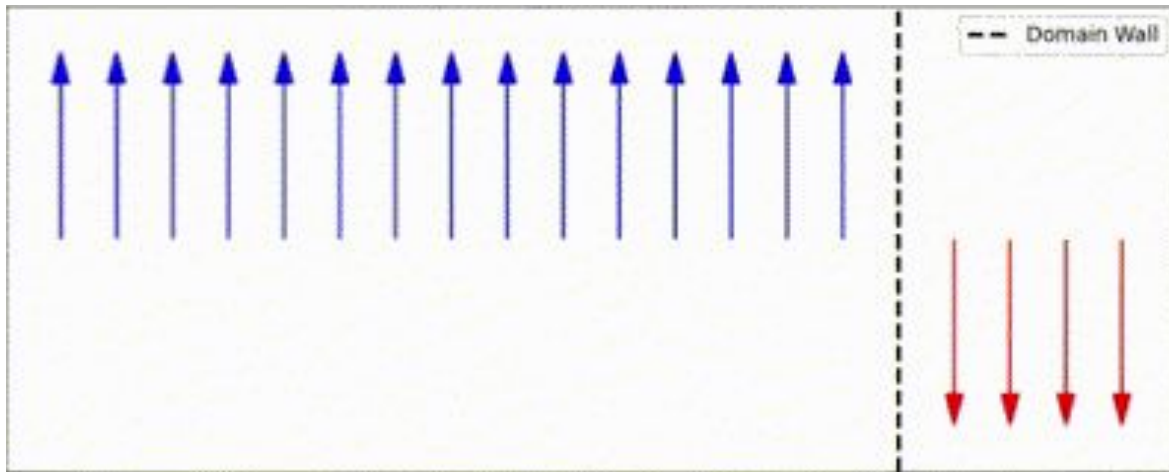
# Ferroelectric Domains

- Different regions of a material with different polarizations
- Separated by domain walls — boundaries of enhanced electrical conductance
- Twist angle determines size of domains in general (inversely related)\* - stress and strain cause deformations

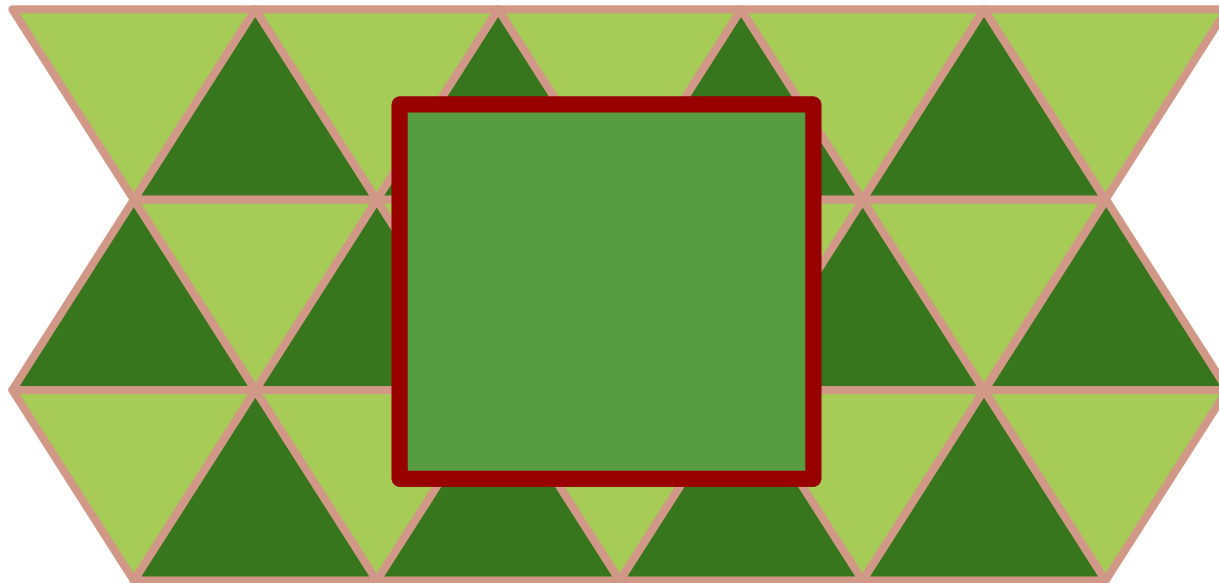


# Local vs. Nonlocal Switching

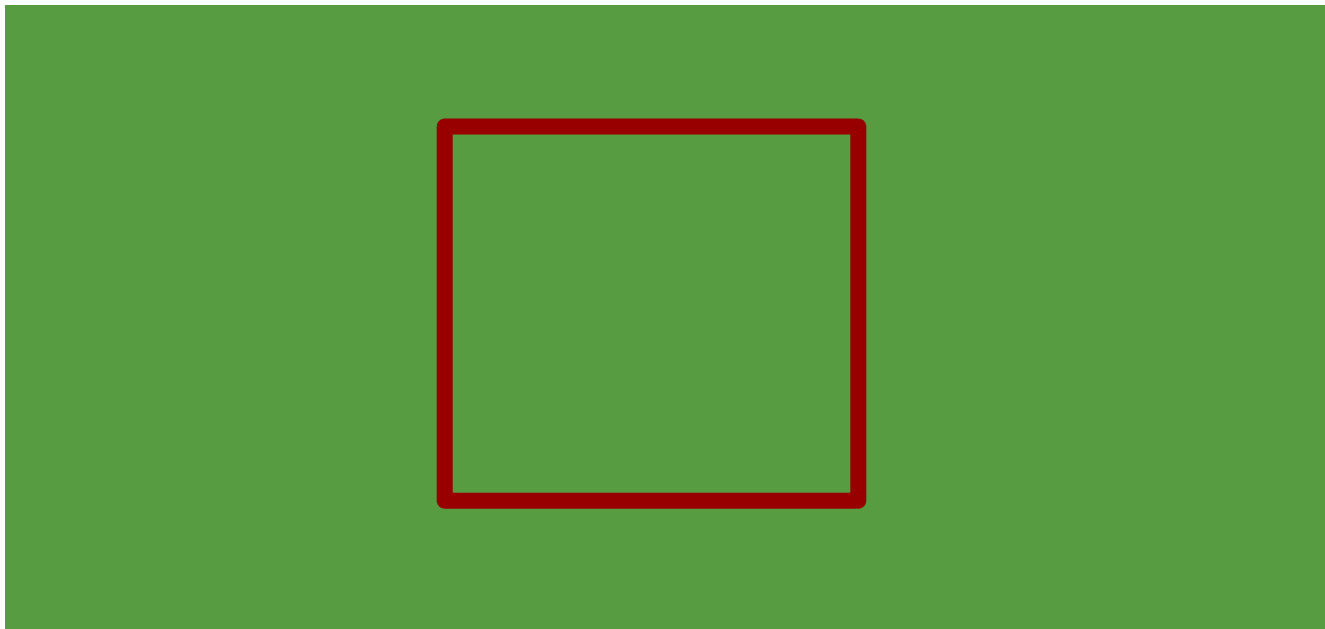
- local domain switching with voltage application —
- domain walls are shifting, and the new region they annex is ascribed the polarization (domain wall gerrymandering)



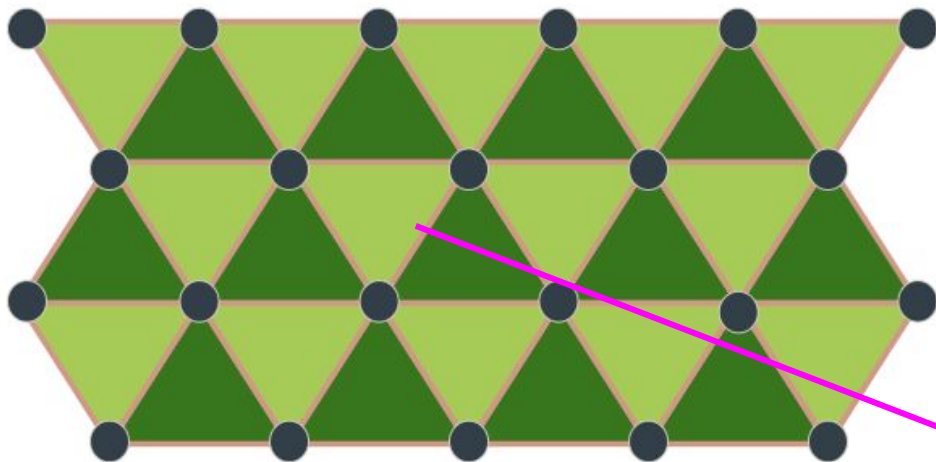
Expected switching behavior:



But in t-hBN, applying voltage to a single region causes switching over the entire sample! Why...?



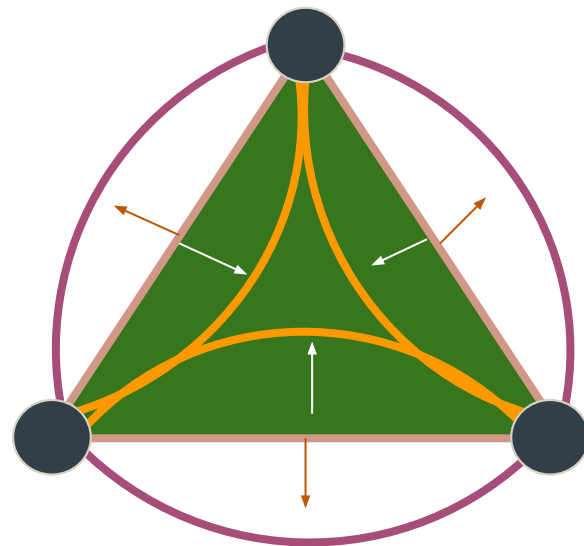




## The answer: Domain wall dynamics

- Domain walls no longer “translate” — they expand/contract about fixed points
- Change size

- Domain wall interconnectivity influences global behavior
- Periodicity is erased — restores back to original state like a rubber band
- Memory is temporarily lost



What can we do with this material?



Make devices.



For what?



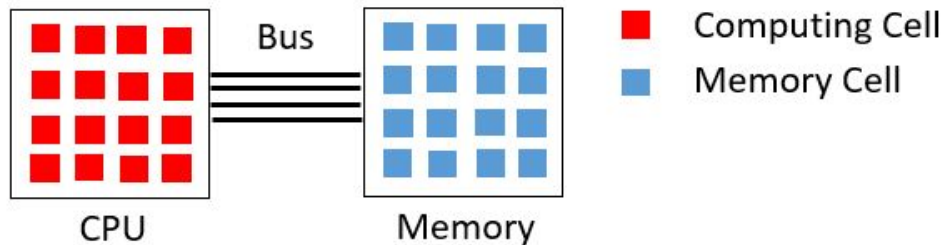
Neuromorphic computing!



What is that?

# What is neuromorphic computing?

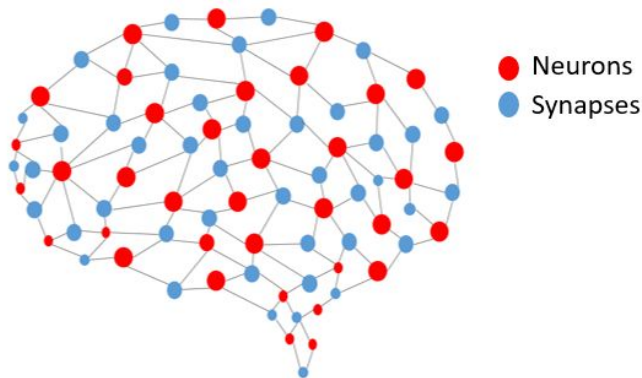
Von Neumann bottleneck -  
memory and processing are  
separate units so data needs to be  
carried back and forth between  
them



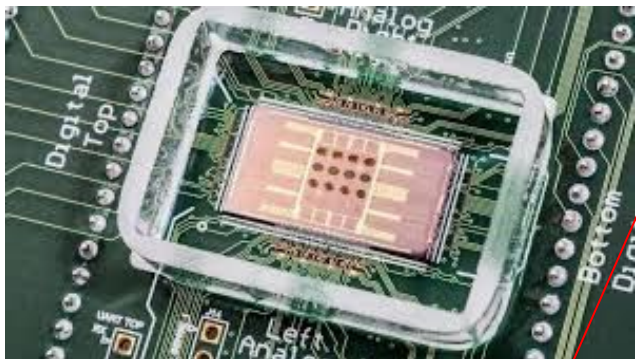
There is transfer latency between  
memory and central processor —  
“memory wall”

# What is neuromorphic computing?

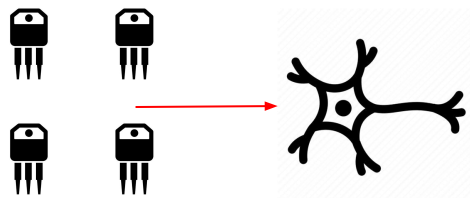
- hardware and algorithms that efficiently process information by mimicking the functionality of the human brain — create artificial neurons and synapses
- computations processed where the data is located — improved processing speed



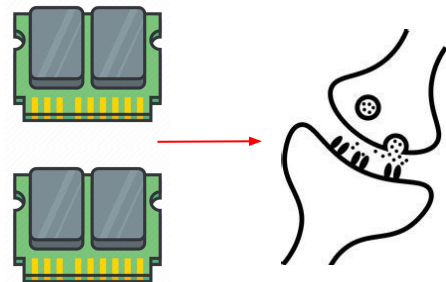
# But there's a problem...



complementary metal-oxide-semiconductor (CMOS) chip



transistors —> neuron



memories —> synapse

brain has ~ 10000 synapses  
per neuron — cannot  
replicate on CMOS

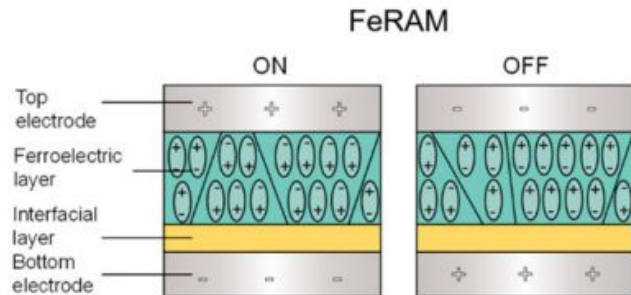
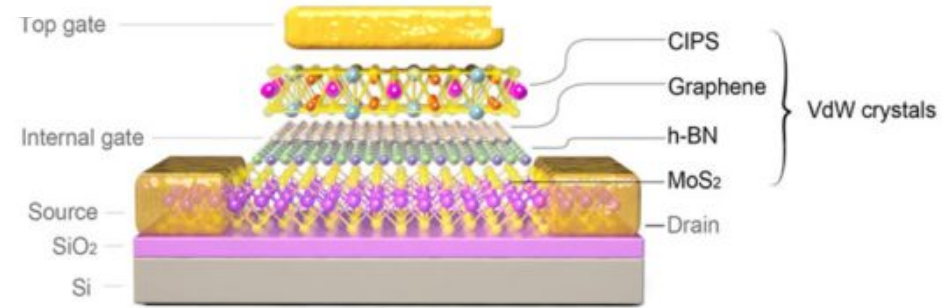
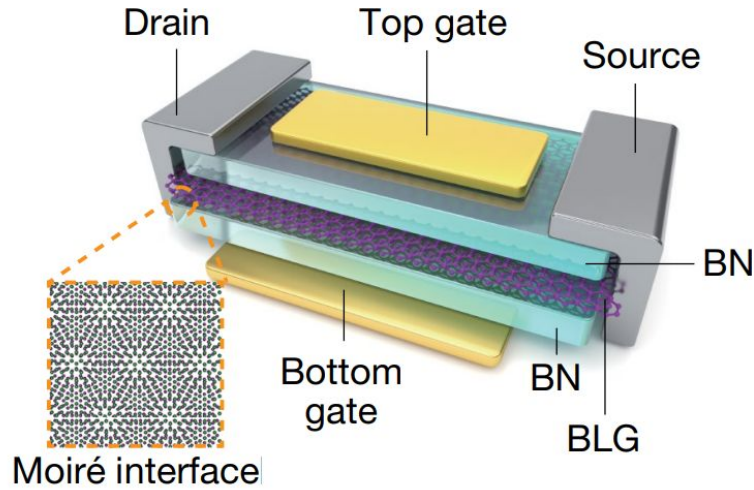
need chips with MILLIONS  
of artificial neurons and  
synapses

How??

# Ferroelectrics in Neuromorphic Computing

## Advantages

- ultra-fast write/read speed
- ultra-low power consumption
  - long retention
  - high endurance
- practical implementation of high-performance synaptic devices
  - non-volatile memory



- FeRAM : ferroelectric memristor with MFM sandwich; two-terminal
- FeFET : ferroelectric field effect transistor; ferroelectrics serve as the gate dielectric in a three-terminal transistor structure
- FTJ : two-terminal device with a ferroelectric material sandwiched between two electrodes

But ferroelectric devices already exist!  
What's special about the t-hBN?

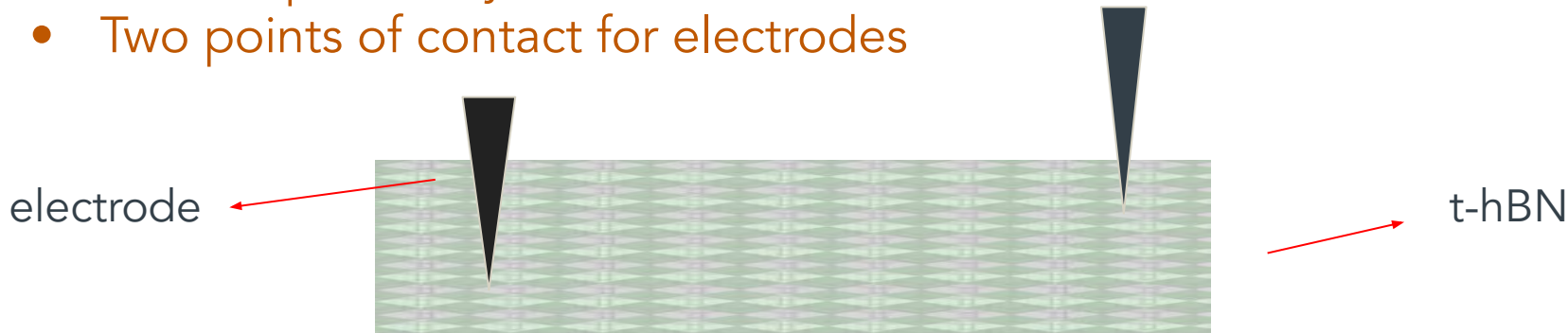


Global switching behavior!



# Applications of Nonlocal Switching To Neuromorphic Computing

- use t-hBN as ferroelectric layer in FeRAM, FTJ, or FeFET - like device
- device with one point of contact to an external electric field; plating is not necessary
- temporary store for memory due to recoverable erasure in moiré periodicity
- Lower energy consumption
- Time dependency
- Two points of contact for electrodes



# Future Efforts

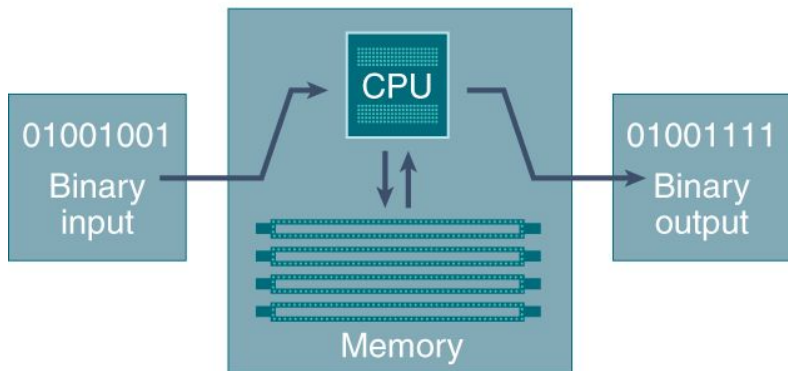
- What causes the “forgetting” and “recovering” of periodicity? Is it a consequence of the moiré structure? Does the capacity for domain walls to store information play a role?
- Why is non-local switching happening? How do domain network dynamics contribute to this? Is synaptic behavior a sufficient explanation?
- What other ferroelectrics can exhibit non-local switching?

# Acknowledgements

I would like to thank Kyoung Pyo Lee and Dr. Xiaoqin Li for giving me the opportunity to work on this project.

# Extra Slides

## Von Neumann architecture



Sequential processing

Separated computation and memory

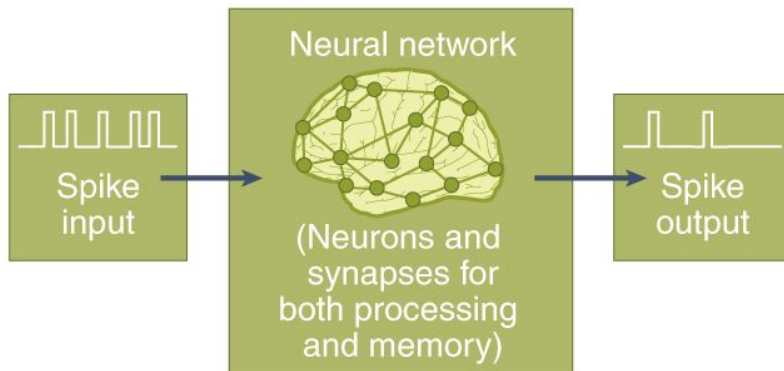
Code as binary instructions

Binary data

Synchronous (clock-driven)

versus

## Neuromorphic architecture



Massively parallel processing

Collocated processing and memory

Spiking neural network

Spikes

Asynchronous (event-driven)

Operation

Organization

Programming

Communication

Timing

## Brains...

- have ultra low power consumption (on the order of 20 W) compared to supercomputers (consumes on the order of 1000 kWh - this is a 6 YEAR energy budget for a brain)
- store memory, learn with few examples and from experience
- have direct access to memory via synapses
- have high plasticity due to many adaptive synapses

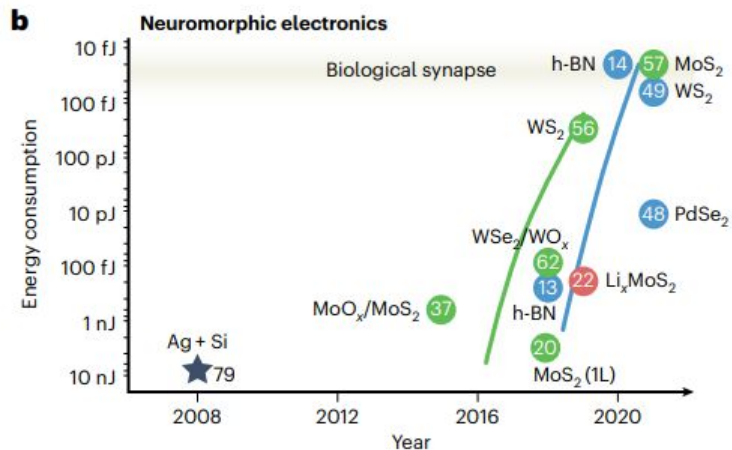
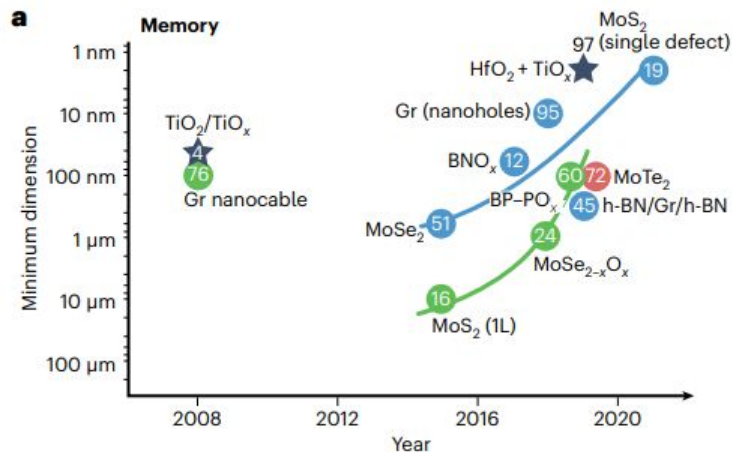
**Table 1.** Benchmark of the memory technologies.

Technology	SRAM	DRAM	NAND	RRAM	PCM	MTJ	FeRAM	FeFET	FTJ
Cell elements	6T	1T1C	1T	1T1R	1T1R	1T1C	1T1C	1T	1R
Cell area	$>100 \text{ F}^2$	$6 \text{ F}^2$	$<4 \text{ F}^2$	$4\text{--}12 \text{ F}^2$	$4\text{--}30 \text{ F}^2$	$6\text{--}50 \text{ F}^2$	$22 \text{ F}^2$	$6 \text{ F}^2$	$4 \text{ F}^2$
Write voltage	$<1 \text{ V}$	$<1 \text{ V}$	$>10 \text{ V}$	$<3 \text{ V}$	$<3 \text{ V}$	$<1.5 \text{ V}$	$<3 \text{ V}$	$<5 \text{ V}$	$<4 \text{ V}$
W/R time	0.3 ns	$<10 \text{ ns}$	0.1 ms	10 ns	50 ns	20 ns	$<5 \text{ ns}$	$<4 \text{ ns}$	$<1 \text{ ns}$
Retention	0	64 ms	$>10 \text{ years}$	$>10 \text{ years}$	$>10 \text{ years}$	$>10 \text{ years}$	$>10 \text{ years}$	$>10 \text{ years}$	$>10 \text{ years}$
Endurance	$>10^{16}$	$>10^{16}$	$>10^5$	$10^6\text{--}10^{12}$	$10^6\text{--}10^9$	$>10^{15}$	$>10^{14}$	$>10^{10}$	$>10^7$
Write energy	$\sim 0.7 \text{ fJ}$	$\sim 5 \text{ fJ}$	$\sim 10 \text{ fJ}$	$\sim 0.1 \text{ pJ}$	$\sim 10 \text{ pJ}$	$\sim 0.1 \text{ pJ}$	$\sim 30 \text{ fJ}$	$<10 \text{ fJ}$	$<5 \text{ fJ}$
Suitability for DNN training	No	No	No	No	No	No	No	Moderate	Moderate
Suitability for SNN applications	Yes	Yes	No	Yes	Yes	Moderate	Yes	Yes	Yes

**Table 2.** Summary of the experimentally examined ferroelectric 2D materials.

Material	Polarization	Thickness obtaining ferroelectricity	Characterization method	$P_r$	$E_c$	$T_c$ (K)	Reference
SnS	In-plane	3.7–8.1 nm	$P$ – $E$ measurement	$\sim 17.5 \mu\text{C cm}^{-2}$	$\sim 20 \text{ kV cm}^{-1}$	873	41
WTe <sub>2</sub>	Out-of-plane	1.4 nm	$I$ – $V$ measurement	—	—	350	32
d1T-MoTe <sub>2</sub>	Out-of-plane	0.8 nm	PFM	—	—	RT	33
SnTe	In-plane	0.63 nm	STM	—	—	270	34
CuInP <sub>2</sub> S <sub>6</sub>	Out-of-plane	4 nm	PFM	—	—	315	35
BA <sub>2</sub> PbCl <sub>4</sub>	In-plane	4 nm	PFM	—	—	453	36
$\alpha$ -In <sub>2</sub> Se <sub>3</sub>	In-plane/Out-of-plane	10 nm	PFM	—	—	RT	37
$\beta'$ -In <sub>2</sub> Se <sub>3</sub>	In-plane	100 nm	PFM	—	—	473	38
2H $\alpha$ -In <sub>2</sub> Se <sub>3</sub>	In-plane/Out-of-plane	1.2 nm	PFM	—	—	RT	39
SnSe	Out-of-plane	28 nm	PFM	—	—	—	40

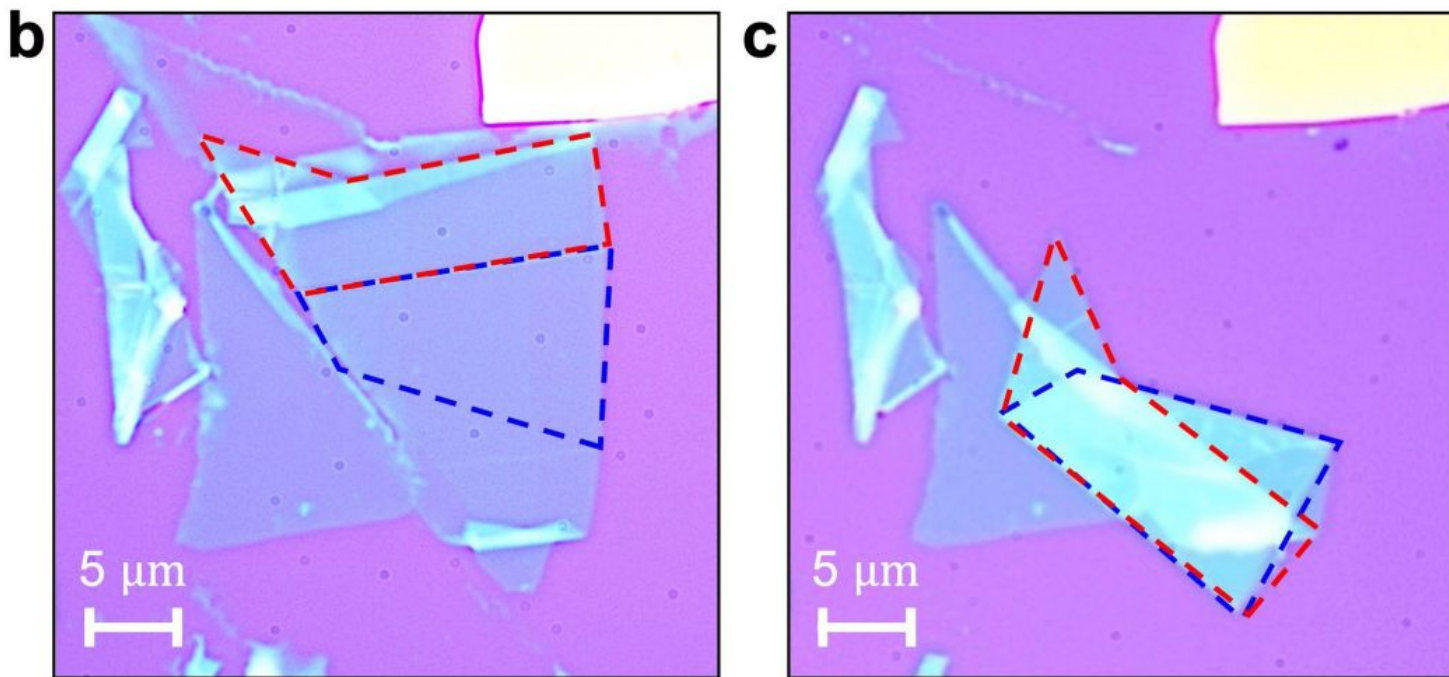




Part of emulating a synapse means to ensure that your device is capable of short and long term plasticity, spike-timing dependent plasticity, and heterosynaptic plasticity.

Artificial synapses can update and memorize internal conductivity known as synaptic weight in response to external stimuli.

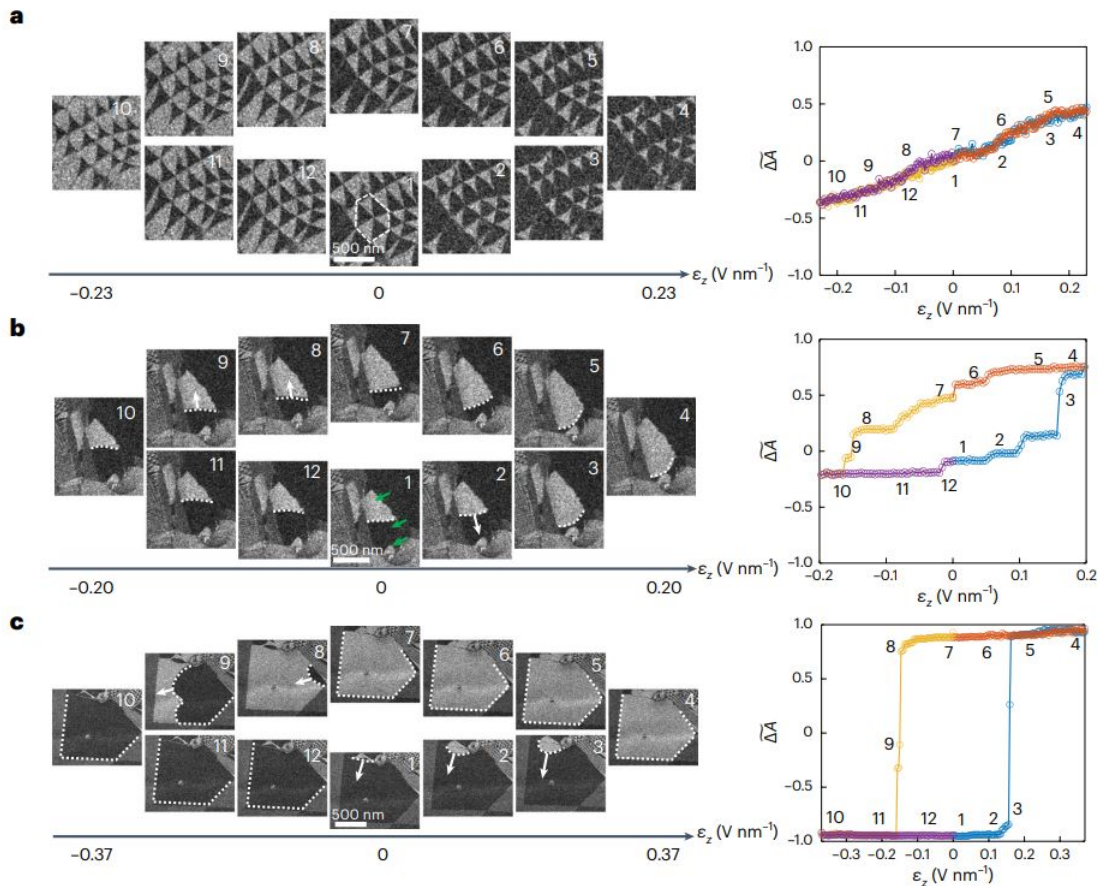
Li, M., Liu, H., Zhao, R. et al. Imperfection-enabled memristive switching in van der Waals materials. *Nat Electron* 6, 491–505 (2023). <https://doi.org/10.1038/s41928-023-00984-2>



**Extended Data Fig. 1 | Introduction of folding and folded hBN flakes.**  
**a**, Illustration of folding along the zigzag (armchair) direction leading to the parallel (anti-parallel) orientation at the interface. Optical image of one - 4 nm

thick hBN flake **(b)** before and **(c)** after folding. Scale bars represent 5 μm. The folded regions are marked by dashed lines with different colour contrasts. The blue and red dashed lines encircle the bilayer and trilayer regions in **(c)**, respectively.

Kim, D.S., Dominguez, R.C., Mayorga-Luna, R. *et al.* Electrostatic moiré potential from twisted hexagonal boron nitride layers. *Nat. Mater.* 23, 65–70 (2024).  
<https://doi.org/10.1038/s41563-023-01637-7>



- White lines show domain wall + direction of motion
- Plots of normalized polarization vs. voltage during sweep

Ko, K., Yuk, A., Engelke, R. *et al.* Operando electron microscopy investigation of polar domain dynamics in twisted van der Waals homobilayers. *Nat. Mater.* 22, 992–998 (2023).  
<https://doi.org/10.1038/s41563-023-01595-0>