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11/29/22

ECE-310

Lab4

Model #1: 4-bit register with synchronous reset and load

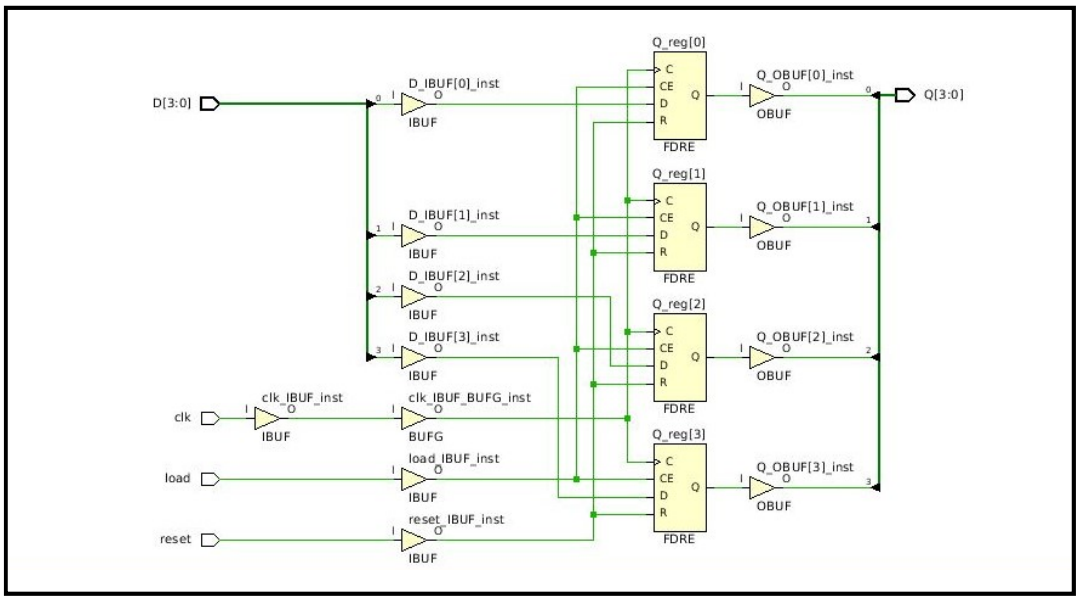


Figure 1: RTL Schematic of 4-bit register

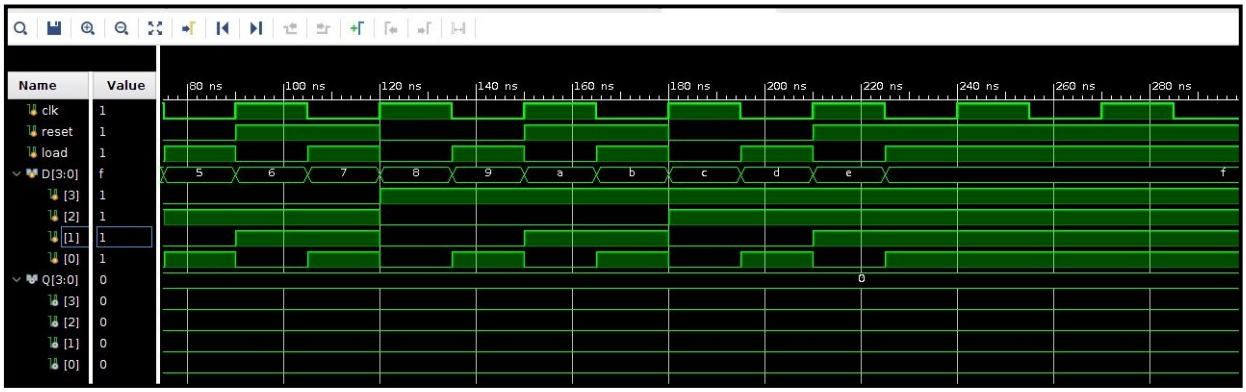
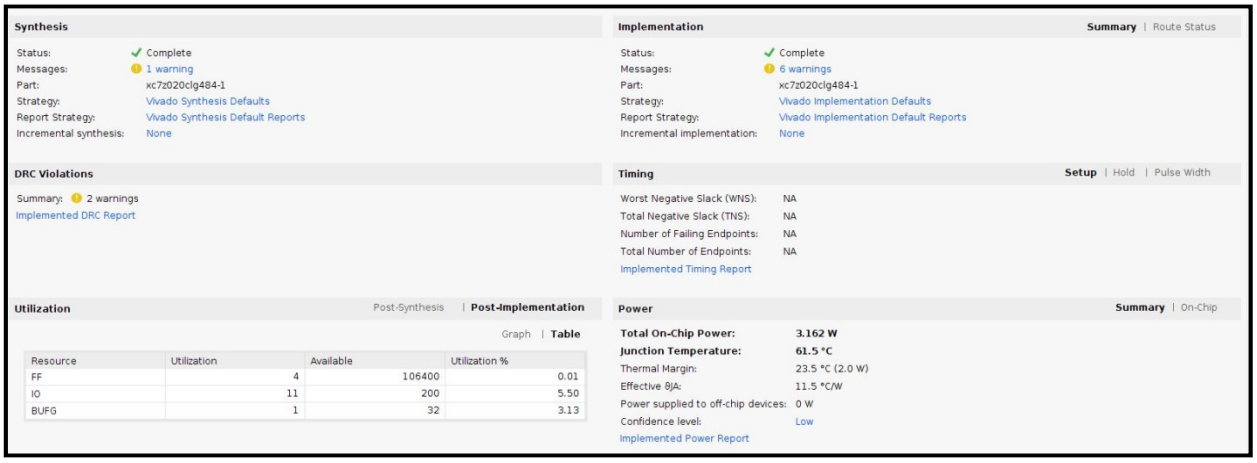


Figure 2: Post-Implementation Timing simulation waveform. It is very similar to the behavioral Simulation waveform.



Synthesis

Status:	Complete
Messages:	1 warning
Part:	xc7z020clg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	None

Implementation — Summary | Route Status

Status:	Complete
Messages:	6 warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 2 warnings

Implemented DRC Report

Timing — Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	NA
Total Negative Slack (TNS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

Implemented Timing Report

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization %
FF	4	106400	0.01
IO	11	200	5.50
BUFG	1	32	3.13

Power — Summary | On-Chip

Total On-Chip Power:	**3.162 W**
Junction Temperature:	**61.5 °C**
Thermal Margin:	23.5 °C (2.0 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Figure 3: Project Summary and Utilization. Highest is IO.

Model #2: 4-bit parallel in left shift register

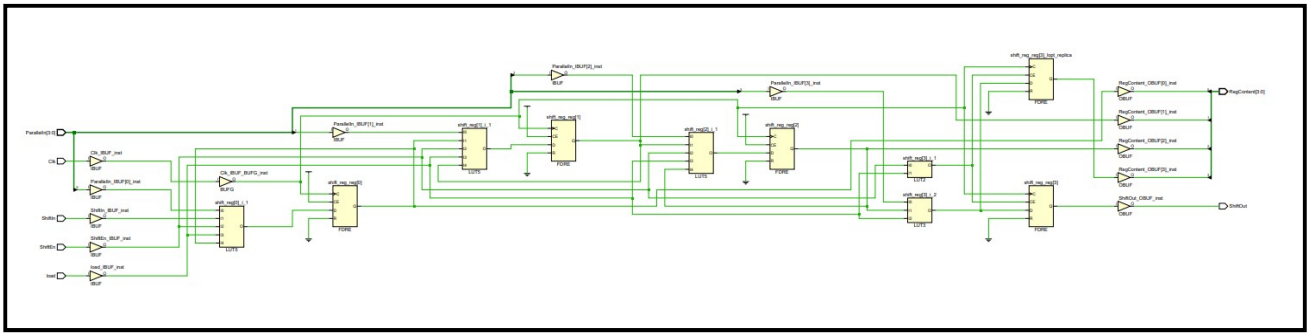


Figure 4: RTL Schematic of 4-bit parallel in left shift register

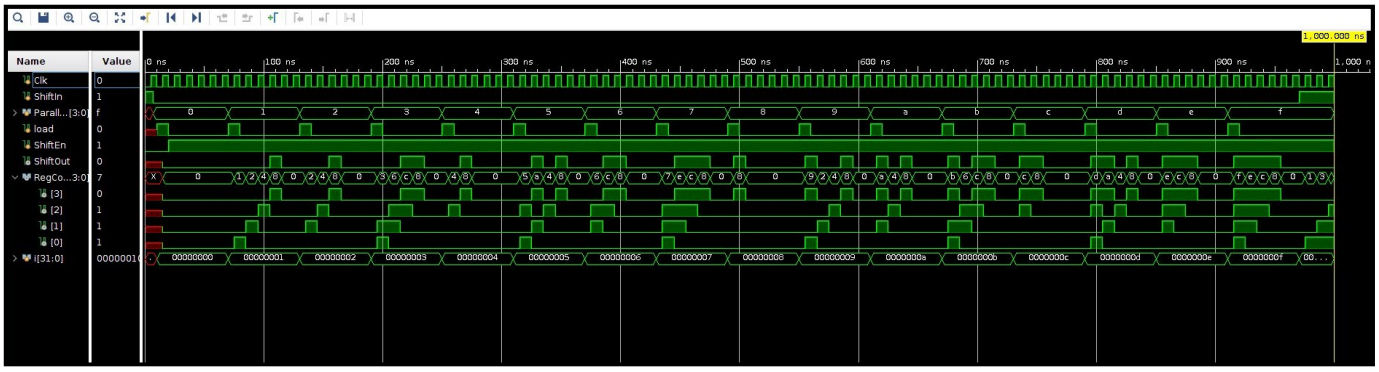


Figure 5: Post-Implementation Timing simulation waveform. Notice RegContent shifts the data as the clocks pulses

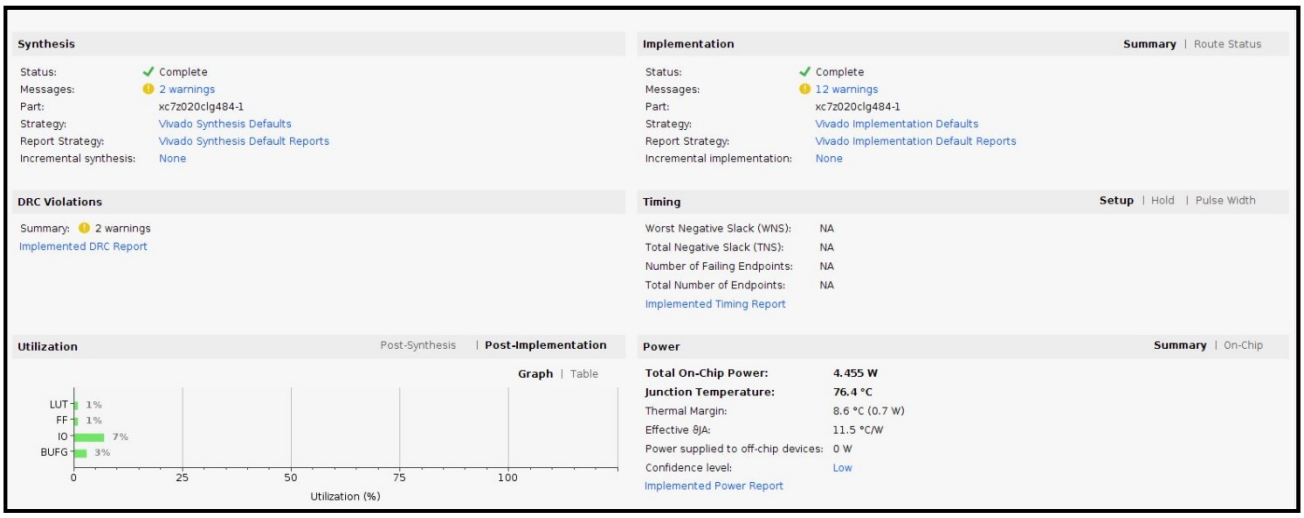


Figure 6: Project Summary and Utilization. Highest is IO with new utilization of LUT.

Model #3: 8-bit counter using T flip-flops

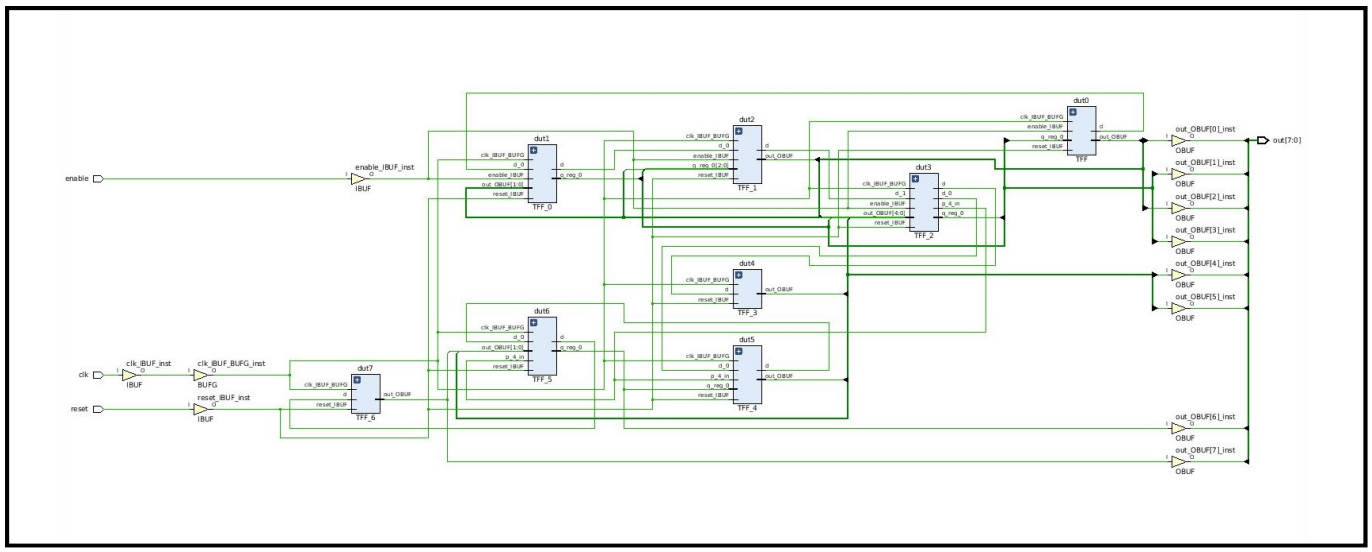


Figure 7: RTL Schematic of 8-bit counter using T flip-flops

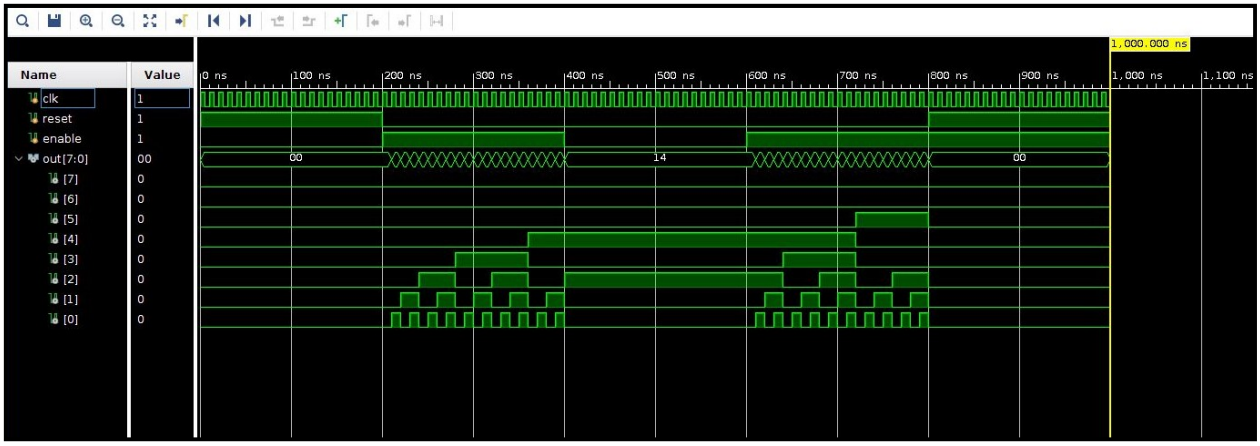


Figure 8: Post-Implementation Timing simulation waveform. Notice Counter value increases from 0 to 14 on positive edge of clock along with the enable and reset mode changes the output correspondingly

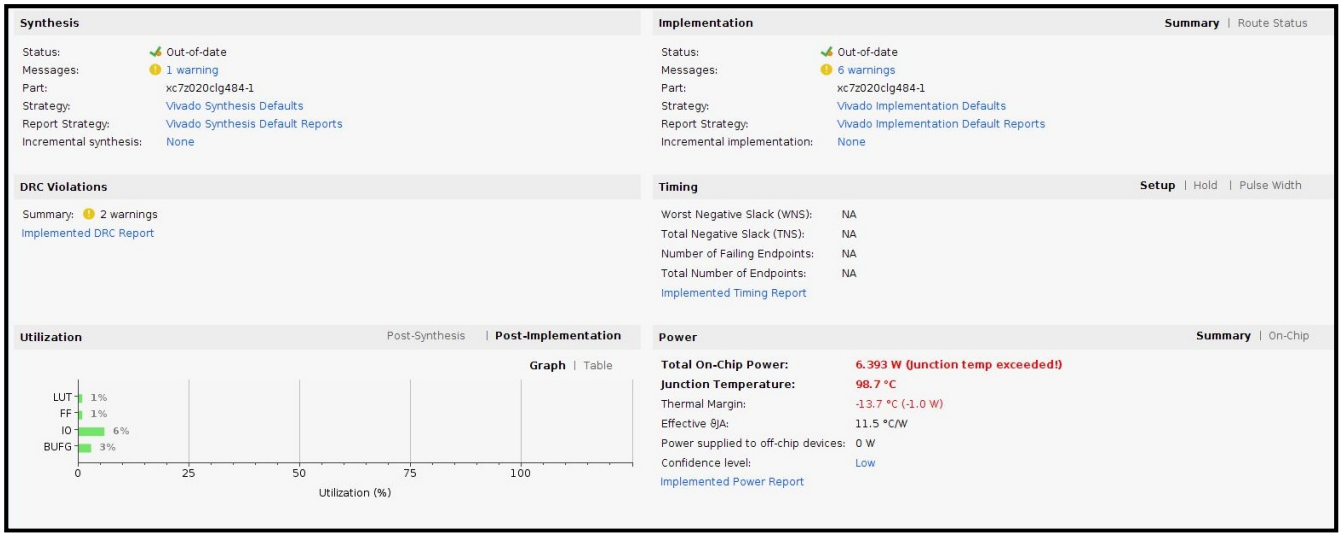


Figure 9: Project Summary and Utilization. Highest is IO and considerable power usage.

Model #4: 8-bit counter using D flip-flops

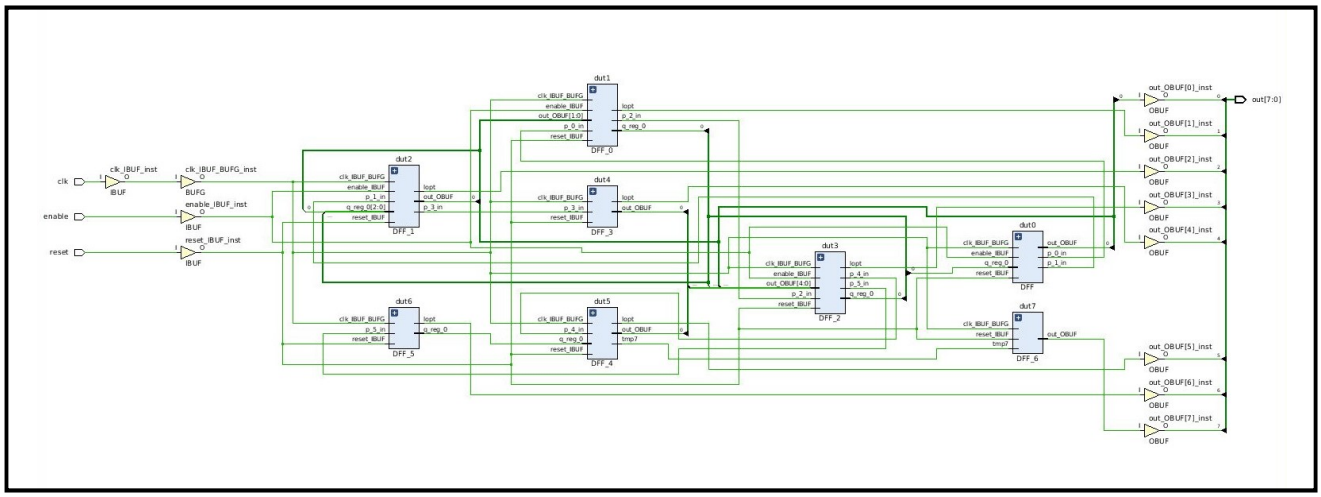


Figure 10: RTL Schematic of 8-bit counter using D flip-flops

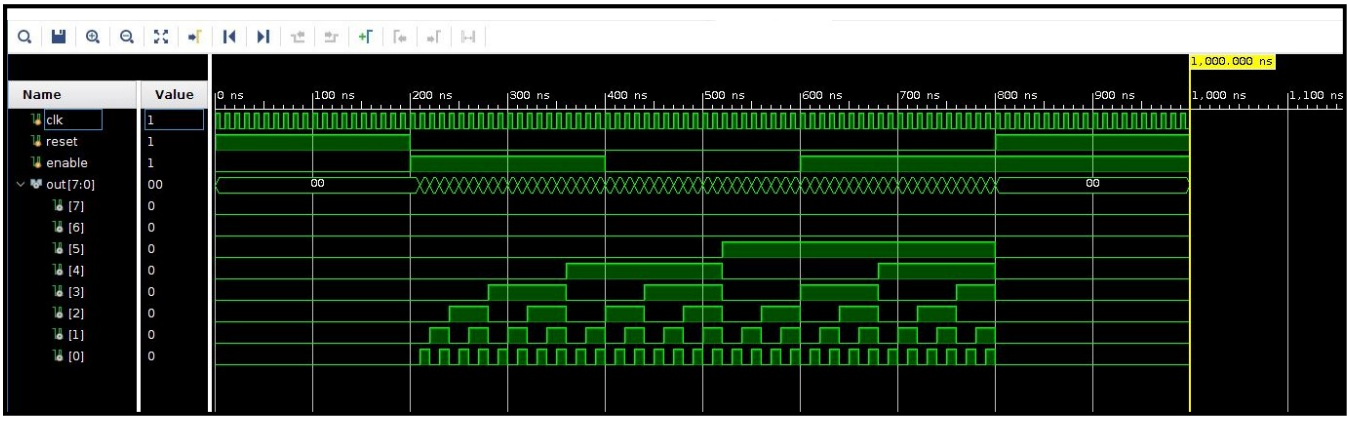


Figure 11: Post-Implementation Timing simulation waveform.

Figure 12: Project Summary and Utilization. Highest is IO and considerable power usage.

Model #5: Counter with sequence: 000, 001, 011, 101, 111, 010

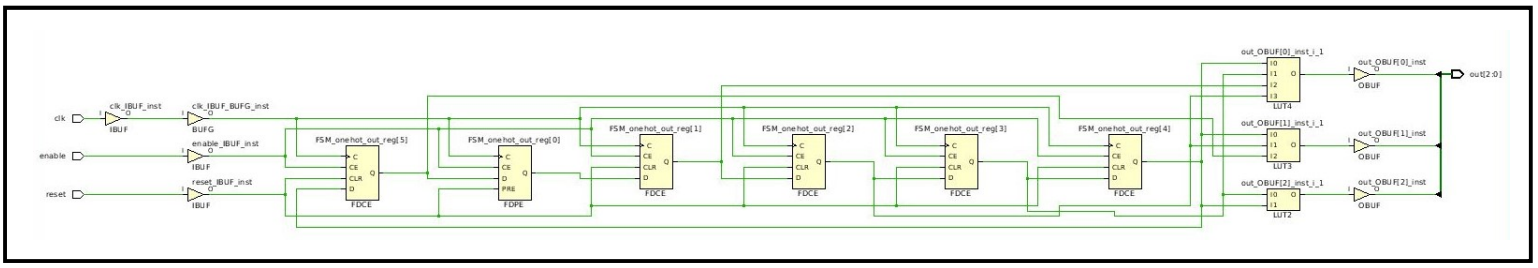


Figure 13: RTL Schematic of Counter

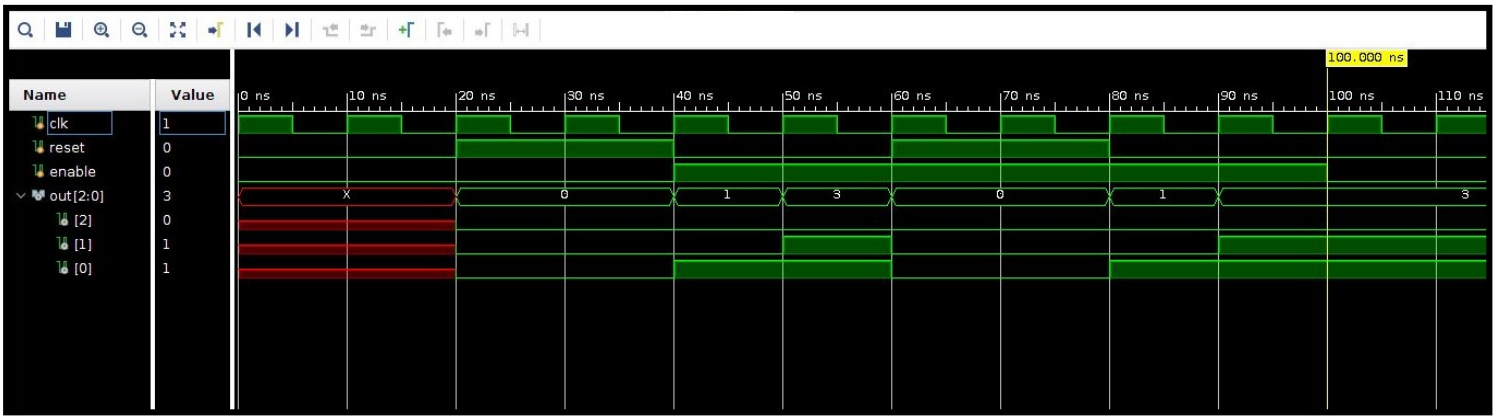


Figure 14: Post-Implementation Timing simulation waveform.

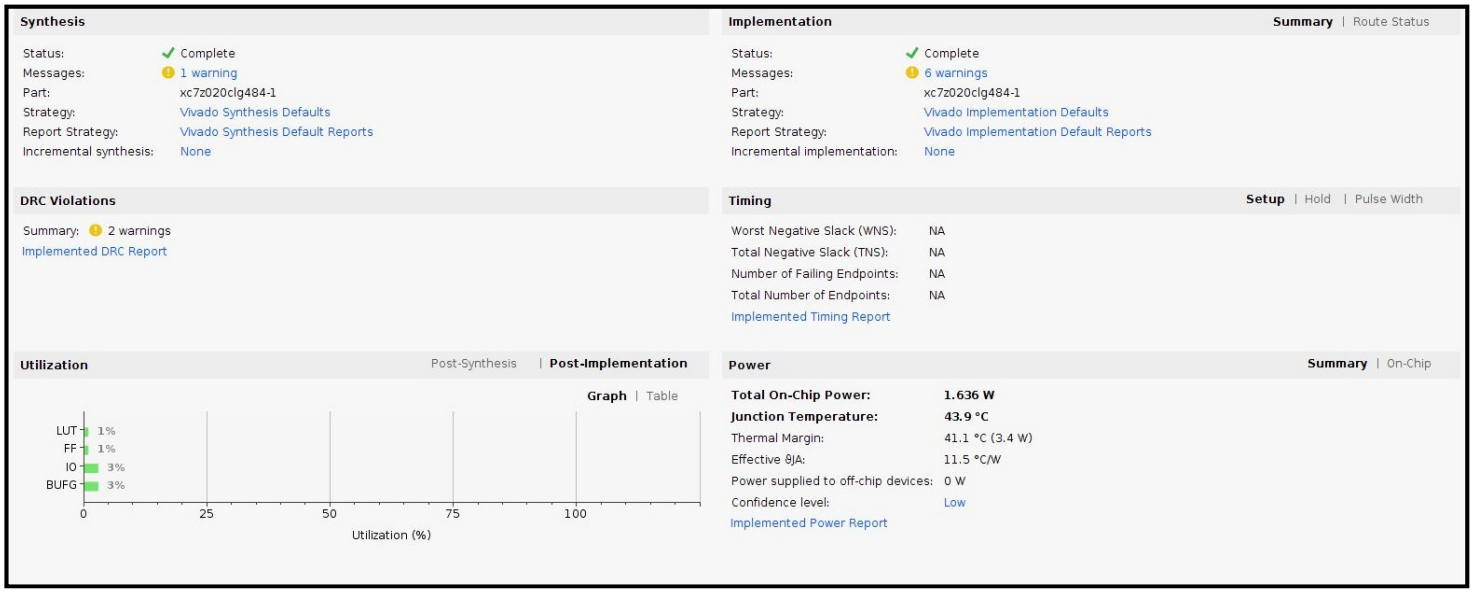


Figure 15: Project Summary and Utilization. Highest is IO and okay power usage.

Model #6: 3bit Multiplier