Project 1: 2.4GHz Two-Stage Operational Amplifier for WiFi/Bluetooth Application

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ECE 345

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Design Requirements

We require an Op-amp with a differential peak-to-peak output swing of over 0.8V (with a single-ended peak-to-peak swing of 0.4V), and there are six key factors we need to consider:

- Unity gain frequency (fu): Given our oscillator operating frequency of 2.4GHz, we need to ensure that the Op-amp's unity gain frequency is at least 5GHz.
- Phase margin: It is important to have a phase margin of at least 60 degrees for the Op-amp.
- Power consumption: We have a target power consumption of 5mW for the Op-amp.
- Gain: A large gain is essential for the Op-amp, with a target of 35dB at low frequencies (< 3dB frequency).
- Peak-to-peak output amplitude: Each output should have a minimum peak-to-peak amplitude of 0.4V, with a differential peak-to-peak amplitude of 0.8V at maximum.
- Common-mode feedback techniques.

General Design

The general structure of the Amplifier is modeled after a Two-Stage OPAMP circuit mentioned in chapter 9 of Behzad Razavi's *Design of Analog CMOS Integrated Circuits*. It features Common Mode Feedback in the inner and outer stages using the bias resistors R1/R2 and R3/R4 respectively.

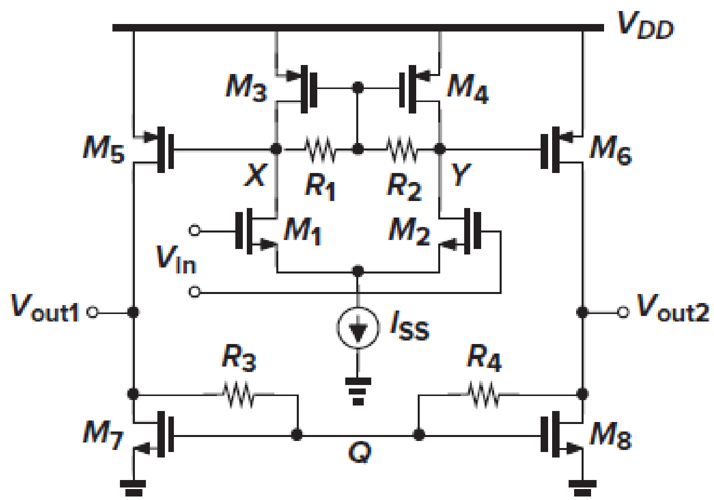
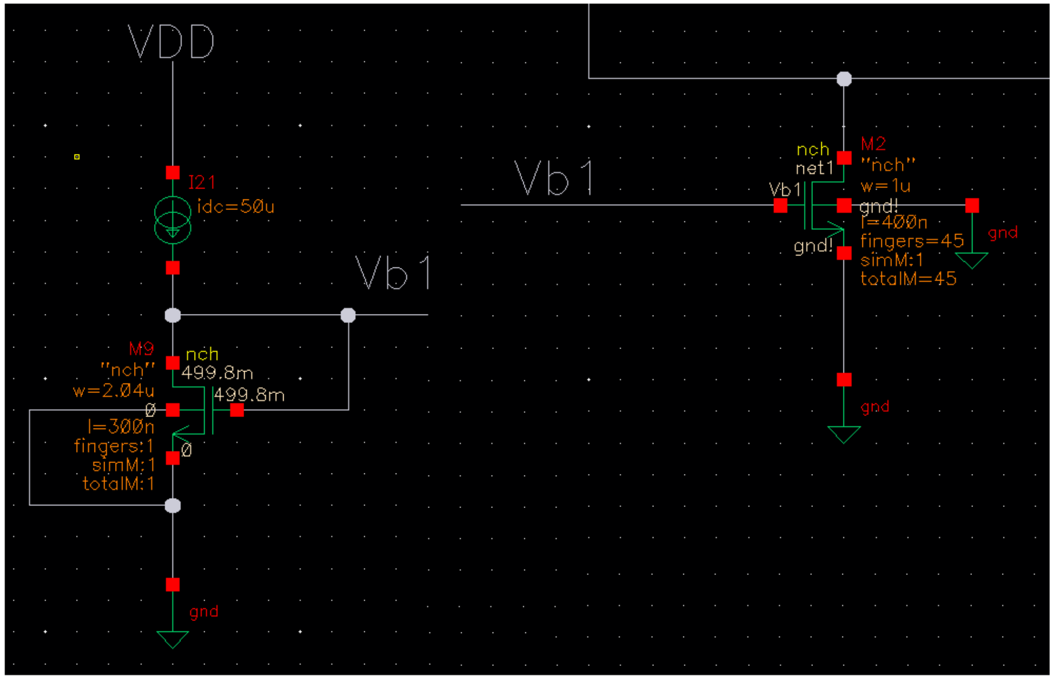


Figure 9.62 Simple CMFB loops around each stage.

Design Strategies

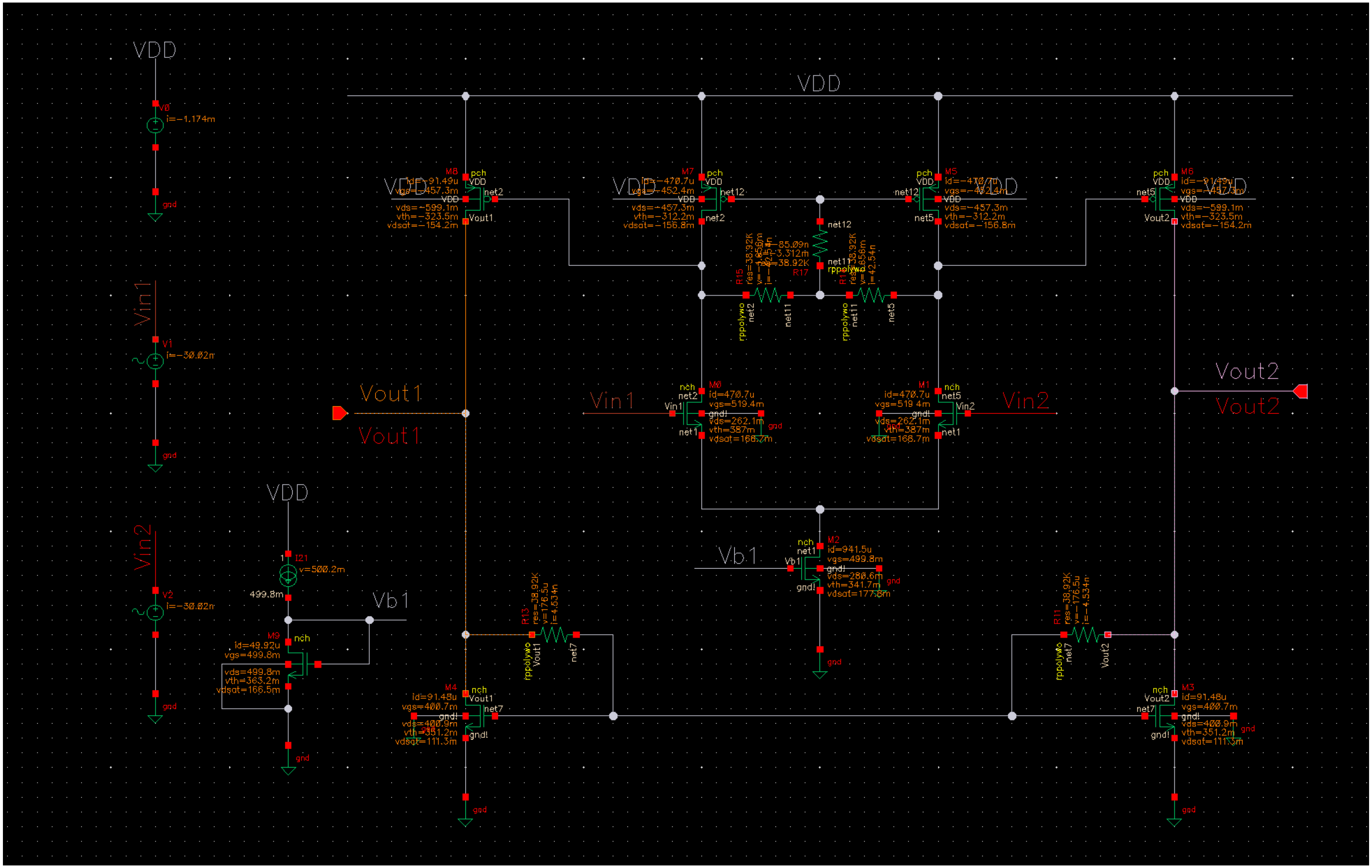
The I_{SS} current was prepared using a current mirror comprising of two N-Type Mosfets and an ideal current source (ideal voltage sources weren't permitted). The gate voltage was set to around 500mv by inclemently increasing the width of the Mosfet. This allows the Mosfet to be biased correctly and always in saturation.



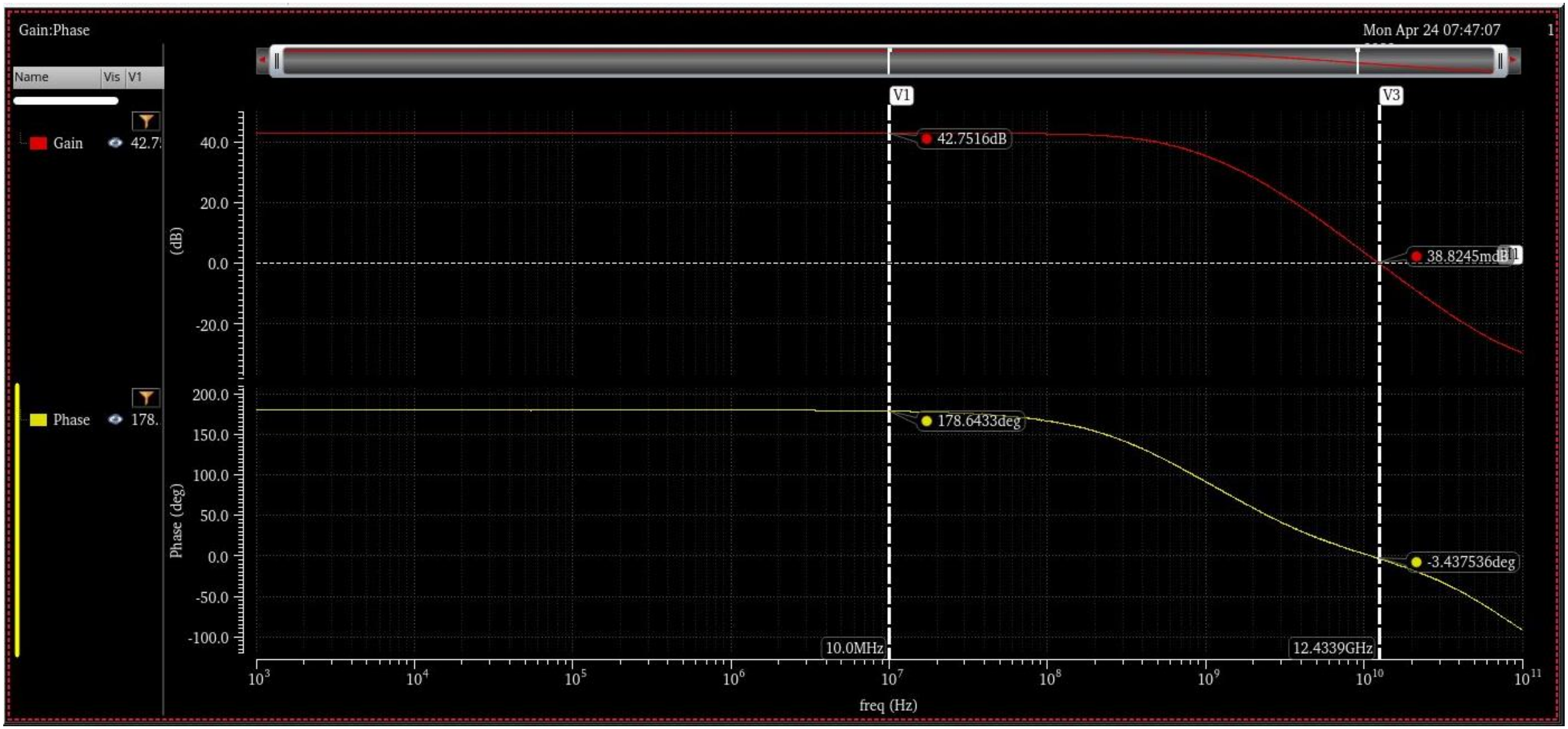
Regarding W/L ratios of the MOSFETS, Increasing the length of the channel will increase its resistance and decrease its transconductance. Increasing the width the channel will increase its transconductance and decrease its resistance, which means that it will be more efficient at amplifying signals and switching between on and off states. However, increasing the width of a MOSFET can also increase its parasitic capacitance. This can limit the MOSFET's high-frequency response and make it more prone to oscillation. Thus, a default length value of 300nM was chosen and width value of 10uM (this was varied arbitrarily for better performance). For the PMOS, I found that a much higher width was necessary, so the number of fingers was increased.

Regarding resistor values, a base value of 1MΩ was chosen for all resistor values at first, and the amplifier had respectable performance. However, the maximum value possible for "rppolywo" is 38.6k, so when the 1MΩ resistors were replaced, the power consumption increased drastically. This was fixed by adding an additional 38.6k resistor to the voltage divider

Final Schematic



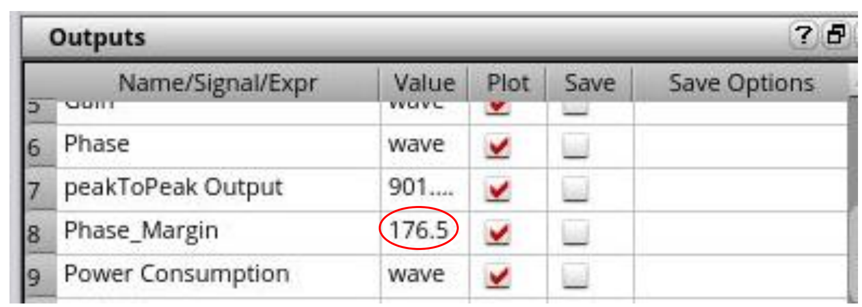
Frequency Response: Gain and Phase Margin



<u>Low Frequency Gain (< 3dB frequency) : 42.751dB</u>

<u>Unity Gain Frequency: 12.4339 GHz</u>

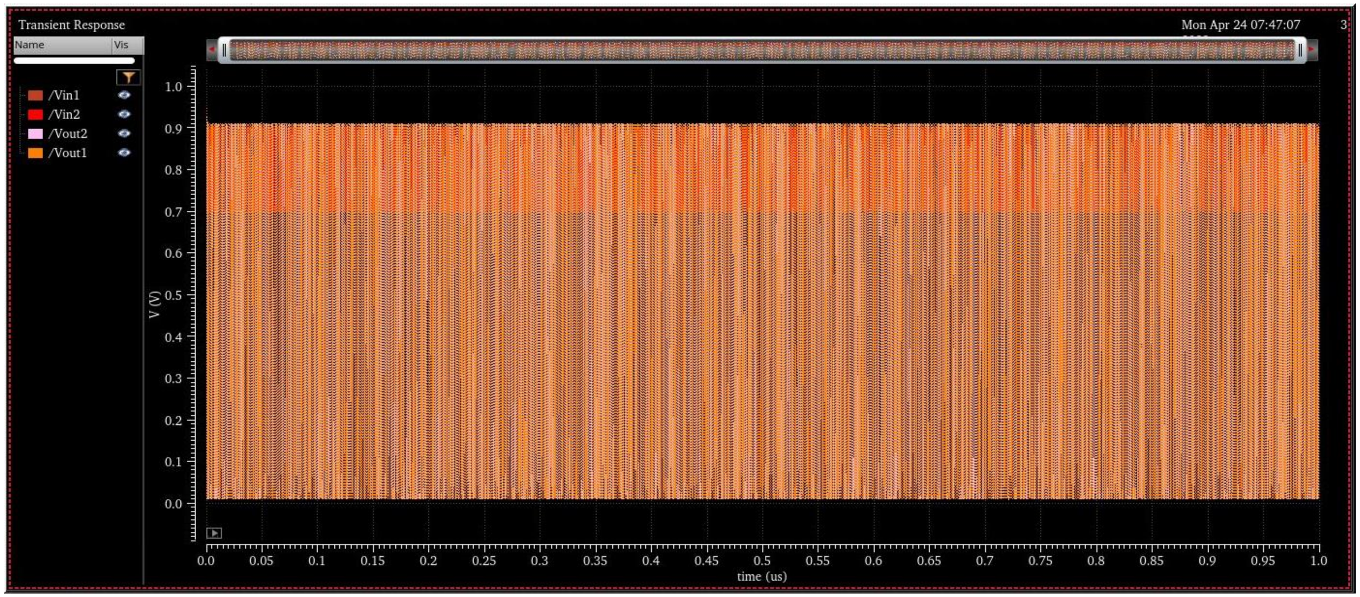
<u>Phase Margin: -3.43+180 = 176.57°</u>

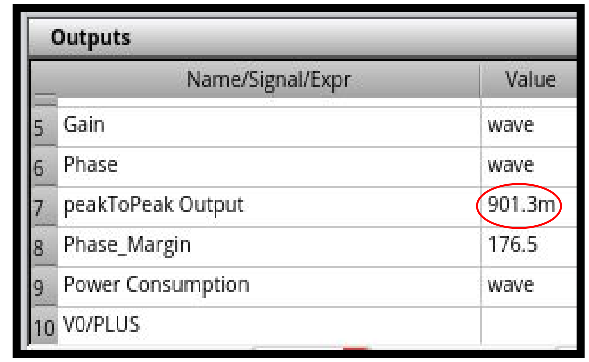


Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
5	Gain	wave	✓		
6	Phase	wave	✓		
7	peakToPeak Output	901....	✓		
8	Phase_Margin	176.5	✓		
9	Power Consumption	wave	✓		

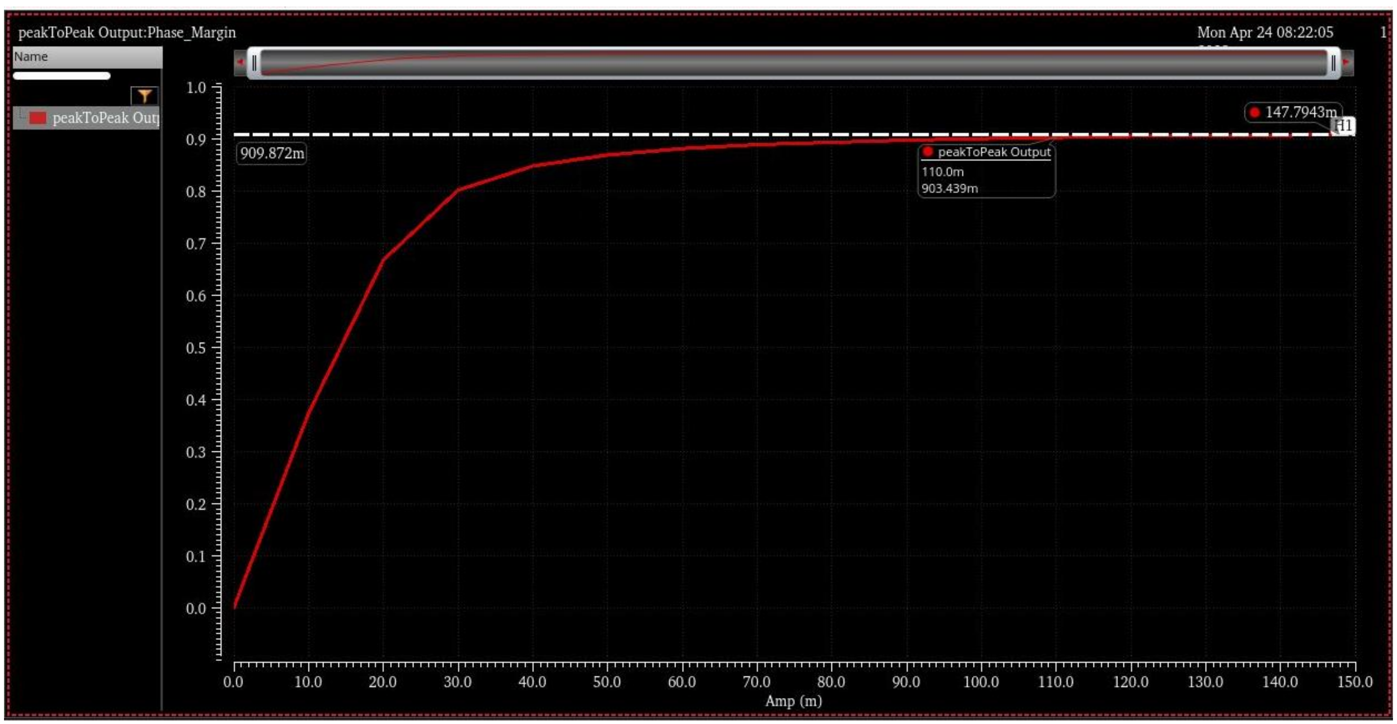
Transient Response: Peak to Peak Amplitude (Single ended)





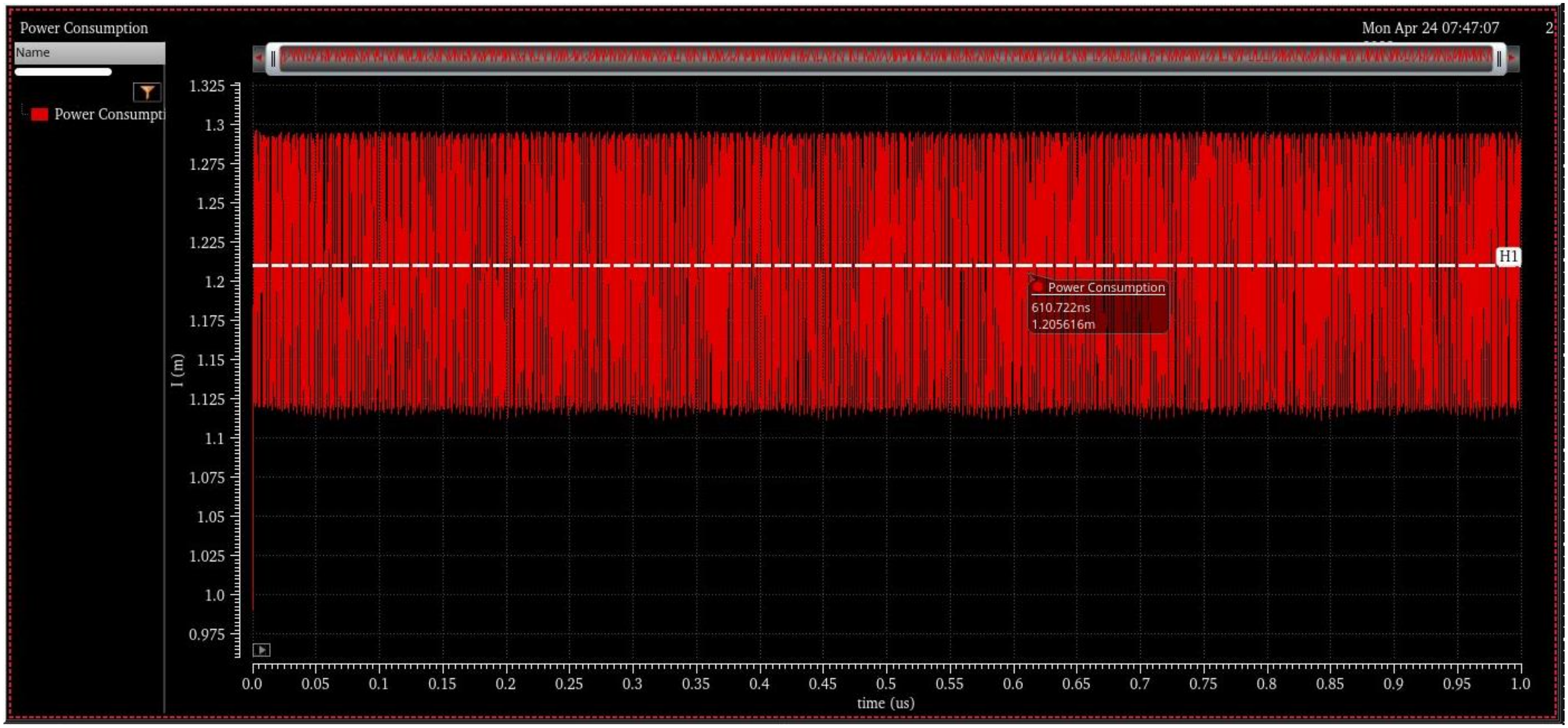
	Name/Signal/Expr	Value
5	Gain	wave
6	Phase	wave
7	peakToPeak Output	901.3m
8	Phase_Margin	176.5
9	Power Consumption	wave
10	VO/PLUS	

Parametric Analysis of Output Swing



<u>**Peak to Peak Amplitude (Single ended): 909mV**</u>

Transient Response: RMS Power Consumption



<u>**Power Consumption: 1.2mW**</u>

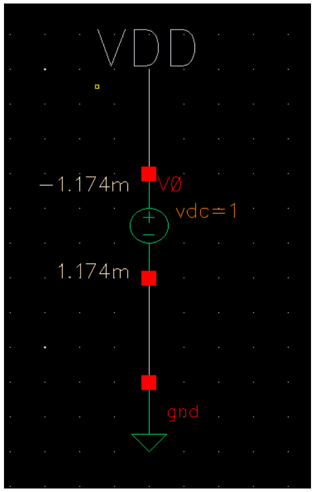


Table of Results:

	Target	Simulation Results
Low Frequency Gain	>40 dB	42.751dB
Unity Gain Frequency	5GHz	12.4339GHz
Phase Margin	>60 °	176.57°
Power Consumption	<4.5mW	1.2mW
Peak to Peak Amplitude (Single ended)	400mV	909mV
LVS Clean	0 errors	N/A
Common Mode Feedback Circuit	R1,R2,R3 provide CMFB for the inner stage and R4 and R5 for the outer stage	