Computer Engineering Department
Faculty of Engineering
Cairo University

Main Requirements

- Synthesize G07 RTL code using an RTL Synthesis tool (Design Compiler)
- [Bonus] Post Synthesis Gate-Level Simulation

General Rules

- Apply timing constraints as given in the lecture on the design (don't forget to set load and drive as well)
- Make sure all of you understand each file in your deliverables, I will ask anyone in anything so better explain to all your team members everything
- Follow a directory structure similar to that given to you in last lecture, I don't want messy files or unprofessional naming for files or variables used in your scripts
- Any missing information will be assumed by you and hence you need to justify why you took these assumptions.

Evaluation Criteria

Here are some guidelines to how the evaluation process will be going to give you some insight about what you need to care about (you will be compared to each other).

- Clock Frequency
- Area
- Scripts Portability (don't use absolute paths)
- Comments
- Directory Structure

Deliverables

- Setup Script file
- Commands log file
- Scripts used for RTL Synthesis
- Constraints file
- Area, timing, constraint and qor reports saved in text files

Due Date and other issues

- Due date for the project will be Monday 14/5/12 10:00 AM (each group on a separate CD in my mailbox)
- Penalties will be applied same way as phase #1 in case of late delivery
- Discussion Date and Schedule will be announced later
- Use your mail and don't send to me a pm using unimasr.