Changes in Components

1. Tri\_state\_bufffer
   * Change the TSB by MUX; to avoid the self-implemented TSB in saed library.
2. Shift
   * Change the variable “shift” by constant number; for simplicity.
3. Set
   * Rearrange the if statements; to reduce its combinations.
4. ROM
   * No changes.
5. Registers
   * No changes.
6. RegDecoder
   * Add a default value to not miss a logic combination; to not add unused Latches.
7. Reg
   * No change
8. RAM
   * Change the default value from ‘Z’ to ‘0’; to not use TSB in saed library.
9. Processor
   * Change the buses to signals, update the components declarations.
10. My\_nDFF
    * No change
11. My\_nadder
    * No change
12. My\_adder
    * Add a signal for “a xor b”; to reduce the number of gates.
13. Mux4x2
    * No change
14. Mux
    * No change
15. Memory
    * Remove Demux, connect IR & MDR direct with RAM output.
16. MemDecoder
    * Change the code to simplified logic circuit; to reduce number of gates.
17. MDDecoder
    * Removed; the outputs was equal to the input so to prevent creating Buffers
18. Logic
    * No change
19. IR
    * No change
20. Inst\_dec
    * Remove the array & change the fault in EQU, NEQ, and EQUI, NEQI.
21. Extend
    * Reduce the conditions by applying common codes in concurrence.
22. DstDecoder
    * Change the code to simplified logic circuit; to reduce number of gates.
23. Demux
    * Removed as no need to separate between MDR & IR (En control both)
24. Decoders
    * Remove MDDecoder, and connect its selectors instead.
25. Decoder5x32
    * No change
26. Arith
    * Change the “add” signal to avoid using buffers or complicated circuit.
27. ALSU
    * No change