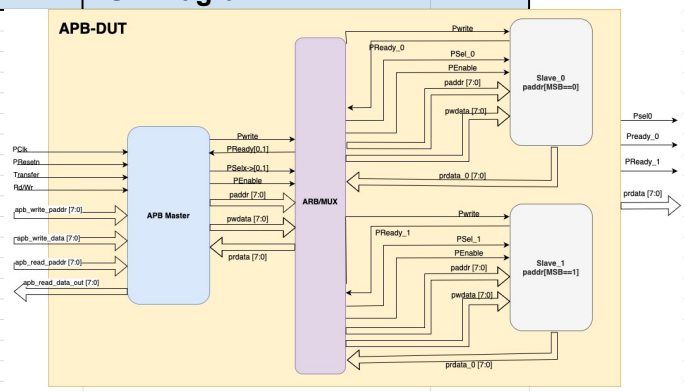
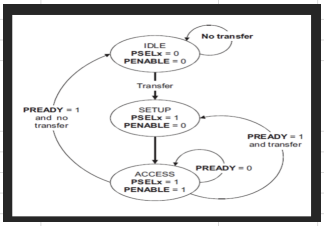
1 DUT Diagram



2 RTL-Signals

No.	Signal Name	Direction	
1	pclk	Input	TOP_in
2	presetn	Input	TOP_in
3	psel_0, psel_1	Output	
4	paddr[31:0]	Input	TOP_in
5	pwdata [31:0]	Input	TOP_in
6	pwrite	Input	TOP_in
7	penable	Input	
8	prdata [31:0]	Output	TOP_in
9	pready	Output	
10	pslaveerror	Output	
11	Transfer	Input	TOP_in

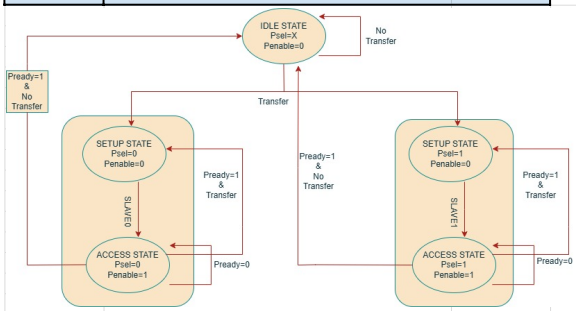
Note: Slave_o and Slave_1 have their own control signals as indicated in DUT Diagram



3 Address Mapping to APB-Slaves

		2^8 = 256		
No	**Address**	**Map To**	**pAddr[MSB]/ pAddr [7]**	PSelx
1	pAddr can Range from [0 to 127]	APB-Slave_0	pAddr[8] == 1'b0;	PSel0
2	pAddr can Range from [128 to 255]	APB-Slave_1	pAddr[8] == 1'b1;	PSel1
	Total: 256 Addresses			

4 Master- 2x Slave FSM



APB Protocol Test Plan

PROJECT TITLE	Verification Of APB- Protocol
PROJECT MANAGER	Priya Ananthkrishanan, Meenal Panasse
PROJECT TEAM	Aman Kumar Gautam, Anindita Mukherjee,Archana Gunasekhar,Harsha Vardhan Reddy, Rishabh S

APB PROTOCOL VERIFICATION TEST PLAN

Summary on APB Protocol

Features:

1. APB stands for Advanced Peripheral Bus
2. APB was developed by ARM (Advanced RISC Machines)
3. It is low bandwidth and low performance bus.
4. It is used for Parallel bus operation.
5. We are using 2 slave design of the APB.
6. Master — Generates APB Transactions[Wr/Rd requests]
7. Slave — Responds to requests based on address mapping

IMPORTANT SIGNALS OF APB:

1	PCLK	Clock Signal used for Synchronisation in APB
2	PRESET	Indicates the readiness of Peripheral Devices. An active low signal
3	PSEL	Select Signal to choose the target slave.We have 1 for each slave
4	PENABLE	Indicates the active state of the transfer. It is an active high signal
5	PWRITE	Indicates the Data Transfer direction
6	PADDR	Specifying the peripheral address
7	PWDATA	Write Data
8	PRDATA	Read Data
9	PREADY	Input signal from the slave. Indicates the readiness of slave for Data Transfer
10	PSLVERR	Indicates transfer failure by the slave
11	TRANSFER	Master transfers only on this signal; when HIGH

USE OF APB:

APB is used to provide interface with the components requiring lower bandwidth like the peripheral devices such as UART, Keypad, Timer and PIO (Peripheral Input Output)

STATUS KEY
On Hold
Not Yet Started
In Progress
Complete

PRIORITY KEY
Low
Medium
High

#1 Test Plan

Tool: Sim- Synopsys VCS/ QuestaS | #DIV/0!

Sl No	STATUS	PRIORITY	TEST CASE NAME	INPUT CONSTRAINTS	EXPECTED OUTPUT	COMMENTS	DESCRIPTION	OWNER	% Coverage	START DATE	END DATE	DURATION
1	Not Started		apb_reset_init_test				Test Reset conditions; Test Control Signal Values;Check IDLE State	Not Assigned				
	Not Started		apb_master_issues_req_to_both_slaves_simultaneously				Arbitration testing	Not Assigned				
			SLAVE_0									
2	Not Started		apb_random_address_write_test_slave_0	pwrite =1,paddr =$urandom, pwdata =$urandom			Exercise Writes to all addresses in Slave_0	Not Assigned				
3	Not Started		apb_random_address_read_test_slave_0	pwrite =0,paddr =$urandom, prdata =$urandom			Exercise Reads to all addresses in Slave_0	Not Assigned				
4	Not Started		apb_address_targetted_write_read_test_slave_0				On a Random address, write known data and read back the same data	Not Assigned				
5	Not Started		apb_single_write_transaction_slave_0				Data written correctly	Not Assigned				
6	Not Started		apb_single_read_transaction_slave_0				data read correctly	Not Assigned				
7	Not Started							Not Assigned				
8	Not Started		apb_write with no wait_slave_0_state_test	pwrite =1,paddr =any specific toaction,pwdata = $urandom (any data) ,penable =1 , psready =1			Apply NO wait state conditions	Not Assigned				
9	Not Started		apb_write with wait_slave_0_state_test	pwrite =1,paddr =any specific toaction,pwdata = $urandom (any data) ,penable =1 , psready =0			Apply wait state conditions	Not Assigned				
10	Not Started		apb_read with no wait_slave_0_state_test	pwrite =0,paddr =any specific toaction,prdata = $urandom (any data) ,penable =1 , psready =1				Not Assigned				
11	Not Started		apb_read with wait_slave_0_state_test	pwrite =0,paddr =any specific toaction,prdata = $urandom (any data) ,penable =1 , psready =0				Not Assigned				
12	Not Started		apb_incremental_addr_write_transaction_slave0				address should be written in increment order	Not Assigned				
13	Not Started		apb_incremental_read_transaction_slave0				data should be read in increment order	Not Assigned				
			SLAVE_1									
13	Not Started		Similar to Slave_1 exercise Test Cases					Not Assigned				
			Protocol Compliance									
	Not Started		apb_handshaking_psel_pen_pready_test					Not Assigned				
	Not Started		apb_master_psel_deasserted_mid_txn					Not Assigned				
	Not Started		apb_slave_delays_pready_random (like a wait state)					Not Assigned				
	Not Started							Not Assigned				
			Negative Test Cases									
12	Not Started		apb_slave_not_responsive_test				Timeout Handling	Not Assigned				0
13	Not Started		apb_wrong_address_access_test				Slave0 && Slave1 Addr	Not Assigned				0
14	Not Started		apb_unexpected_rst_condition_test		applying rst in the middle of Txn	Should return to IDLE state		Not Assigned				0
	Not Started		apb_corrupt_data_test		Master detects incorrect data			Not Assigned				
	Not Started		apb_write_invalid_address_test					Not Assigned				
			Arbitration Test Cases: Slave_0 and Slave_1									
15	Not Started		apb_simultaneous_address_access_test		Access Slave 0 and 1	Temporal access		Not Assigned				
16	Not Started		apb_slave_access_alternating_test				Trying if interleaving can happen	Not Assigned				
17	Not Started		apb_back_to_back_access_test		Txns to same/different slaves			Not Assigned				

#2 Assertion Plan

1	Not Started		A1:-check for presetn,psel is in known state only				Needs 2 Assertions, for Slave_0 and	Not Assigned				
2	Not Started		A2:- Assert pwdata when psel && pwrite is high					Not Assigned				
3	Not Started		A3:- Penable becomes deasserted in next clock cycle when pready is high					Not Assigned				
4	Not Started		A4:-penable has to assert one clock cycle delay when psel;ect goes high					Not Assigned				
5	Not Started		A5:-when penable & psel and pwrite==1'b1 ; assertted pwdata is valid or not we have to check,				Indicates Valid signal for data via pwrite	Not Assigned				
6	Not Started		A6: pReady==0; Hold Penable==1 && Psel==1;					Not Assigned				
7	Not Started		A7: Select Slave 0 for Txn Slave 1 is in IDLE					Not Assigned				
8	Not Started		A8: Select Slave 1 for Txn Slave 0 is in IDLE					Not Assigned				
9	Not Started		A9: PEnable ==0 and PSel ==0 ALways returns IDLE					Not Assigned				

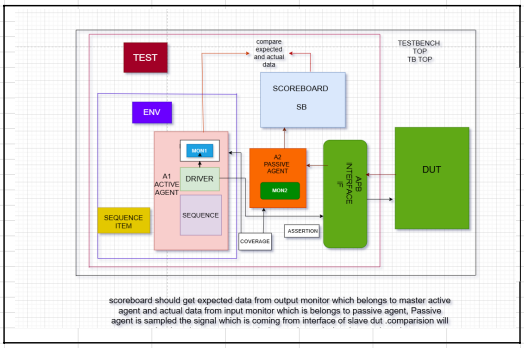
#3 Coverage Plan

Tool: Synopsys Verdi/QuestaSim

	Status		Covergroups	Description	#VALUE!	Signal Name	Bit Size to be Covered	0%	Direction	Comments	Owner	
								This is an example				
1	Not Started		c1:-cover point bins for pwrite (1,0)					0%			Not Assigned	
2	Not Started		c2:-cover point bins for paraddr [Both Slaves]					0%			Not Assigned	
3	Not Started		c3:-cover point bins for pwdata					0%			Not Assigned	
4	Not Started		c4:-cover point bins for prdata					0%			Not Assigned	
5	Not Started		c5:-cover point bins for penable(1,0)					0%			Not Assigned	
6	Not Started	Low	c6:-cover point bins for pready(1,0)					0%			Not Assigned	
7	Not Started	Low	c7:-cross cover for pwrite ==1 x paddr					0%			Not Assigned	
8	Not Started	Low	c8:-cross cover for pwrite ==0 x paddr					0%			Not Assigned	
9	Not Started	Low	c9,c10,c11: FSM States TO be covered					0%			Not Assigned	

UVM TB Architecture

Tool used for TB architecture https://app.diagrams.net/



Feedback: Passive Agent- Monitor A2
Active Agent with DRV MON SEQR A1

Changes to be made:

1. ENV to have both Agents
2. Where is the SEQR?-- We need Seq_item--> Seq--> Seqr
3. Please inidcate TML ports for connections made inside Agent

Notes:

Priya Mentions:

1. If Slave design has error, both slaves reflect the error. Remove and test wrt VIP
2. Loop back with write and read mechanism
3. Replace a slave and connect to master we verify the master

File Structure

```
uvm_apb_tb/
├── tb_top.sv                    // Top-level testbench
│
├── rtl/                         // RTL Design Files
│   ├── apb_master.sv
│   ├── apb_slave.sv
│   ├── apb_bus.sv
│   └── apb_defines.sv
│
├── tb/                          // Testbench Files
│   ├── uvm_pkg.sv               // UVM Package (Includes all TB files)
│   │
│   ├── interface/               // APB Interfaces
│   │   └── apb_if.sv            // APB signal interface
│   │
│   ├── seq_lib/                 // Sequence Library
│   │   ├── apb_base_seq.sv      // Base Sequence
│   │   ├── apb_write_seq.sv     // Write Transaction Sequence
│   │   └── apb_read_seq.sv      // Read Transaction Sequence
│   │
│   │   ├── apb_error_seq.sv     // Error Handling Sequence
│   │
│   ├── agent/                   // Master & Slave Agents
│   │   ├── apb_master_agent.sv  // APB Master Agent          Note: Subjective to change based on TB
│   │   ├── apb_master_driver.sv // APB Master Driver
│   │   ├── apb_master_monitor.sv // APB Master Monitor
│   │   ├── apb_master_sequencer.sv // APB Master Sequencer
│   │   ├── apb_slave_agent.sv   // APB Slave Agent (Common for all slaves)
│   │   ├── apb_slave_driver.sv  // APB Slave Driver
│   │   ├── apb_slave_monitor.sv // APB Slave Monitor
│   │   └── apb_slave_sequencer.sv // APB Slave Sequencer
│   │
│   ├── env/                     // Test Environment
│   │   ├── apb_scoreboard.sv    // Scoreboard (Comparison of expected vs actual)
│   │   ├── apb_coverage.sv      // Coverage Collection
│   │   └── apb_env.sv           // Environment (connects components)
│   │
│   ├── tests/                   // Testcases
│   │   ├── apb_base_test.sv     // Base Test (common setup)
│   │   ├── apb_write_test.sv    // Write Transaction Test
│   │   ├── apb_read_test.sv     // Read Transaction Test
│   │   ├── apb_burst_test.sv    // Burst Test
│   │   ├── apb_reset_test.sv    // Reset During Transaction Test
│   │   ├── apb_arbitration_test.sv // Arbitration and Multi-Slave Test
│   │   └── apb_error_test.sv    // Error Handling Test
│   │
│   └── sim/                     // Simulation Scripts if needed
---------Makefile
```

# No	Task	Owner	Status	Description	ETA	Start Date
1	APB Spec Readup	All	Done	Go through the APB Spec and discuss	2/18/2025	2/18/2025
2	APB-Test Planning	All	Done	Start test plan	2/19/2025	2/20/2025
3	DUT- Diagram	Rishabh	Done		2/19/2025	2/19/2025
4	List Top Signals	Harsha	Done		2/19/2025	2/19/2025
5	Summary of APB	Aman Kumar	Done			2/19/2025
6	Identify Address Mapping	Rishabh	Done		2/19/2025	2/19/2025
7	Identify Test Cases	Rishabh, Harsha	Done		2/20/2025	2/20/2025
8	Identify SVA's	Rishabh, Harsha	Done		2/20/2025	2/20/2025
9	Identify Coverage	Rishabh, Harsha	Done		2/20/2025	2/20/2025
10	UVM Test Bench Architecture	Anindita	In Progress			2/20/2025
11	Directory Structure	Rishabh	Done		2/20/2025	2/20/2025
12	Setup Git Repository	Rishabh	In Progress		2/25/2025	2/19/2025
13	Create a 2 Slave FSM for DUT	Aman Kumar	Done	Custom to given DUT, as a learning curve, create a 2 Slave FSM, Refer to top signals and DUT diagram	2/25/2025	2/25/2025
14	Test Bench Development	All	In Progress			2/25/2025
15	Test Bench File Structure and ENV	Rishabh	In Progress			2/25/2025
16	Environment Bringup	Harsha, Rishabh	Not Started	Have skeletal code ready and empty compile free for Questa Sim		2/25/2025
17						

Status to Meenal

No	Task	Status
1	APB Spec Discussion	Done
2	APB Design requirement understanding	Done
3	DUT Diagram	Done
4	Test Case Plan	Done
5	Assertion Plan	Done
6	Coverage Plan	Done
7	UVM TB Architecture	In Progress
8	File Structure	Done
9	Test Plan Review by Meenal	Done
10	Test Bench Development	Not Started

Skeleton ONLY

No	File Name	Owner	Status	ETA	Notes
1	apb_top.svh	Rishabh	In Progress	2/25/2025	
2	apb_tb_top.sv	Rishabh	Not Started	2/25/2025	
3	apb_test.sv	Rishabh	Not Started	2/25/2025	
4	apb_env.sv	Rishabh	Not Started	2/25/2025	
5	apb_agent_a1.sv	Harsha	Not Started	2/25/2025	
6	apb_agent_a2.sv	Aman Kumar	Not Started	2/25/2025	
7	apb_a1_driver.sv	Harsha	Not Started	2/25/2025	
8	apb_a1_seqr.sv	Harsha	Not Started	2/25/2025	
9	apb_a1_monitor.sv	Harsha	Not Started	2/25/2025	
10	apb_a2_monitor.sv	Aman Kumar	Not Started	2/25/2025	
11	apb_base_sequence.sv	Aman Kumar	Not Started	2/25/2025	
12	apb_write_seq.sv	Aman Kumar	Not Started	2/25/2025	
13	apb_read_seq.sv	Aman Kumar	Not Started	2/25/2025	
14	apb_coverage.sv	Anindita	Not Started	2/25/2025	
15	apb_scoreboard.sv	Anindita	Not Started	2/25/2025	
16	apb_assertions.sv	Anindita	Not Started	2/25/2025	
17				2/25/2025	
18	apb_interface.sv	Anindita	Not Started	2/25/2025	
19	apb_dut.sv	All	Not Started	2/25/2025	
20	apb_dut_master.sv	All	Not Started	2/25/2025	optional, based on DUT