Aman Goel

APPLIED SCIENTIST II, AMAZON WEB SERVICES, USA

Current Position & Contact

Applied Scientist II, AWS Database Systems Lab, Amazon Web Services, USA

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Research Summary

My research explores techniques to automatically check the correctness, reliability, and security of complex hardware and software systems. Recently, I have been working on automatically finding bugs or proving their absence for distributed systems that power modern database and cloud computing services.

EDUCATION

University of Michigan, Ann Arbor, USA

Aug 2016 - Oct 2021

Doctor of Philosophy, Computer Science & Engineering

- Grade Point Average: 3.96/4 - Advisor: Prof. Karem Sakallah
- Dissertation: From Finite to Infinite: Scalable Automatic Verification of Hardware Designs and Distributed Protocols

IIT Madras, India

July 2011 - May 2016 Silver Medalist

Bachelor of Technology, Electrical Engineering Master of Technology, Microelectronics & VLSI

Grade Point Average: 9.23/10

Minor: Industrial Engineering (GPA: 9.33/10)

Research EXPERIENCE

Contributor to P

Dec 2021 - Present

- P is a framework for automatically checking correctness of complex distributed systems
- Developed state-of-the-art systematic testing and model checking techniques
- Finds critical design bugs that could not be found using traditional testing approaches
- Successfully being used by several services teams at Amazon: S3, DynamoDB, MemoryDB

Developer of IC3PO with Karem Sakallah

Nov 2019 - Oct 2021

IC3PO is a tool for automatic push-button verification of distributed protocols

- Automatically generates inductive proofs for high-level distributed protocol specifications
- Uses formal methods and domain regularity to simplify and automate verification tasks
- Enabled other research works: Sift, reTLA, Paxos proof, Bakery proof, and QSM

Developer of AVR with Karem Sakallah

Sep 2016 - Oct 2021

AVR is a tool for automatic verification of complex hardware systems

- Successfully applied on several hardware systems such as RISC-V and industry designs
- Applies automated reasoning with SMT solvers to perform word-level formal verification
- Uses intelligent abstraction techniques to scale property checking
- Won 1st place in the prestigious Hardware Model Checking Competition (HWMCC) 2020 with 7×7 , 1×7 , 1×8 medals

Contributor to Yices with Bruno Dutertre

Intern 2020, SRI, USA

Yices 2 is a state-of-the-art SMT solver from SRI

- Worked with the CSL team and developed techniques for quantified SMT solving
- Developed automated reasoning techniques with a flavor of reinforcement learning

Contributor to JasperGold with Ziyad Hanna

Intern 2019, Cadence, Israel

JasperGold is a state-of-the-art formal verification platform from Cadence

- Developed word-level verification engines for JasperGold
- Developed algorithms for automatically solving hard verification tasks

Incremental Timing Analysis Engine with Nitin Chandrachoodan Dec 2014 - Mar 2015 Won International 3^{rd} place at the TAU Contest, presented at ICCAD 2015

Solar Charger for Hearing Aid Devices

May - July 2013

Won National Award for the Empowerment of Persons with Disabilities 2013

Professional Experience

Full time

- Applied Scientist II, Amazon Web Services, USA	Nov 2021 - Present
- Research Assistant University of Michigan USA	Aug 2016 - Nov 2021

Part time

- Intern, Computer Science Lab, SRI International, USA	May - Aug 2020
– Intern, Systems Verification Group, Cadence, Israel	May - Sep 2019
– Intern, Texas Instruments, India	May - July 2014
– Intern, Flexitron, India	May - July 2013

TEACHING EXPERIENCE

University of Michigan

Masters	EECS 492 Introduction to Artificial Intelligence	Jan - Apr 2020
Masters	EECS 579 Digital System Testing	Aug - Dec 2019
Masters	EECS 478 Logic Synthesis & Optimization	Jan - Apr 2018
Bachelors	EECS 281 Data Structures & Algorithms	Aug - Dec 2017 & 2018

IIT Madras

Masters	EE 5332 Mapping Signal Processing Alg. to DSP Architectures	Jan - May 2016
Masters	EE 5311 Digital IC Design	Aug - Nov 2015

Research Service

Artifact evaluation committee member for CAV 2023, SOSP 2021, MICRO 2021, OSDI 2021, VMCAI 2021, OOPSLA 2020, CAV 2020

RESEARCH PUBLICATIONS

SAT-Based Quantified Symmetric Minimization of the Reachable States of Distributed Protocols Katalin Fazekas, Aman Goel, Karem Sakallah. In Formal Methods in Computer-Aided Design (FMCAD), 2023.

- Towards an Automatic Proof of the Bakery Algorithm

 Aman Goel, Stephan Merz, Karem Sakallah. In International Conference on Formal Techniques for Distributed Objects, Components, and Systems (FORTE), 2023.
- Regularity and quantification: a new approach to verify distributed protocols

 Aman Goel, Karem A Sakallah. In Special Issue: Selected Extended Papers of NFM 2021 at
 Innovations in Systems and Software Engineering, A NASA Journal (ISSE), 2022.
- Sift: Using Refinement-guided Automation to Verify Complex Distributed Systems
 Haojun Ma, Hammad Ahmad, Aman Goel, Eli Goldweber, Jean-Baptiste Jeannin, Manos Kapritsos,
 and Baris Kasikci. In USENIX Annual Technical Conference (ATC), 2022.
- reTLA: Towards an automatic transpiler from TLA+ to VMT

 Jure Kukovec, Aman Goel, Igor Konnov, Stephan Merz, Karem Sakallah. In TLA+ Conference

 (TLA+ Conf), 2022.
- Towards an Automatic Proof of Lamport's Paxos

 * featured in Y combinator

 Aman Goel, and Karem Sakallah. In Formal Methods in Computer-Aided Design (FMCAD), 2021.
- On Symmetry and Quantification: A New Approach to Verify Distributed Protocols
 Aman Goel, and Karem Sakallah. In NASA Formal Methods Symposium (NFM), 2021.
- AVR: Abstractly Verifying Reachability

 Aman Goel, and Karem Sakallah. In International Conference on Tools and Algorithms for the

Construction and Analysis of Systems (TACAS), 2020.

- Model checking of Verilog RTL using IC3 with syntax-guided abstraction
 Aman Goel, and Karem Sakallah. In NASA Formal Methods Symposium (NFM), 2019.
- L4: Incremental Inference of Inductive Invariants for Verification of Distributed Protocols
 Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A.
 Sakallah. In the 27th Symposium on Operating Systems Principles (SOSP), 2019.
- Towards Automatic Inference of Inductive Invariants
 Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In the Workshop on Hot Topics in Operating Systems (HotOS), 2019.
- Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs
 Aman Goel, and Karem Sakallah. In Design, Automation & Test in Europe (DATE), 2019.
- iitRACE: A memory efficient engine for fast incremental timing analysis
 Peddawad, Chaitanya, Aman Goel, B. Dheeraj, and Nitin Chandrachoodan. In IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2015.
- Solar Charger for Rechargeable Batteries Used in Hearing Aid Devices
 Aman Goel. In International Journal of Engineering Science and Innovative Technology (IJESIT),
 2013.

Awards

- Recipient of Rackham Predoctoral Fellowship 2020 for outstanding PhD research
- Best student research award in the hardware discipline in the CSE Graduate Student Honors
 Competition 2019 for outstanding PhD research
- Recipient of Dwight F. Benton fellowship at University of Michigan for 2016-17
- Branch position 2 in Electrical Engineering at IIT Madras (Silver medalist)
- Won international 3rd place in TAU Contest at ICCAD 2015 for Incremental Timing Analysis
- Recipient of best undergraduate research project at Pan IIT Research Expo 2014
- Recipient of *Electronics for You* prize for best academic performance at the graduate level
- Won National Award for the Empowerment of Persons with Disabilities 2013
- Invited participant as a visiting graduate student at Simons Institute, Spring 2021
- Invited participant at Summer School on Formal Techniques 2018 hosted by SRI

Press

■ Y Combinator

My work on automatically proving Paxos featured in **top 10 posts** of the week at Y Combinator, attracting 159 points and 68 comments

■ U-M Code Blue

My tools AVR and I4 got an article in Code Blue, the annual publication from CSE at the University of Michigan which highlights high-impact work

- The Michigan Engineer News Center
 Hardware model checker takes gold at international competition
- The Michigan Engineer News Center
 Predoctoral Fellowship for mathematically provable hardware design
- The Michigan Engineer News Center
 2019 CSE Graduate Student Honors Competition highlights outstanding research
- IIT Madras Newsletter

 The team iitRACE from IIT Madras has won the 3rd place at the programming contest conducted by the TAU Workshop, Monterey, CA, 2015

Skills

- Expert in Java, Python, C#, C++, C, Shell scripting
- Working knowledge of MATLAB, HTML, LLVM, Verilog
- Good understanding of SAT & SMT solvers

Research Talks

- Towards an Automatic Proof of Lamport's Paxos
 Conference talk at Formal Methods in Computer-Aided Design (FMCAD), Virtual, October 2021.
- On Symmetry and Quantification: A New Approach to Verify Distributed Protocols Workshop talk at Satisfiability Modulo Theories Workshop (SMT), Virtual, July 2021.

Push-Button Verification with Provable Assurance
Talk at Amazon Web Services Automated Reasoning Group, Virtual, June 2021.

On Symmetry and Quantification: A New Approach to Verify Distributed Protocols Conference Talk at NASA Formal Methods Symposium (NFM), Virtual, May 2021.

E-matching + Reinforcement Learning for Quantified UF Solving in Yices Intern talk at SRI CSL team, Virtual, August 2020.

One-click Verification with Provable Assurance Talk at SRI CSL team, Virtual, July 2020.

Evaluation of Word-level Model Checking Engine AVR in JasperGold Talk at Cadence SVG team, Haifa, Israel, August 2019.

Model checking of Verilog RTL using IC3 with syntax-guided abstraction Conference talk at NASA Formal Methods Symposium (NFM), Rice University, Houston, May 2019.

Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs Conference talk at Design, Automation & Test in Europe (DATE), Florence, Italy, March 2019.