

AMAN GOEL

Ph.D. Candidate, Computer Science & Engineering, University of Michigan

BASIC INFORMATION

4th Year Ph.D. Candidate (adviser: Prof. [Karem Sakallah](#))
Formal Methods & Automated Reasoning Group, CSE
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RESEARCH INTERESTS

My research interests include exploring reliability & security of complex systems, and developing automated reasoning algorithms for ensuring system correctness. I also have a developing interest in distributed systems, data structures & algorithms, programming languages, machine learning and web systems. My current work focuses on automatic verification of distributed systems.

EDUCATION

University of Michigan, Ann Arbor, USA
Ph.D. student, Computer Science & Engineering
Grade Point Average: **3.96/4**

Aug 2016 - Present

IIT Madras, India
Bachelor of Technology, Electrical Engineering
Master of Technology, Microelectronics & VLSI
- Grade Point Average: **9.23/10**
- Minor: Industrial Engineering (GPA: 9.33/10)

July 2011 - May 2016
Silver Medalist

RECENT RESEARCH EXPERIENCE

Developer of *I4*

Aug 2018 - Present

I4 is a tool for automatic, push-button verification of distributed systems
– Performs automated correctness checking and bug-hunting for distributed systems
– Uses formal methods and symmetry to simplify and automate verification tasks
– Uses state-of-the-art SMT solvers ([Z3](#), [Yices 2](#)) to derive proof guarantees or to compute counterexample traces

Developer of *AVR*

Sep 2016 - Present

AVR is a tool for automatic verification of state-transition systems
– Successfully applied on hardware and software systems
– Uses SMT solvers to perform word-level formal verification
– Uses data abstraction for scaling unbounded property verification
– Won 1st place in the BV track and 2nd place in the ABV track at the prestigious Hardware Model Checking Competition ([HWMCC](#)) 2019

Contributor to Open-source Tools

Sep 2016 - Present

[Yices 2](#) - a state-of-the-art SMT solver
[Yosys](#) - an open-source framework for design synthesis

Contributor to Commercial Tools

Summer 2019 @ Haifa, Israel

[JasperGold](#)
– A state-of-the-art formal verification platform from [Cadence](#)
– Developed word-level verification engines for JasperGold
– Worked with Cadence SVG (systems verification group) and developed algorithms for automatically solving hard verification tasks

RECENT SERVICE

CAV AEC

2019 - Present

Invited member of artifact evaluation committee for 32nd International Conference on Computer-Aided Verification (CAV) 2020

SKILLS	<p>Good knowledge of <i>C++</i>, <i>C</i>, <i>Python</i>, <i>Verilog</i>, <i>Shell scripting</i></p> <p>Working knowledge of <i>MATLAB</i>, <i>Java</i>, <i>HTML</i>, <i>LLVM</i></p> <p>Good understanding of <i>SAT</i> / <i>SMT solvers</i></p>		
SELECTED PUBLICATIONS	<p> <i>I4: Incremental Inference of Inductive Invariants for Verification of Distributed Protocols</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the 27th Symposium on Operating Systems Principles (<i>SOSP</i>), ACM, 2019.</p> <p> <i>Towards Automatic Inference of Inductive Invariants</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the Workshop on Hot Topics in Operating Systems (<i>HotOS</i>), pp. 30-36. ACM, 2019.</p> <p> <i>Model checking of Verilog RTL using IC3 with syntax-guided abstraction</i> Aman Goel, and Karem Sakallah. In NASA Formal Methods Symposium (<i>NFM</i>), pp. 166-185. Springer, Cham, 2019.</p> <p> <i>Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs</i> Aman Goel, and Karem Sakallah. In 2019 Design, Automation & Test in Europe Conference & Exhibition (<i>DATE</i>), pp. 618-621. IEEE, 2019.</p> <p> <i>iitRACE: A memory efficient engine for fast incremental timing analysis and clock pessimism removal</i> Peddawad, Chaitanya, Aman Goel, B. Dheeraj, and Nitin Chandrachoodan. In 2015 IEEE/ACM International Conference on Computer-Aided Design (<i>ICCAD</i>), pp. 903-909. IEEE, 2015.</p>		
HONORS & AWARDS	<ul style="list-style-type: none"> – Recipient of Dwight F. Benton fellowship at University of Michigan for 2016-17 – Recipient of research travel grant and Israel travel award for 2019 – Branch position 2 in Electrical Engineering at IIT Madras (<i>Silver medalist</i>) – Won international 3rd place in TAU Contest at <i>ICCAD</i> 2015 for Incremental Timing Analysis – Recipient of <i>best undergraduate research project</i> at Pan IIT Research Expo 2014 – Recipient of <i>Electronics for You</i> prize for best academic performance at graduate level – Won <i>National Award</i> for the Empowerment of Persons with Disabilities 2013 for Solar Charger for Hearing Aid Devices 		
SELECTED COURSES	<p>University of Michigan</p> <ul style="list-style-type: none"> - <i>Advanced Algorithms</i> - <i>Advanced Compilers</i> - <i>Formal Verification</i> - <i>AI Foundations</i> - <i>Web Systems</i> <p>IIT Madras</p> <p>Computer Science:</p> <ul style="list-style-type: none"> - <i>Data Structures & Algorithms</i> - <i>Design Verification</i> - <i>Computational Engineering</i> - <i>Digital Systems Testing</i> - <i>Computer Organisation</i> - <i>CAD Systems</i> <p>Mathematics & Operations Research:</p> <ul style="list-style-type: none"> - <i>Combinatorial Optimization</i> - <i>Probability Foundations</i> - <i>Fundamentals of Operational Research</i> - <i>Decision Modelling</i> 		

TEACHING EXPERIENCE	<i>University of Michigan:</i>	
	EECS 281 Data Structures & Algorithms	<i>Aug - Dec 2017 & 2018</i>
	EECS 478 Logic Synthesis & Optimization	<i>Jan - Apr 2018</i>
	EECS 579 Digital System Testing	<i>Aug - Dec 2019</i>
	<i>IIT Madras:</i>	
	EE 5311 Digital IC Design	<i>Aug - Nov 2015</i>
	EE 5332 Mapping Signal Processing Algorithms to DSP Architectures	<i>Jan - May 2016</i>
FORMER ACTIVITIES	– <i>SSFT: Summer School on Formal Techniques</i> <i>Summer 2018 @ Menlo Park, CA</i>	
	Invited participant at Summer School on Formal Techniques 2018 hosted by SRI	
	– <i>MPUC: Compiler for Memristor Arrays</i> <i>Jan - Apr 2017</i>	
	Developed a compiler for coarse-grained architecture of memristor arrays	
	– <i>Radiation Pattern Measurement System for Automotive Radar</i> <i>May - July 2014</i>	
	Wireless Connectivity Solutions, Texas Instruments , India	
	Developed an automatic radar positioning system for radar modules testing	
	– <i>Voice to Text Converter</i> <i>Mar 2013</i>	
	Developed software that converts voice input in a language to text field in other chosen language using available softwares of Google Voice Recognition and Google Translate	
OTHERS	– <i>U-M Mentorship program</i> <i>2016 - Present</i>	
	Encourage and guide undergraduate students towards CS major, programming and graduate studies	
	– Voluntary blood donor	
HOBBIES	Swimming, Water Polo, Skating (ice & roller), Soccer	