# Aman Goel

*Ph.D. Candidate, Computer Science & Engineering, University of Michigan*


**Basic Information**

$5^{th}$ Year Ph.D. Candidate (adviser: Prof. Karem Sakallah)
Formal Methods & Automated Reasoning Group, CSE
University of Michigan, Ann Arbor, USA

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**Research Interests**

My research interests include exploring reliability & security of complex systems, and developing automated reasoning algorithms for ensuring system correctness. I also have a developing interest in data structures & algorithms, programming languages, machine learning and web systems. My current work focuses on automatic verification of distributed systems.

**Education**

**University of Michigan**, Ann Arbor, USA — *Aug 2016 - Present*
*Ph.D. student*, Computer Science & Engineering
Grade Point Average: **3.96/4**

**IIT Madras**, India — *July 2011 - May 2016*
*Bachelor of Technology*, Electrical Engineering — *Silver Medalist*
*Master of Technology*, Microelectronics & VLSI

- Grade Point Average: **9.23/10**
- Minor: Industrial Engineering (GPA: 9.33/10)

**Recent Research Experience**

**Developer of *AVR*** — *Sep 2016 - Present*
AVR is a tool for automatic verification of state-transition systems
– Successfully applied on hardware and software systems
– Uses SMT solvers to perform word-level formal verification
– Uses data abstraction for scaling unbounded property verification
– Won $1^{st}$ place in the prestigious Hardware Model Checking Competition (HWMCC) 2020 – 7 x 🥇, 1 x 🥈, 1 x 🥉 medals

**Developer of *IC3PO*** — *Nov 2019 - Present*
IC3PO is a tool for automatic, push-button verification of distributed systems
– Performs automated correctness checking and bug-hunting for distributed systems
– Uses formal methods and symmetry to simplify and automate verification tasks
– Generates quantified inductive invariants with both universal and existential quantifiers

**Contributor to Open-source Tools** — *Summer 2020 @ Menlo Park, CA*
Yices 2 is a state-of-the-art SMT solver from SRI
– Worked with the CSL team and developed techniques for quantified SMT solving

**Contributor to Commercial Tools** — *Summer 2019 @ Haifa, Israel*
JasperGold is a state-of-the-art formal verification platform from Cadence
– Developed word-level verification engines for JasperGold
– Worked with Cadence SVG (systems verification group) and developed algorithms for automatically solving hard verification tasks

**Recent Service**

Artifact evaluation committees (AEC) — *2019 - Present*
**OSDI 2021**, **VMCAI 2021**, **OOPSLA 2020**, **CAV 2020**

**Skills**

Good knowledge of *C++, C, Python, Verilog, Shell scripting*
Working knowledge of *MATLAB, Java, HTML, LLVM*
Good understanding of *SAT / SMT solvers*

## Selected Publications

*On Symmetry and Quantification: A New Approach to Verify Distributed Protocols*
**Aman Goel**, and Karem Sakallah. In NASA Formal Methods Symposium (*NFM*), 2021.

*AVR: Abstractly Verifying Reachability*
**Aman Goel**, and Karem Sakallah. In International Conference on Tools and Algorithms for the Construction and Analysis of Systems (*TACAS*), 2020.

*I4: Incremental Inference of Inductive Invariants for Verification of Distributed Protocols*
Ma, Haojun, **Aman Goel**, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In the 27th Symposium on Operating Systems Principles (*SOSP*), 2019.

*Towards Automatic Inference of Inductive Invariants*
Ma, Haojun, **Aman Goel**, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In the Workshop on Hot Topics in Operating Systems (*HotOS*), 2019.

*Model checking of Verilog RTL using IC3 with syntax-guided abstraction*
**Aman Goel**, and Karem Sakallah. In NASA Formal Methods Symposium (*NFM*), 2019.

*Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs*
**Aman Goel**, and Karem Sakallah. In 2019 Design, Automation & Test in Europe Conference & Exhibition (*DATE*), 2019.

*iitRACE: A memory efficient engine for fast incremental timing analysis*
Peddawad, Chaitanya, **Aman Goel**, B. Dheeraj, and Nitin Chandrachoodan. In 2015 IEEE/ACM International Conference on Computer-Aided Design (*ICCAD*), 2015.

## Honors & Awards

- Recipient of **Rackham Predoctoral Fellowship** 2020-21 for outstanding PhD research
- Best student research award in the hardware discipline in the **CSE Graduate Student Honors Competition** 2019 for outstanding PhD research
- Recipient of Dwight F. Benton fellowship at University of Michigan for 2016-17
- Recipient of research travel grant and Israel travel award for 2019
- Branch position 2 in Electrical Engineering at IIT Madras (*Silver medalist*)
- Won international $3^{rd}$ place in TAU Contest at ICCAD 2015 for Incremental Timing Analysis
- Recipient of *best undergraduate research project* at Pan IIT Research Expo 2014
- Recipient of *Electronics for You* prize for best academic performance at graduate level
- Won *National Award* for the Empowerment of Persons with Disabilities 2013 for Solar Charger for Hearing Aid Devices
- Invited participant at Summer School on Formal Techniques 2018 hosted by SRI

## Selected Courses

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| *Advanced Algorithms* | *Advanced Compilers* | *Formal Verification* |
| *AI Foundations* | *Data Structures & Alg.* | *Digital Systems Testing* |

## Teaching Experience

*University of Michigan*:

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|---|---|
| EECS 281 Data Structures & Algorithms | *Aug - Dec 2017 & 2018* |
| EECS 478 Logic Synthesis & Optimization | *Jan - Apr 2018* |
| EECS 579 Digital System Testing | *Aug - Dec 2019* |
| EECS 492 Introduction to Artificial Intelligence | *Jan - Apr 2020* |

*IIT Madras*:

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|---|---|
| EE 5311 Digital IC Design | *Aug - Nov 2015* |
| EE 5332 Mapping Signal Processing Algorithms to DSP Architectures | *Jan - May 2016* |

## Hobbies

Swimming, Water Polo, Skating, Badminton, Soccer