

AMAN GOEL

Ph.D. Candidate, Computer Science & Engineering, University of Michigan

BASIC INFORMATION

5th Year Ph.D. Candidate (adviser: Prof. [Karem Sakallah](#))
Formal Methods & Automated Reasoning Group, CSE
University of Michigan, Ann Arbor, USA

amangoel@umich.edu
+1 (734) 881-0674
[aman-goel.github.io](https://github.com/aman-goel)



RESEARCH INTERESTS

My research interests include exploring reliability & security of complex systems, and developing automated reasoning algorithms for ensuring system correctness. I also have a developing interest in data structures & algorithms, programming languages, machine learning and web systems. My current work focuses on automatic verification of complex systems.

EDUCATION

University of Michigan, Ann Arbor, USA
Ph.D. student, Computer Science & Engineering
Grade Point Average: **3.96/4**

Aug 2016 - Present

IIT Madras, India
Bachelor of Technology, Electrical Engineering
Master of Technology, Microelectronics & VLSI
- Grade Point Average: **9.23/10**
- Minor: Industrial Engineering (GPA: 9.33/10)

July 2011 - May 2016
Silver Medalist

RECENT RESEARCH EXPERIENCE



Developer of *AVR*

Sep 2016 - Present

- AVR is a tool for automatic verification of state-transition systems
- Successfully applied on hardware and software systems
- Uses SMT solvers to perform word-level formal verification
- Uses data abstraction for scaling unbounded property verification
- Won 1st place in the prestigious Hardware Model Checking Competition (**HWMCC**) 2020



Developer of *I4*

Aug 2018 - Present

- I4 is a tool for automatic, push-button verification of distributed systems
- Performs automated correctness checking and bug-hunting for distributed systems
- Uses formal methods and symmetry to simplify and automate verification tasks

Contributor to Open-source Tools

Summer 2020 @ Menlo Park, CA

- Yices 2**
- A state-of-the-art SMT solver from **SRI**
- Worked with the **CSL** team and developed techniques for quantified SMT solving

Contributor to Commercial Tools

Summer 2019 @ Haifa, Israel

- JasperGold**
- A state-of-the-art formal verification platform from **Cadence**
- Developed word-level verification engines for JasperGold
- Worked with Cadence SVG (systems verification group) and developed algorithms for automatically solving hard verification tasks

RECENT SERVICE







Artifact evaluation committees (AEC)

2019 - Present

VMCAI'21: Conference on Verification, Model Checking, and Abstract Interpretation

OOPSLA'20: Conference on Object-Oriented Programming Systems, Languages, and Apps

CAV'20: Conference on Computer-Aided Verification

SKILLS	<p>Good knowledge of <i>C++</i>, <i>C</i>, <i>Python</i>, <i>Verilog</i>, <i>Shell scripting</i> Working knowledge of <i>MATLAB</i>, <i>Java</i>, <i>HTML</i>, <i>LLVM</i> Good understanding of <i>SAT</i> / <i>SMT solvers</i></p>		
SELECTED PUBLICATIONS	<p> <i>AVR: Abstractly Verifying Reachability</i> Aman Goel, and Karem Sakallah. In International Conference on Tools and Algorithms for the Construction and Analysis of Systems (<i>TACAS</i>), 2020 (to appear).</p> <p> <i>I4: Incremental Inference of Inductive Invariants for Verification of Distributed Protocols</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the 27th Symposium on Operating Systems Principles (<i>SOSP</i>), ACM, 2019.</p> <p> <i>Towards Automatic Inference of Inductive Invariants</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the Workshop on Hot Topics in Operating Systems (<i>HotOS</i>), pp. 30-36. ACM, 2019.</p> <p> <i>Model checking of Verilog RTL using IC3 with syntax-guided abstraction</i> Aman Goel, and Karem Sakallah. In NASA Formal Methods Symposium (<i>NFM</i>), pp. 166-185. Springer, Cham, 2019.</p> <p> <i>Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs</i> Aman Goel, and Karem Sakallah. In 2019 Design, Automation & Test in Europe Conference & Exhibition (<i>DATE</i>), pp. 618-621. IEEE, 2019.</p> <p> <i>iitRACE: A memory efficient engine for fast incremental timing analysis and clock pessimism removal</i> Peddawad, Chaitanya, Aman Goel, B. Dheeraj, and Nitin Chandrachoodan. In 2015 IEEE/ACM International Conference on Computer-Aided Design (<i>ICCAD</i>), pp. 903-909. IEEE, 2015.</p>		
HONORS & AWARDS	<ul style="list-style-type: none"> – Recipient of Rackham Predoctoral Fellowship 2020-21 for outstanding PhD research – Runner-up finalist of the CSE Graduate Student Honors Competition 2019 for outstanding PhD research for <i>Push-button Verification using Abstraction and Induction</i> – Recipient of Dwight F. Benton fellowship at University of Michigan for 2016-17 – Recipient of research travel grant and Israel travel award for 2019 – Branch position 2 in Electrical Engineering at IIT Madras (<i>Silver medalist</i>) – Won international 3rd place in TAU Contest at ICCAD 2015 for Incremental Timing Analysis – Recipient of <i>best undergraduate research project</i> at Pan IIT Research Expo 2014 – Recipient of <i>Electronics for You</i> prize for best academic performance at graduate level – Won <i>National Award</i> for the Empowerment of Persons with Disabilities 2013 for Solar Charger for Hearing Aid Devices 		
SELECTED COURSES	<p>University of Michigan</p> <ul style="list-style-type: none"> - <i>Advanced Algorithms</i> - <i>Advanced Compilers</i> - <i>Formal Verification</i> - <i>AI Foundations</i> - <i>Web Systems</i> <p>IIT Madras</p> <p>Computer Science:</p>		

	<ul style="list-style-type: none"> - <i>Data Structures & Algorithms</i> - <i>Computational Engineering</i> 	<ul style="list-style-type: none"> - <i>Design Verification</i> - <i>Digital Systems Testing</i>
	Mathematics & Operations Research:	
	<ul style="list-style-type: none"> - <i>Combinatorial Optimization</i> - <i>Fundamentals of Operational Research</i> 	<ul style="list-style-type: none"> - <i>Probability Foundations</i> - <i>Decision Modelling</i>
TEACHING EXPERIENCE	<p><i>University of Michigan:</i></p> <p>EECS 281 Data Structures & Algorithms</p> <p>EECS 478 Logic Synthesis & Optimization</p> <p>EECS 579 Digital System Testing</p> <p>EECS 492 Introduction to Artificial Intelligence</p> <p><i>IIT Madras:</i></p> <p>EE 5311 Digital IC Design</p> <p>EE 5332 Mapping Signal Processing Algorithms to DSP Architectures</p>	<p><i>Aug - Dec 2017 & 2018</i></p> <p><i>Jan - Apr 2018</i></p> <p><i>Aug - Dec 2019</i></p> <p><i>Jan - Apr 2020</i></p> <p><i>Aug - Nov 2015</i></p> <p><i>Jan - May 2016</i></p>
FORMER ACTIVITIES	<ul style="list-style-type: none"> - <i>Summer School on Formal Techniques</i> - <i>Invited participant at Summer School on Formal Techniques 2018 hosted by SRI</i> - <i>MPUC: Compiler for Memristor Arrays</i> - <i>Radiation Pattern Measurement System for Automotive Radar</i> - <i>Voice to Text Converter</i> 	<p><i>Summer 2018 @ Menlo Park, CA</i></p> <p><i>Jan - Apr 2017</i></p> <p><i>May - July 2014</i></p> <p><i>Mar 2013</i></p>
OTHERS	<ul style="list-style-type: none"> - <i>U-M Mentorship program</i> - <i>Voluntary blood donor</i> 	<p><i>2016 - Present</i></p>
HOBBIES	Swimming, Water Polo, Skating (ice & roller), Soccer	