

CURRICULUM VITAE

Aman Goel *Ph.D. Student, CSE, University of Michigan*

BASIC INFORMATION	4 th Year Ph.D. Student (adviser: Prof. Karem Sakallah) Computer Science & Engineering University of Michigan, Ann Arbor, USA	Phone: +1-734-881-0674 Email: amangoel@umich.edu Webpage: aman-goel.github.io
MAILING ADDRESS	1929 Plymouth Road, Apt 1022, Ann Arbor, MI - 48105, USA	
RESEARCH INTERESTS	My research interests include exploring reliability & security of complex systems, and developing automated reasoning algorithms for ensuring system correctness. I also have a keen interest in programming languages, data structures & algorithms, machine learning and web systems. My current work focuses on automatic verification of distributed systems.	
EDUCATION	University of Michigan , Ann Arbor, USA <i>Ph.D. student, Computer Science & Engineering</i> Grade Point Average: 3.96/4	<i>Aug 2016 - Present</i>
	IIT Madras , India <i>Bachelor of Technology</i> , Electrical Engineering <i>Master of Technology</i> , Microelectronics & VLSI - Grade Point Average: 9.23/10 - Minor: Industrial Engineering (GPA: 9.33/10)	<i>July 2011 - May 2016</i>
RECENT RESEARCH EXPERIENCE	Developer of I4 I4 is a tool for automatic, push-button verification of distributed systems - Performs automated correctness checking and bug-hunting for distributed systems - Uses formal methods and symmetry to simplify and automate verification tasks - Uses state-of-the-art SMT solvers (Z3 , Yices 2) to derive proof guarantees or to compute counterexample traces	<i>Aug 2018 - Present</i>
	Developer of AVR AVR is a tool for automatic verification of state-transition systems - Successfully applied on hardware and software systems - Uses SMT solvers to perform word-level formal verification - Uses data abstraction for scaling unbounded property verification	<i>Sep 2016 - Present</i>
	Contributor to Open-source Tools Yices 2 - a state-of-the-art SMT solver Yosys - an open-source framework for design synthesis	<i>Sep 2016 - Present</i>
	Contributor to Commercial Tools JasperGold - A state-of-the-art formal verification platform from Cadence - Developed word-level verification engines for JasperGold - Worked with Cadence SVG (systems verification group) and developed algorithms for automatically solving hard verification tasks	<i>Summer 2019 @ Haifa, Israel</i>
	Others CAV 2020 AEC - Member of artifact evaluation committee (AEC) for International Conference on Computer-Aided Verification (CAV) 2020	<i>2019 - Present</i>
	SSFT 2018 - Invited participant at Summer School on Formal Techniques (SSFT) 2018 hosted by SRI	<i>Summer 2018 @ Menlo Park, CA</i>

SKILLS	Good knowledge of C++, C, Python, Verilog, Shell scripting Working knowledge of MATLAB, Java, HTML, CSS, JavaScript, SQL, LLVM Good understanding of SAT / SMT solvers																		
SELECTED PUBLICATIONS	<p><i>I4: Incremental Inference of Inductive Invariants for Verification of Distributed Protocols</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the 27th Symposium on Operating Systems Principles (<i>SOSP</i>), ACM, 2019.</p> <p><i>Towards Automatic Inference of Inductive Invariants</i> Ma, Haojun, Aman Goel, Jean-Baptiste Jeannin, Manos Kapritsos, Baris Kasikci, and Karem A. Sakallah. In Proceedings of the Workshop on Hot Topics in Operating Systems (<i>HotOS</i>), pp. 30-36. ACM, 2019.</p> <p><i>Model checking of Verilog RTL using IC3 with syntax-guided abstraction</i> Aman Goel, and Karem Sakallah. In NASA Formal Methods Symposium (<i>NFM</i>), pp. 166-185. Springer, Cham, 2019.</p> <p><i>Empirical evaluation of IC3-based model checking techniques on Verilog RTL designs</i> Aman Goel, and Karem Sakallah. In 2019 Design, Automation Test in Europe Conference Exhibition (<i>DATE</i>), pp. 618-621. IEEE, 2019.</p> <p><i>iitRACE: A memory efficient engine for fast incremental timing analysis and clock pessimism removal</i> Peddawad, Chaitanya, Aman Goel, B. Dheeraj, and Nitin Chandrachoodan. In 2015 IEEE/ACM International Conference on Computer-Aided Design (<i>ICCAD</i>), pp. 903-909. IEEE, 2015.</p>																		
TEACHING EXPERIENCE	<p>Graduate Student Instructor</p> <p><i>University of Michigan:</i></p> <table><tr><td>EECS 281 Data Structures & Algorithms</td><td>Aug - Dec 2017 & 2018</td></tr><tr><td>EECS 478 Logic Synthesis & Optimization</td><td>Jan - Apr 2018</td></tr><tr><td>EECS 579 Digital System Testing</td><td>Aug - Dec 2019</td></tr></table> <p><i>IIT Madras:</i></p> <table><tr><td>EE 5311 Digital IC Design</td><td>Aug - Nov 2015</td></tr><tr><td>EE 5332 Mapping Signal Processing Algorithms to DSP Architectures</td><td>Jan - May 2016</td></tr></table>			EECS 281 Data Structures & Algorithms	Aug - Dec 2017 & 2018	EECS 478 Logic Synthesis & Optimization	Jan - Apr 2018	EECS 579 Digital System Testing	Aug - Dec 2019	EE 5311 Digital IC Design	Aug - Nov 2015	EE 5332 Mapping Signal Processing Algorithms to DSP Architectures	Jan - May 2016						
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SELECTED COURSES	<p>University of Michigan</p> <table><tr><td>- <i>Advanced Algorithms</i></td><td>- <i>Advanced Compilers</i></td><td>- <i>Formal Verification</i></td></tr><tr><td>- <i>AI Foundations</i></td><td>- <i>Web Systems</i></td><td></td></tr></table> <p>IIT Madras</p> <p>Computer Science:</p> <table><tr><td>- <i>Data Structures & Algorithms</i></td><td>- <i>Design Verification</i></td></tr><tr><td>- <i>Computational Engineering</i></td><td>- <i>Digital Systems Testing</i></td></tr><tr><td>- <i>Computer Organisation</i></td><td>- <i>CAD Systems</i></td></tr></table> <p>Mathematics & Operations Research:</p> <table><tr><td>- <i>Combinatorial Optimization</i></td><td>- <i>Probability Foundations</i></td></tr><tr><td>- <i>Fundamentals of Operational Research</i></td><td>- <i>Decision Modelling</i></td></tr></table>			- <i>Advanced Algorithms</i>	- <i>Advanced Compilers</i>	- <i>Formal Verification</i>	- <i>AI Foundations</i>	- <i>Web Systems</i>		- <i>Data Structures & Algorithms</i>	- <i>Design Verification</i>	- <i>Computational Engineering</i>	- <i>Digital Systems Testing</i>	- <i>Computer Organisation</i>	- <i>CAD Systems</i>	- <i>Combinatorial Optimization</i>	- <i>Probability Foundations</i>	- <i>Fundamentals of Operational Research</i>	- <i>Decision Modelling</i>
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HONORS	<ul style="list-style-type: none"> – Recipient of Dwight F. Benton fellowship at University of Michigan for 2016-17 – Recipient of research travel grant and Israel travel award for 2019 – Branch position 2 in Electrical Engineering at IIT Madras (<i>Silver medalist</i>) – Won international 3rd place in TAU Contest at ICCAD 2015 for Incremental Timing Analysis – Recipient of <i>best undergraduate research project</i> at Pan IIT Research Expo 2014 – Recipient of <i>Electronics for You</i> prize for best academic performance at graduate level – Won <i>National Award</i> for the Empowerment of Persons with Disabilities 2013 for Solar Charger for Hearing Aid Devices
FORMER SHORT PROJECTS	<ul style="list-style-type: none"> – <i>MPUC: Compiler for Memristor Arrays</i> <i>Jan - Apr 2017</i> Developed a compiler for coarse-grained architecture of memristor arrays – <i>Systolic Arrays in Bluespec</i> <i>Aug - Nov 2015</i> Designed and analyzed different architectures of matrix-matrix multiplication using systolic arrays using Xilinx ISE – <i>Radiation Pattern Measurement System for Automotive Radar</i> <i>May - July 2014</i> Wireless Connectivity Solutions, Texas Instruments Developed an automatic radar positioning system for radar modules testing – <i>String Matching Problem & Variants</i> <i>Mar - May 2014</i> Surveyed the historical Knuth-Morris-Pratt (KMP) algorithm and other similar variants to find all occurrences of a given pattern string in a text – <i>Voice to Text Converter</i> <i>Mar 2013</i> Developed software that converts voice input in a language to text field in other chosen language using available softwares of Google Voice Recognition and Google Translate – <i>SPICE Circuit Simulator</i> <i>Aug - Nov 2012</i> Developed a circuit solver in C similar to SPICE for solving linear circuits
OTHER ACTIVITIES	<ul style="list-style-type: none"> – <i>Lunch & Lab program</i> <i>2016 - Present</i> Encourage and guide undergraduate students towards CS major, programming and graduate studies – Voluntary blood donor
HOBBIES	Swimming, Water Polo, Skating (ice & roller), Soccer