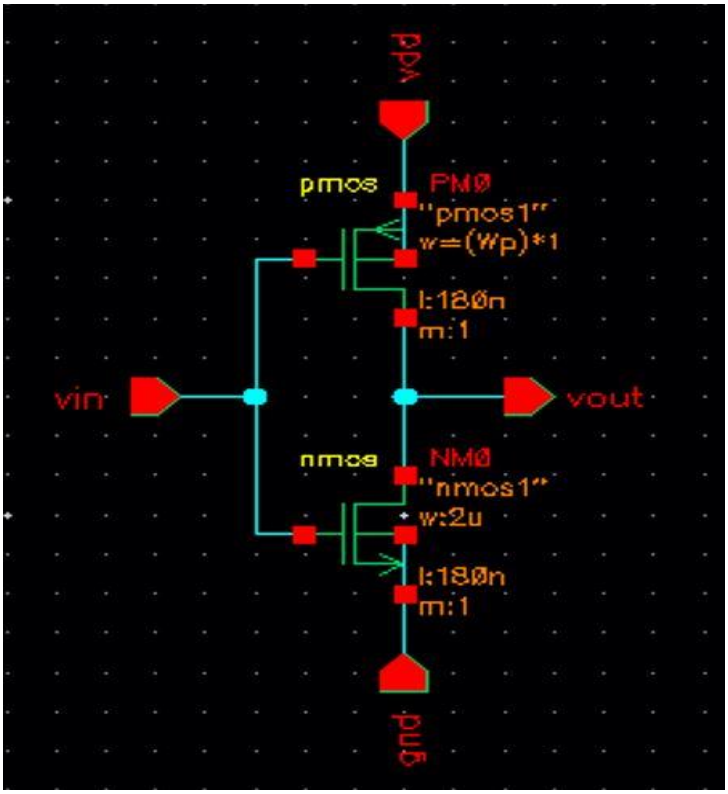
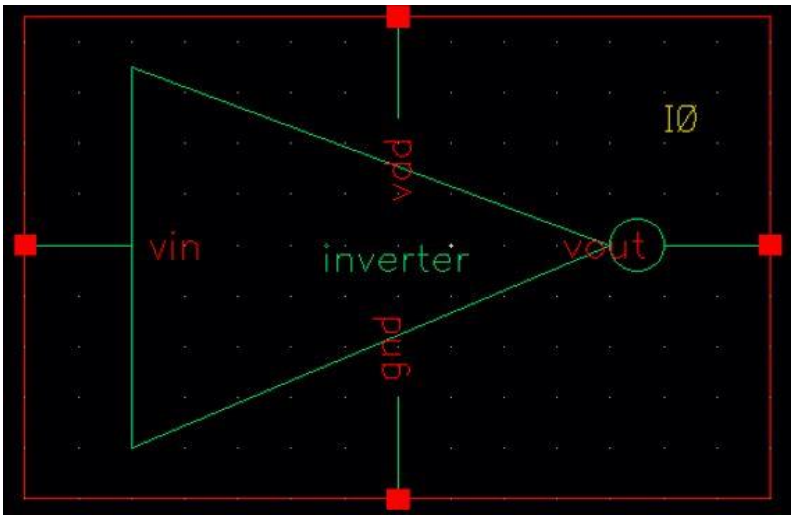
CMOS Inverter – Schematic Design



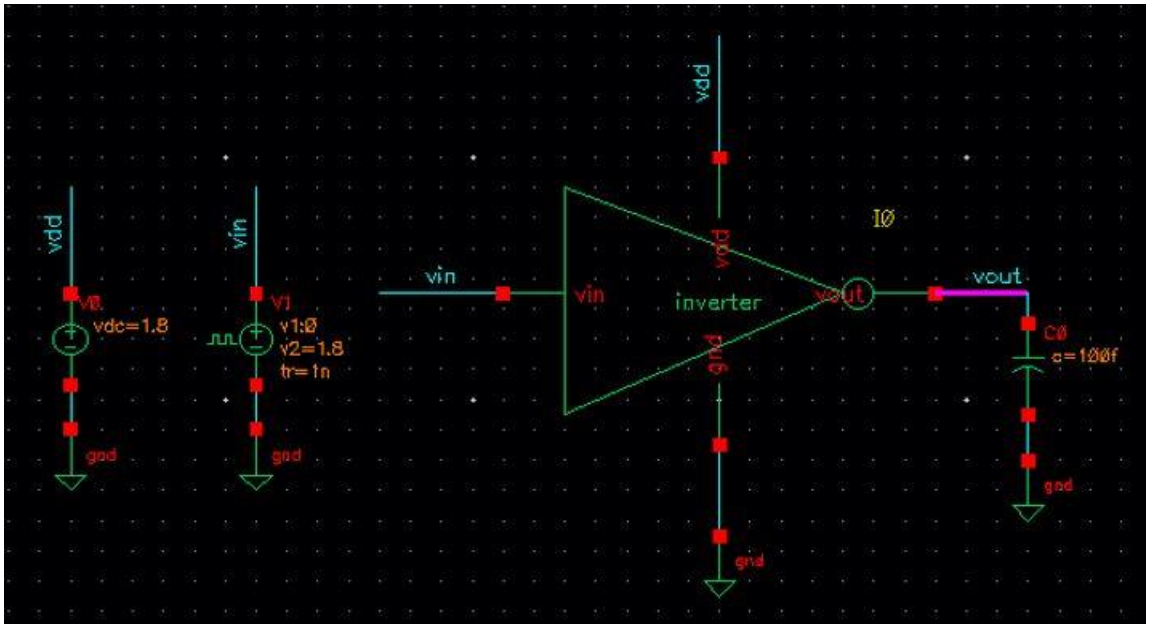
CMOS Inverter schematic

Table of components for building the schematic:

Library Name	Cell Name	Properties
gpdk180	pmos	W = Wp, L = 180n
gpdk180	nmos	W = 2u, L = 180n



CMOS Inverter symbol

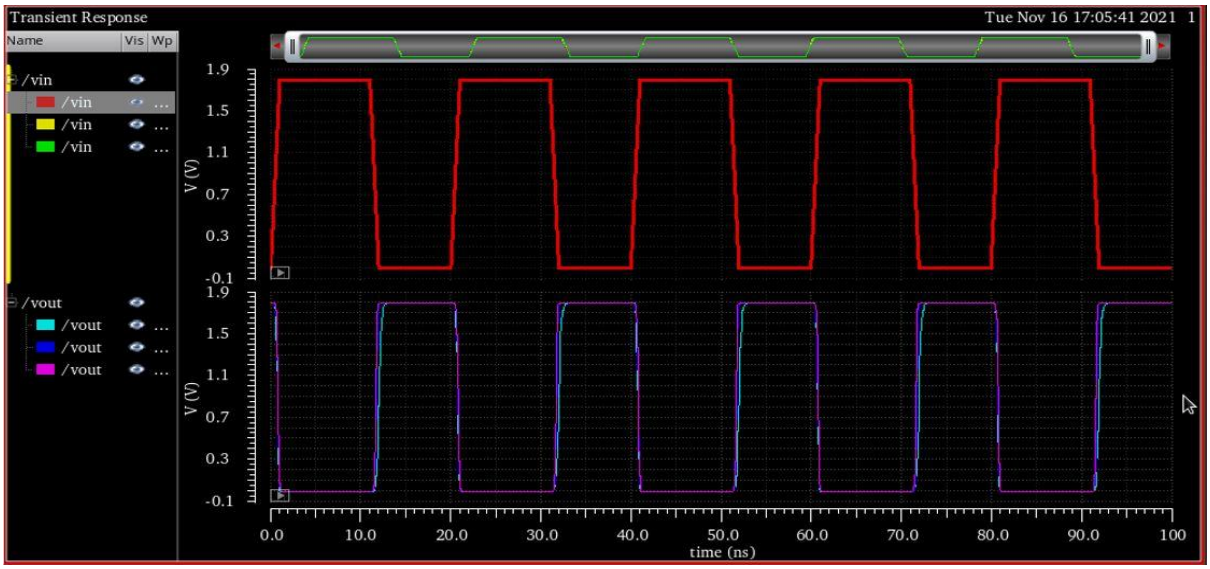


CMOS Inverter test schematic

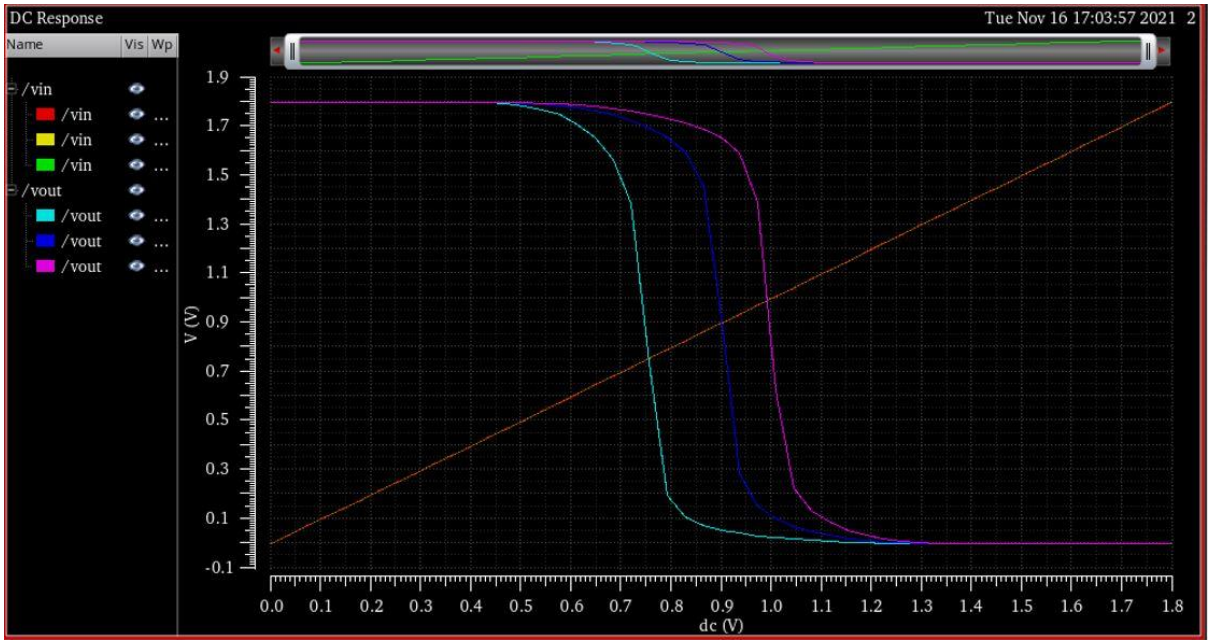
Table of components for building the test schematic:

Library Name	Cell Name	Properties
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 20n, Rise time = 1n, Fall time = 1n, Pulse width = 10n
analogLib	Vdc	Vdc = 1.8
analogLib	gnd	
analogLib	cap	0.1pF

Analog Simulation with spectre for inverter:



Transient Response



DC Response

Table of values to setup for different analysis:

Analysis Name	Settings	Properties
Transient	trans	Stop time = 100n, moderate
DC	DC Analysis	Save DC Operating point
	Sweep Variable Component Parameter	Component Name = Select input signal component (Vpulse) Parameter Name = dc
	Sweep Range Start – Stop	Start = 0, Stop 1.8

Tabulated Values of Delay:

Values of t_{phl}, t_{plh} and t_{pd} for different geometries

Width setting	MOSFET	Width	t_{phl} (ps)	t_{plh} (ps)	t_{pd} (ps)
Wp = Wn	pmos	2u	188.4	445.5	316.95
	nmos	2u			
Wp = 3.75 Wn	pmos	7.5u	225.4	208.4	216.9
	nmos	2u			
Wp = 6.5 Wn	pmos	13u	260.6	115.7	188.15
	nmos	2u			

DC operating point values for different geometries

Width setting	MOSFET	Width	Vin (mV)	Vout (mV)
Wp = Wn	pmos	2u	755.1	755.1
	nmos	2u		
Wp = 3.75 Wn	pmos	7.5u	901.2	901.2
	nmos	2u		
Wp = 6.5 Wn	pmos	13u	990.8	990.8
	nmos	2u		