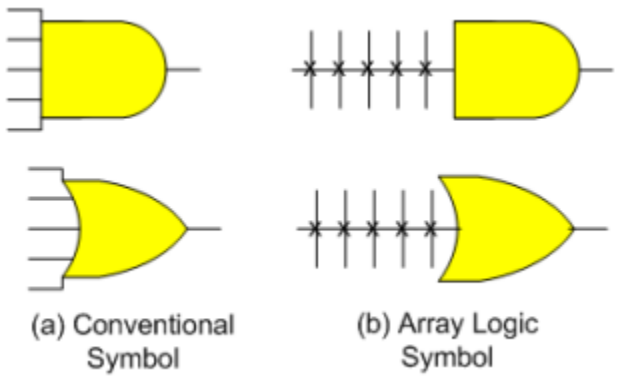
Programmable Logic Devices

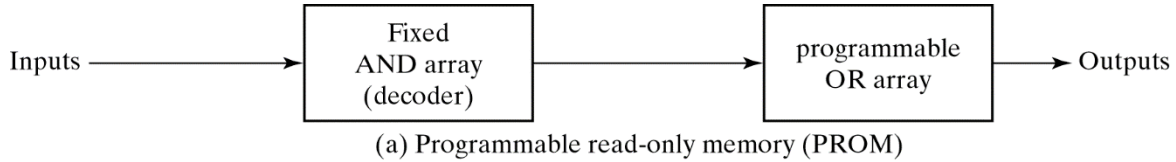
- An IC that contains large numbers of gates, flip-flops, etc. that can be configured by the user to perform different functions is called a Programmable Logic Device (PLD).
- The internal logic gates and/or connections of PLDs can be changed/configured by a programming process.
- One of the simplest programming technologies is to use fuses.
- In the original state of the device, all the fuses are intact.
- Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.

Types of PLDs

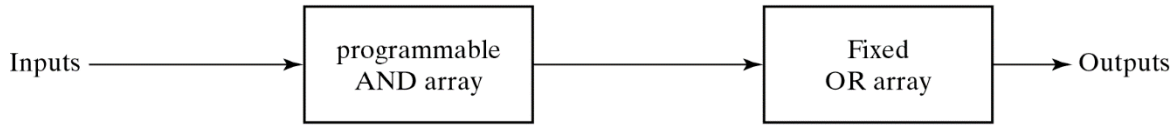
1. SPLDs (Simple Programmable Logic Devices)
   - ❑ROM (Read-Only Memory)
   - ❑PLA (Programmable Logic Array)
   - ❑PAL (Programmable Array Logic)
   - ❑GAL (Generic Array Logic)
2. CPLD (Complex Programmable Logic Device)
3. FPGA (Field-Programmable Gate Array)

Device	AND-array	OR-array
PROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

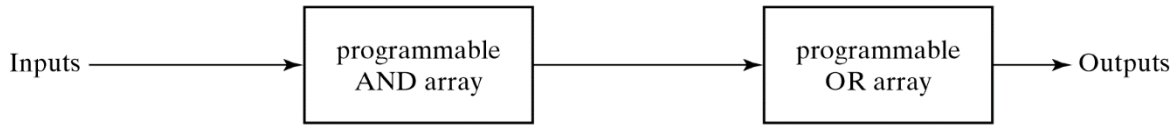




(a) Programmable read-only memory (PROM)



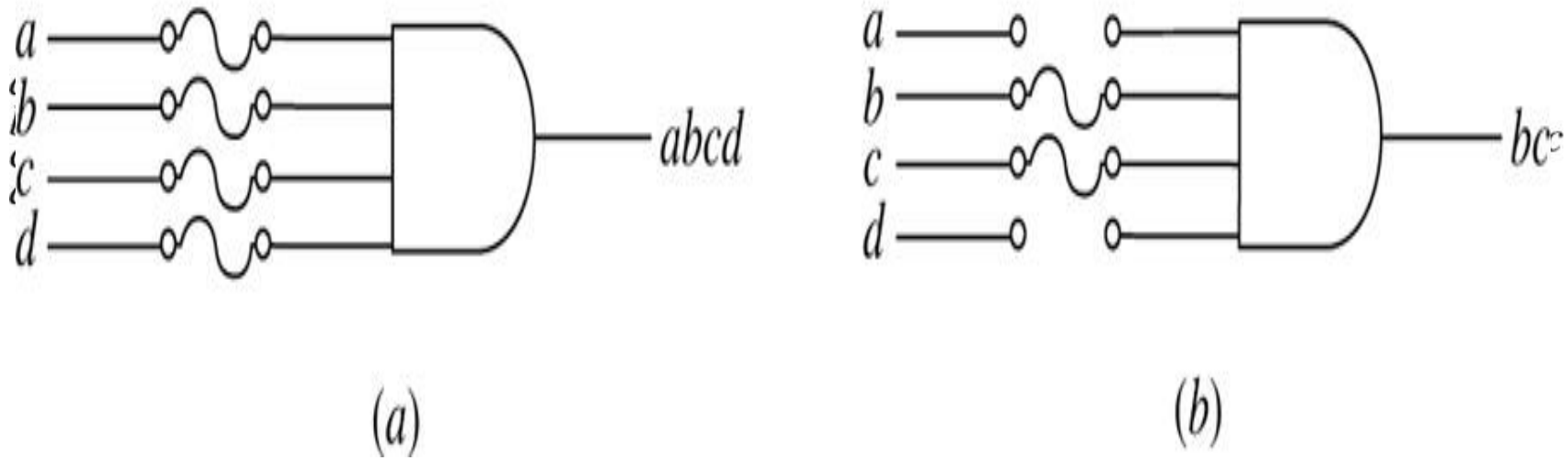
(b) Programmable array logic (PAL)



(c) Programmable logic array (PLA)

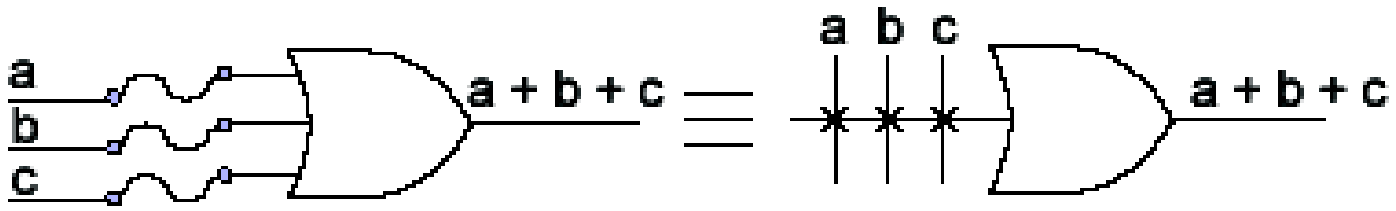
Source: Morris Mano

Programming By Blowing Fuses

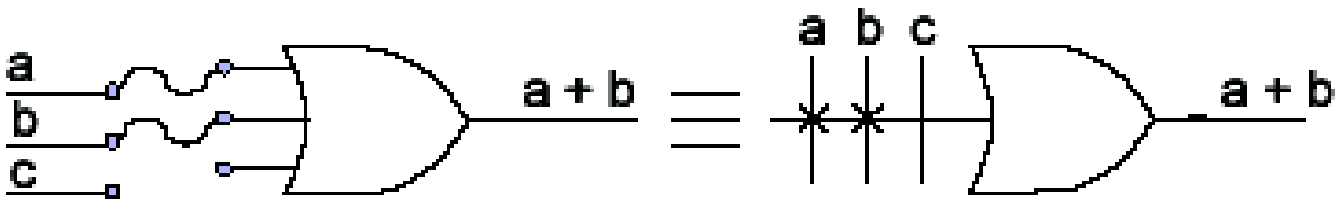


(*a*) Before programming. (*b*) After programming.

OR-PLD Notation

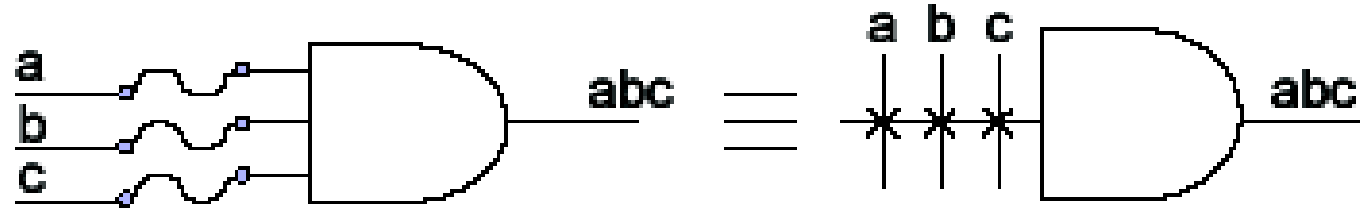


OR gate before programming

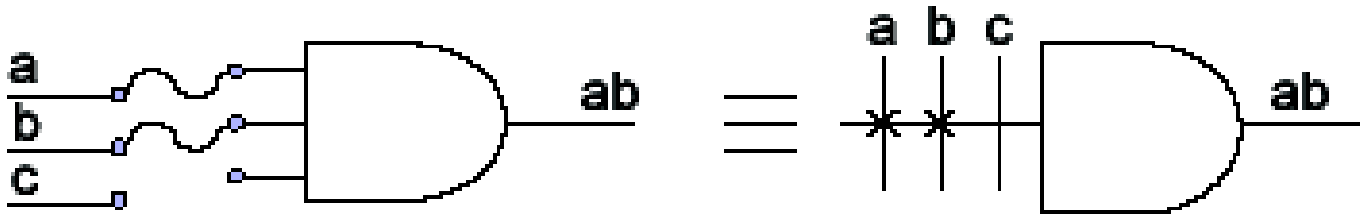


OR gate after programming

AND-PLD Notation



AND gate before programming



AND gate after programming

Read-Only Memory

- A block diagram of a ROM is shown below. It consists of k address inputs and n data outputs.
- The number of words in a ROM is determined from the fact that k address input lines are needed to specify 2^k words.

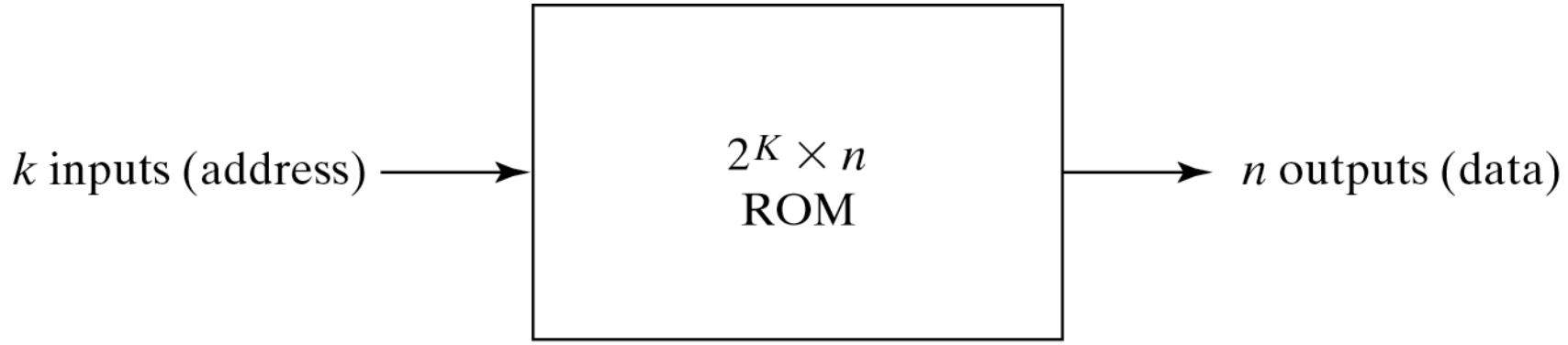


Fig. 7-9 ROM Block Diagram

Source: Morris Mano

Construction of ROM

- Each output of the decoder represents a memory address.
- Each OR gate must be considered as having 32 inputs.
- A 2^k X n ROM will have an internal k X 2^k decoder and n OR gates.

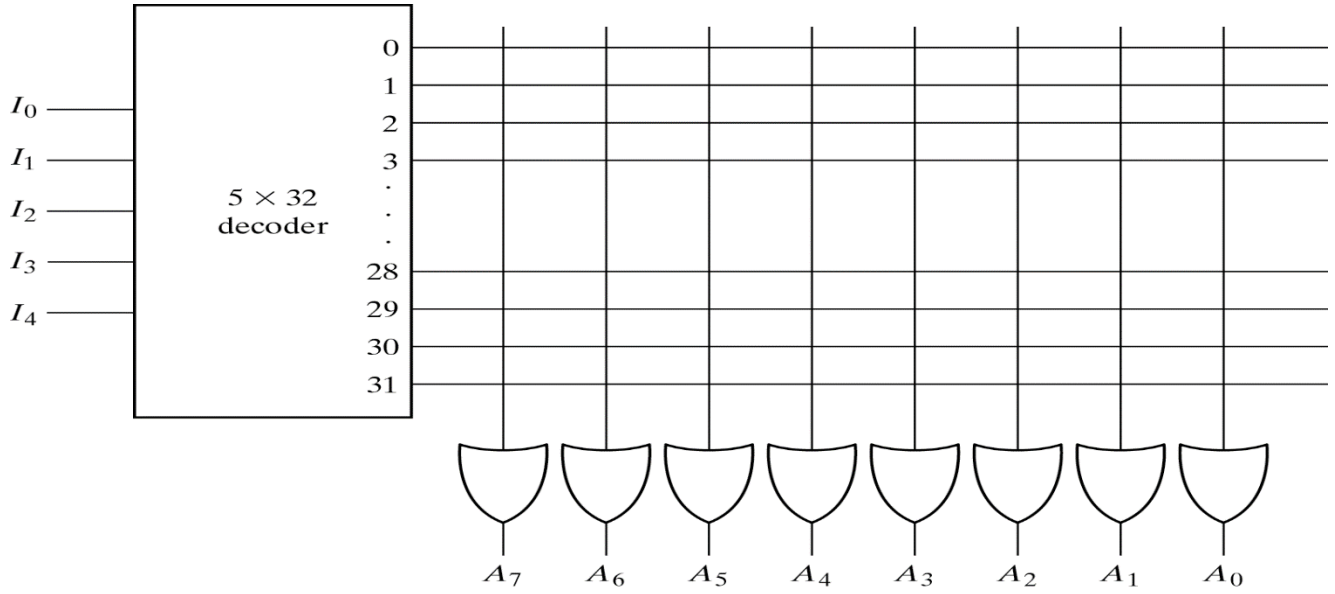


Fig. 7-10 Internal Logic of a 32 × 8 ROM

Source: Morris Mano

Truth table of ROM

- A programmable connection between to lines is logically equivalent to a switch that can be altered to either be close or open.
- Intersection between two lines is sometimes called a cross-point.

Table 7-3
ROM Truth Table (Partial)

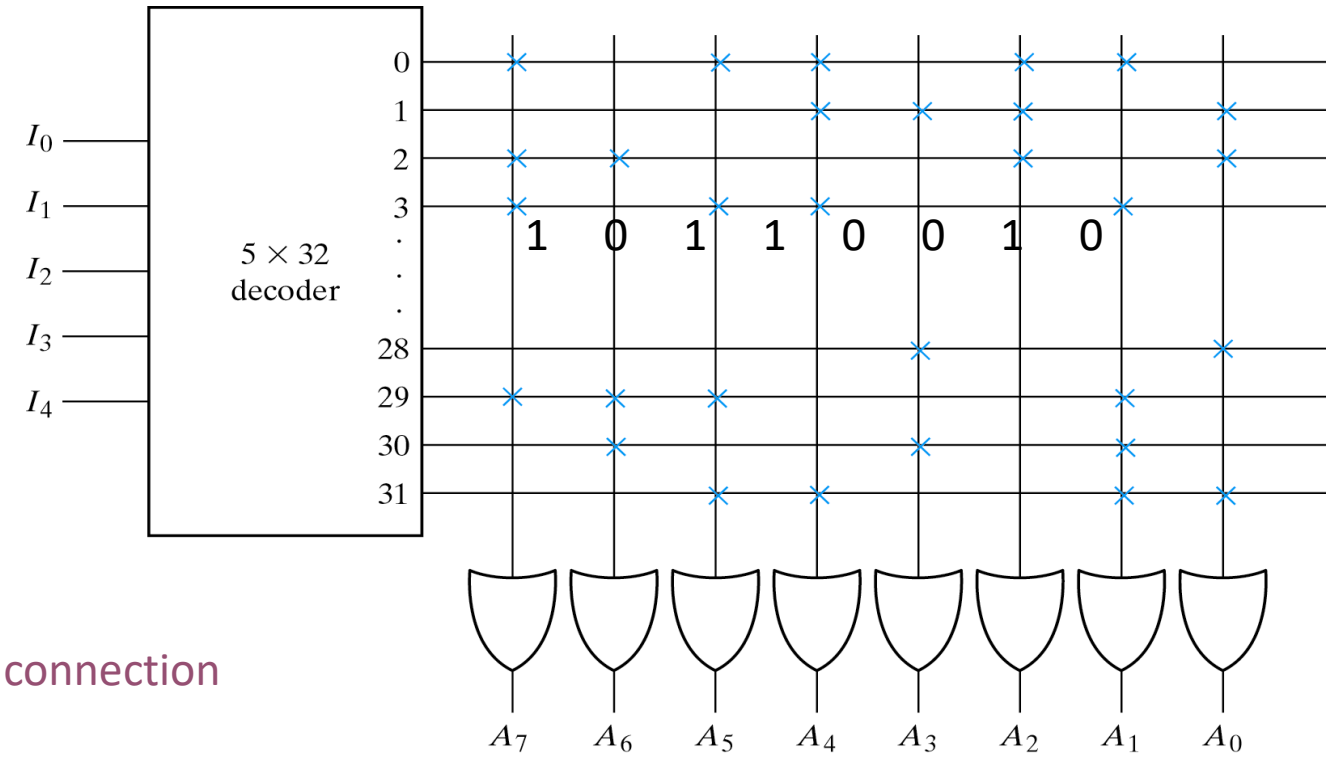
Inputs					Outputs							
I4	I3	I2	I1	I0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮					⋮					
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Programming the ROM

In Table 7-3, 0 → no connection

1 → connection

Address 3 = 10110010 is permanent storage using fuse link



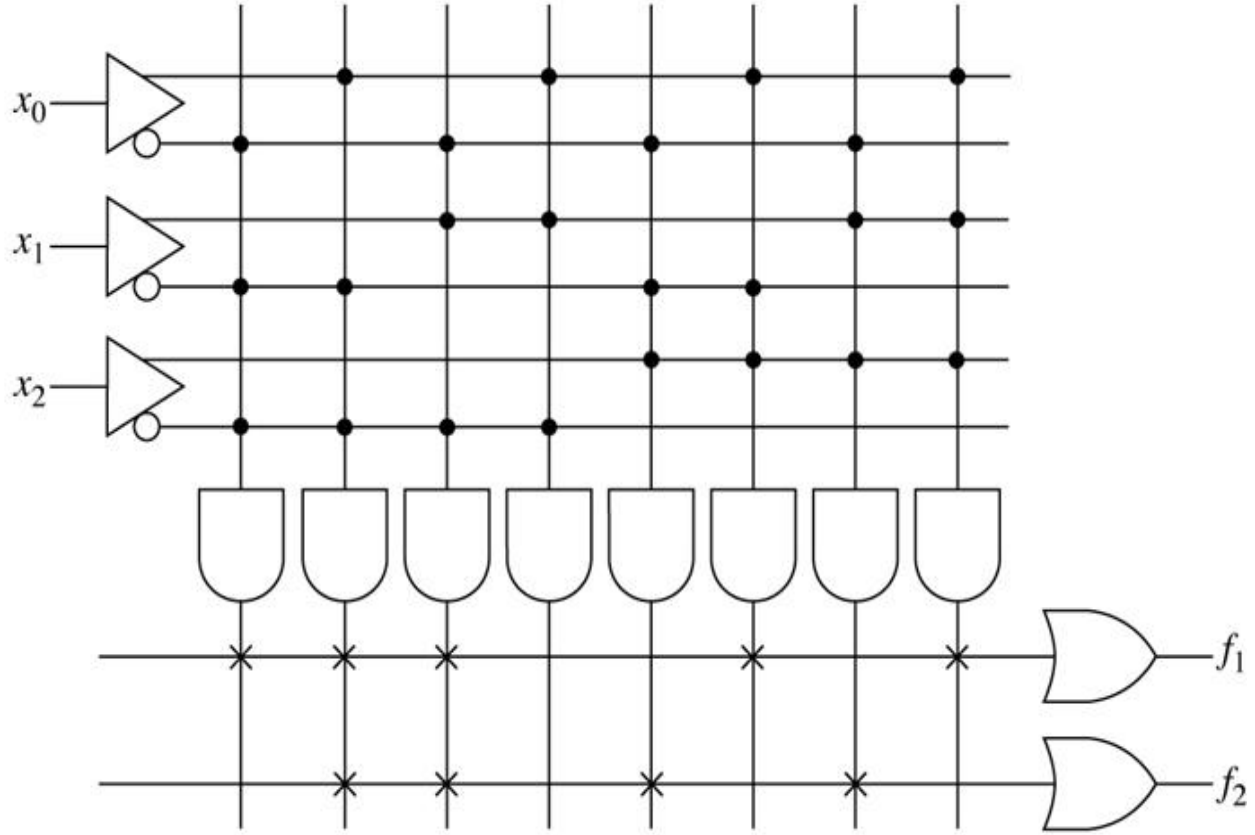
X : means connection

Fig. 7-11 Programming the ROM According to Table 7-3

Using a PROM for logic design

x_2	x_1	x_0	f_1	f_2
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

(*a*)



(*b*)

(*a*) Truth table. **(*b*) PROM realization.**

Quick Quiz

- PAL refers to _____

  a) Programmable Array Loaded
  b) Programmable Logic Array
  c) Programmable Array Logic
  d) Programmable AND Logic

Quick quiz

- The inputs in the PLD is given through _____

  a) NAND gates
  b) OR gates
  c) NOR gates
  d) AND gates