DIGITAL ELECTRONICS

Presented by

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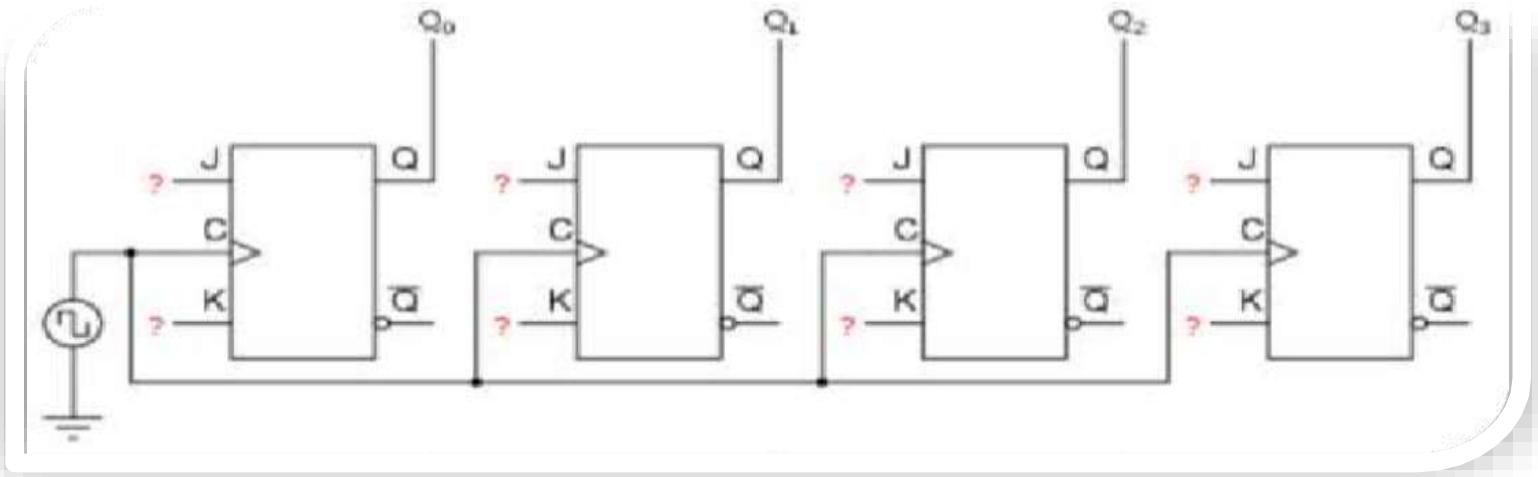
Presentation Topic

- What is synchronous counter
- A three-bit synchronous "UP" counter
- A three-bit synchronous "down" counter
- How to design synchronous counter

Synchronous counter

- A *synchronous counter* , in contrast to an *asynchronous counter* , is one whose output bits change state simultaneously, with no ripple. The only way we can build such a counter circuit from J-K flip-flops is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time:

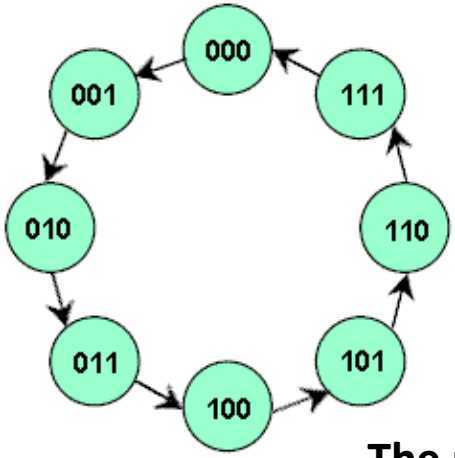


Synchronous counter

- In synchronous binary counter, clock pulses are applied to the CP inputs of all flip-flops and triggered simultaneously.
- If J = K = 0, the flip-flop remains unchanged. If J = K = 1, the flip-flop Complements.

Truth table for JK flip-flop

J	K	Q
0	0	No change
0	1	0
1	0	1
1	1	Toggle



3 – Bit Synchronous Up Counter

State diagram of a 3-bit binary up counter.

The next step is to obtain the state table, which is derived from the state diagram

State table

Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2\ Q_1\ Q_0$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

Truth Table for JK Flip-Flop

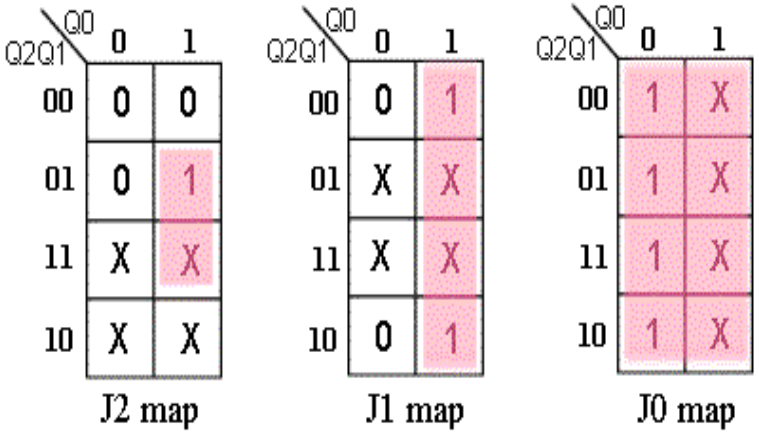
Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table for JK Flip-Flop

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table

Output State Transitions		Flip-flop inputs		
Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2\ Q_1\ Q_0$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

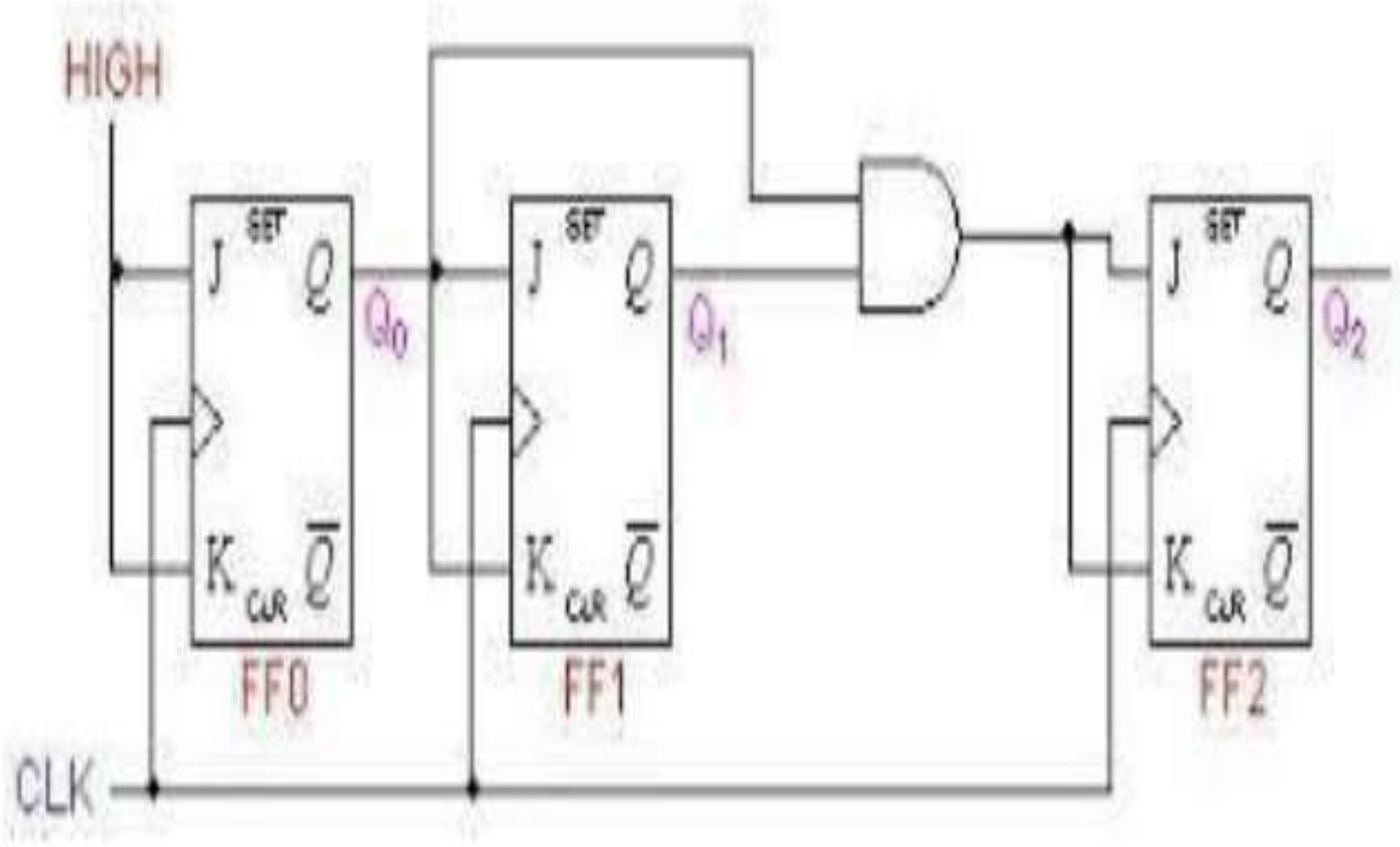


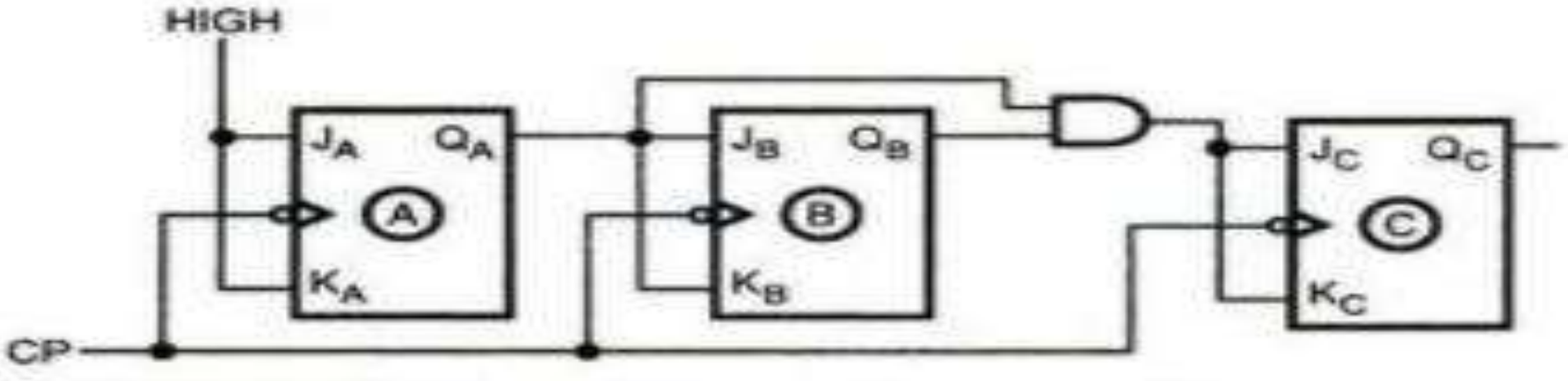
The 1s in the Karnaugh maps are grouped with "don't cares" and the following expressions for the J and K inputs of each flip-flop are obtained:

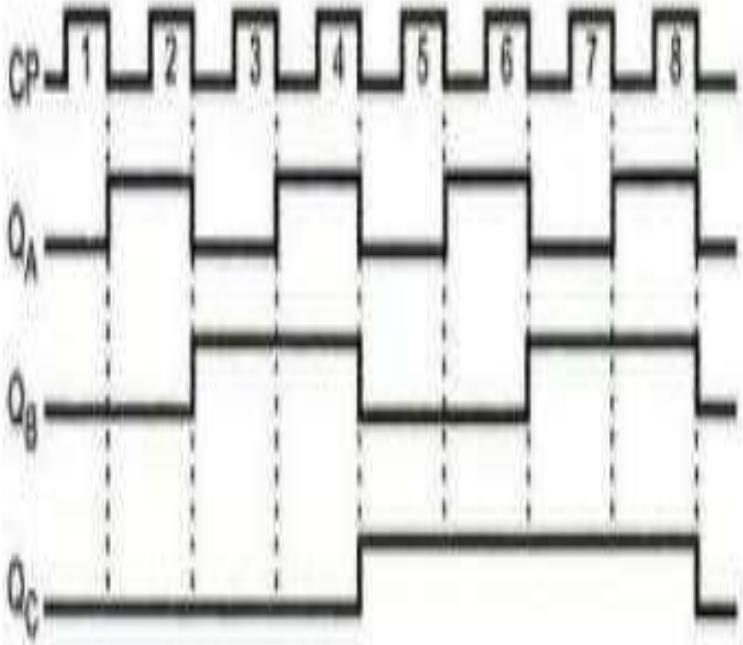
$$J_0 = K_0 = 1$$

$$J_1 = K_1 = Q_0$$

$$J_2 = K_2 = Q_1 * Q_0$$


HIGH
SET
J
Q
K
CLR
$\overline{Q}$
Q_0
Q_1
Q_2
FF0
FF1
FF2
CLK





CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

3-bit Synchronous down counter with JK flip-flops

Present State	Next State
111	110
110	101
101	100
100	011
011	010
010	001
001	000
000	111

Present State	Next State	J_2K_2	J_1K_1	J_0K_0
111	110	d 0	d 0	d 1
110	101	d 0	d 1	1 d
101	100	d 0	0 d	d 1
100	011	d 1	1 d	1 d
011	010	0 d	d 0	d 1
010	001	0 d	d 1	1 d
001	000	0 d	0 d	d 1
000	111	1 d	1 d	1 d

K-map for each JK inputs:

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	0	0
1	d	d	d	d

$J_2=\overline{Q_1}\overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	d	d	d	d
1	1	0	0	0

$K_2=\overline{Q_1}\overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	d	d
1	1	0	d	d

$J_1=\overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	d	0	d
1	1	d	0	d

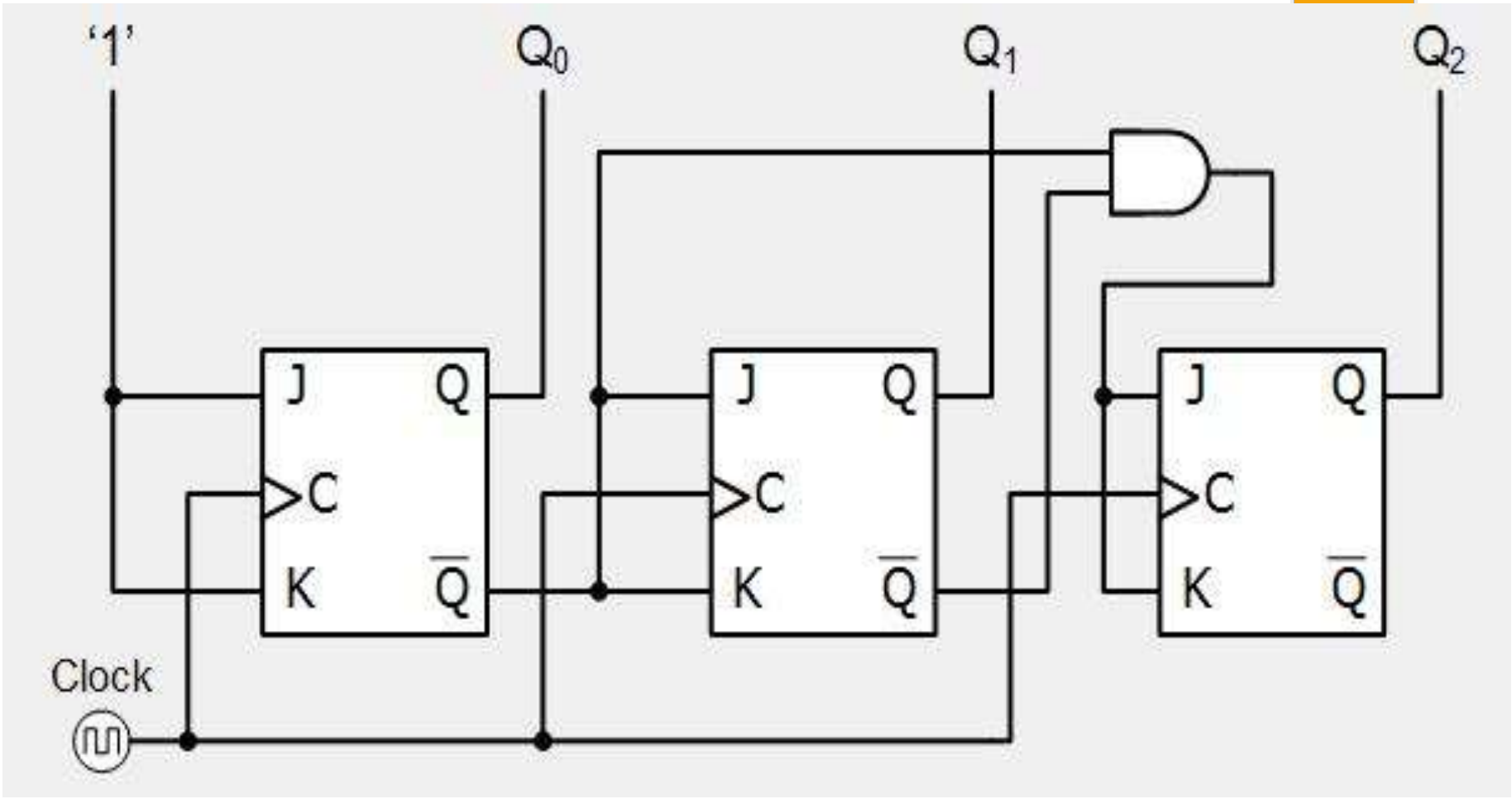
$K_1=\overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	d	d	1
1	1	d	d	1

$J_0=1$

Q_2 \ Q_1Q_0	00	01	11	10
0	d	1	1	d
1	d	1	1	d

$K_0=1$

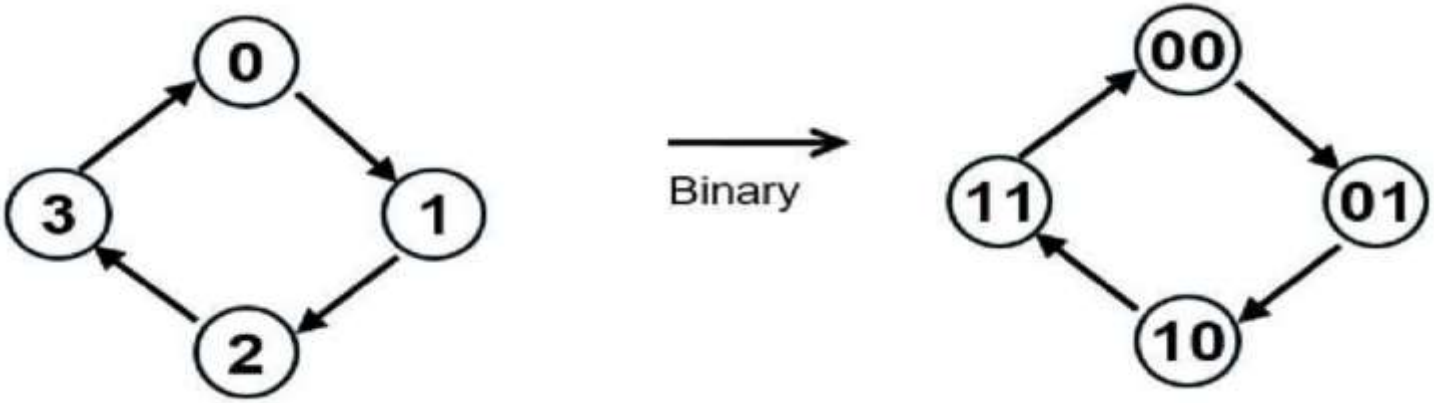

'1'
Q_0
Q_1
Q_2
J
Q
C
K
$\overline{Q}$
J
Q
C
K
$\overline{Q}$
J
Q
C
K
$\overline{Q}$
Clock

How to design synchronous counter

- For synchronous counters, all the flip-flops are using the same CLOCK signal. Thus, the output would change synchronously.
- Procedure to design synchronous counter are as follows:-
- **STEP 1**: Obtain the State Diagram.
- **STEP 2**: Obtain the Excitation Table using state transition table for any particular FF (JK or D). Determine number of FF used.
- **STEP 3:** Obtain and simplify the function of each FF input using K-Map.
- **STEP 4:** Draw the circuit.

How to design synchronous counter

- Design a MOD-4 synchronous up-counter, using JK FF.
- **STEP 1:** Obtain the State transition Diagram



How to design synchronous counter

STEP 2: Obtain the Excitation table. Two JK FF are used.

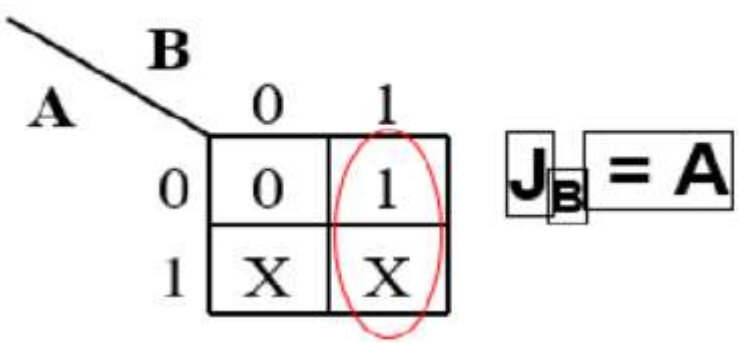
OUTPUT TRANSITION		FF INPUT	
Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table

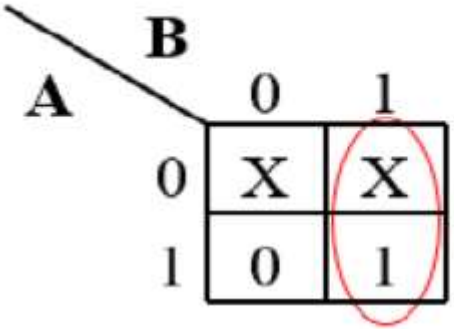
Present State	Next State	Input, J K	
B A	B A	J_B K_B	J_A K_A
0 0	0 1	0 X	1 X
0 1	1 0	1 X	X 1
1 0	1 1	X 0	1 X
1 1	0 0	X 1	X 1

How to design synchronous counter

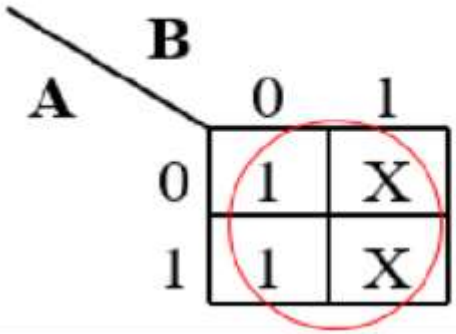
STEP 3: Obtain the simplified function using K-Map



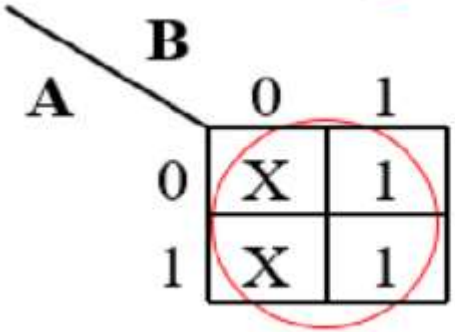
$J_B = A$



$K_B = A$



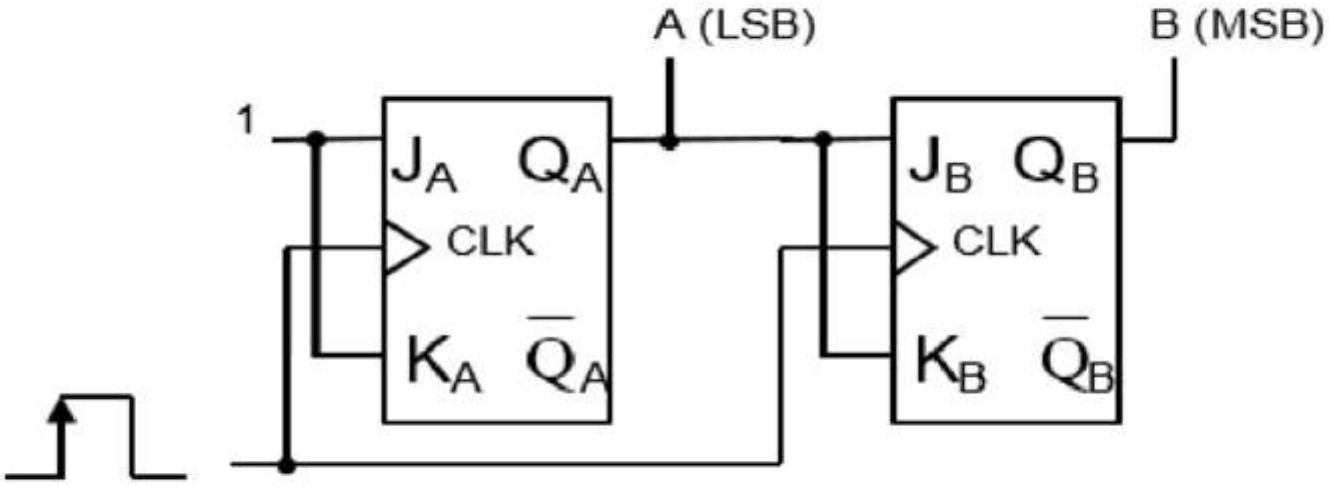
$J_A = 1$



$K_A = 1$

How to design synchronous counter

STEP 4: Draw the circuit diagram.



(MOD-4 synchronous up-counter)

Quick Quiz

Ripple counters are also called _____

a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters