Unit IV

Introduction to Sequential Logic Circuits

by

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Need of D flip flop

One of the main disadvantages of the basic SR *flip flop circuit is that the indeterminate input* condition of "SET" = logic "0" and "RESET" = logic "0" is forbidden.

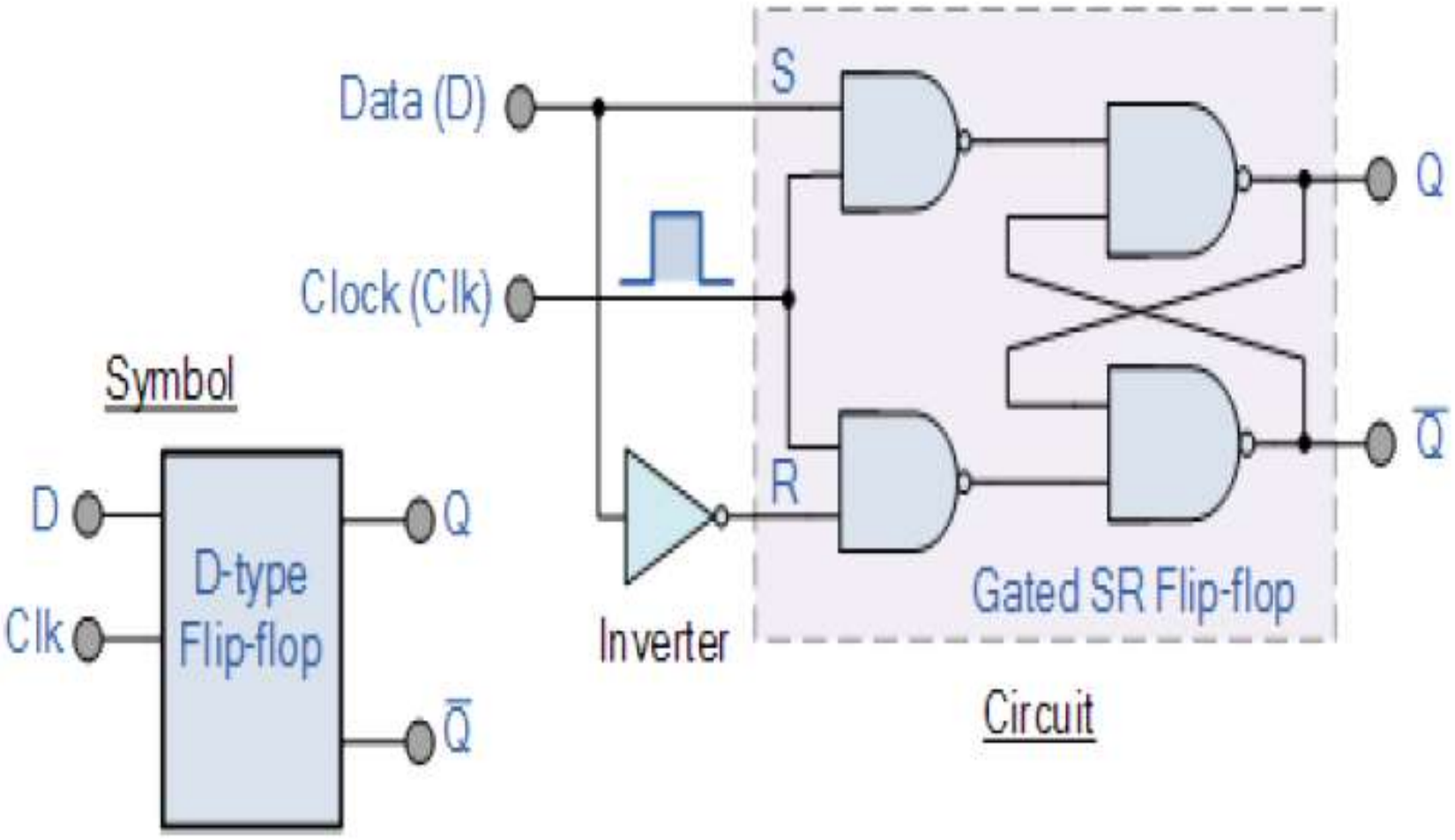
In Simpler words , When R=S=0 or R=S=1 , the outputs Q and Q' either don't change or they are indeterminate(Invalid)

In order to overcome the shortcomings of RS flip flop , the D flip flop was designed , **Data Latch or simply a D-type flip-flop**

The D flip-flop is the most important of the clocked flipflops as it ensures that inputs S and R are never equal to one at the same time.

D-type flip-flops are constructed from a gated SR flipflop with an inverter added between the S and the R inputs to allow for a single D (data) input

D flip-flop Circuit



Working of D flip flop

The **D flip-flop will store and output whatever logic level is applied** to its data terminal so long as the clock input is HIGH.

Once the clock input goes LOW the "set" and "reset" inputs of the flip-flop are both held at logic level "1" so it will not change state and store whatever data was present on its output before the clock transition occurred. In other words the output is "latched" at either logic "0" or logic "1".

D Flip-flop

Symbol

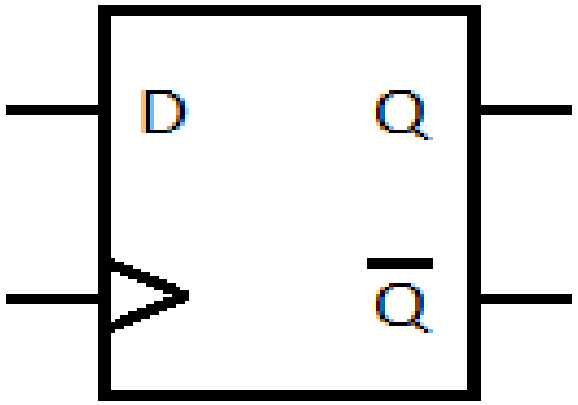


Table of truth:

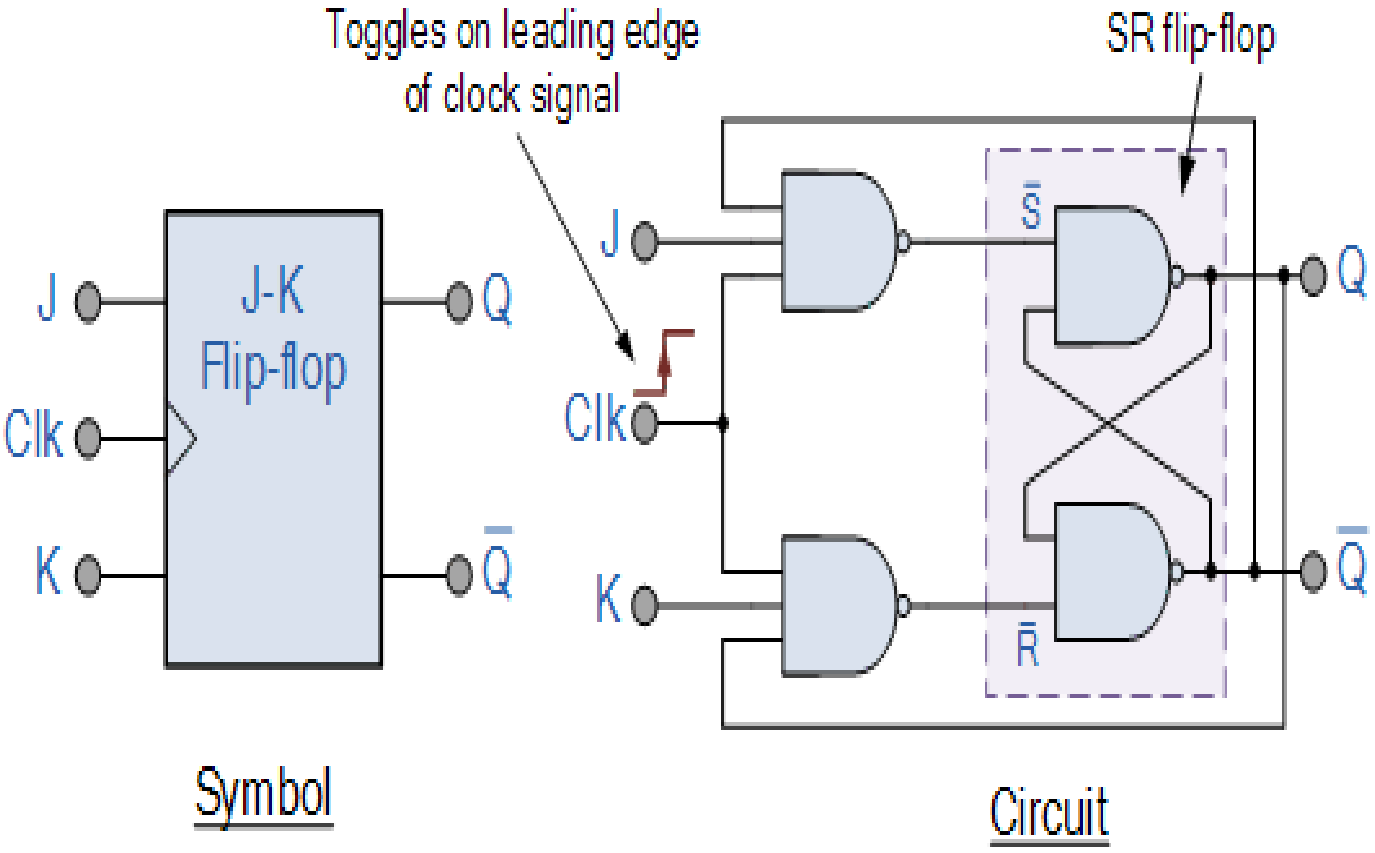
clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

JK Flip Flop

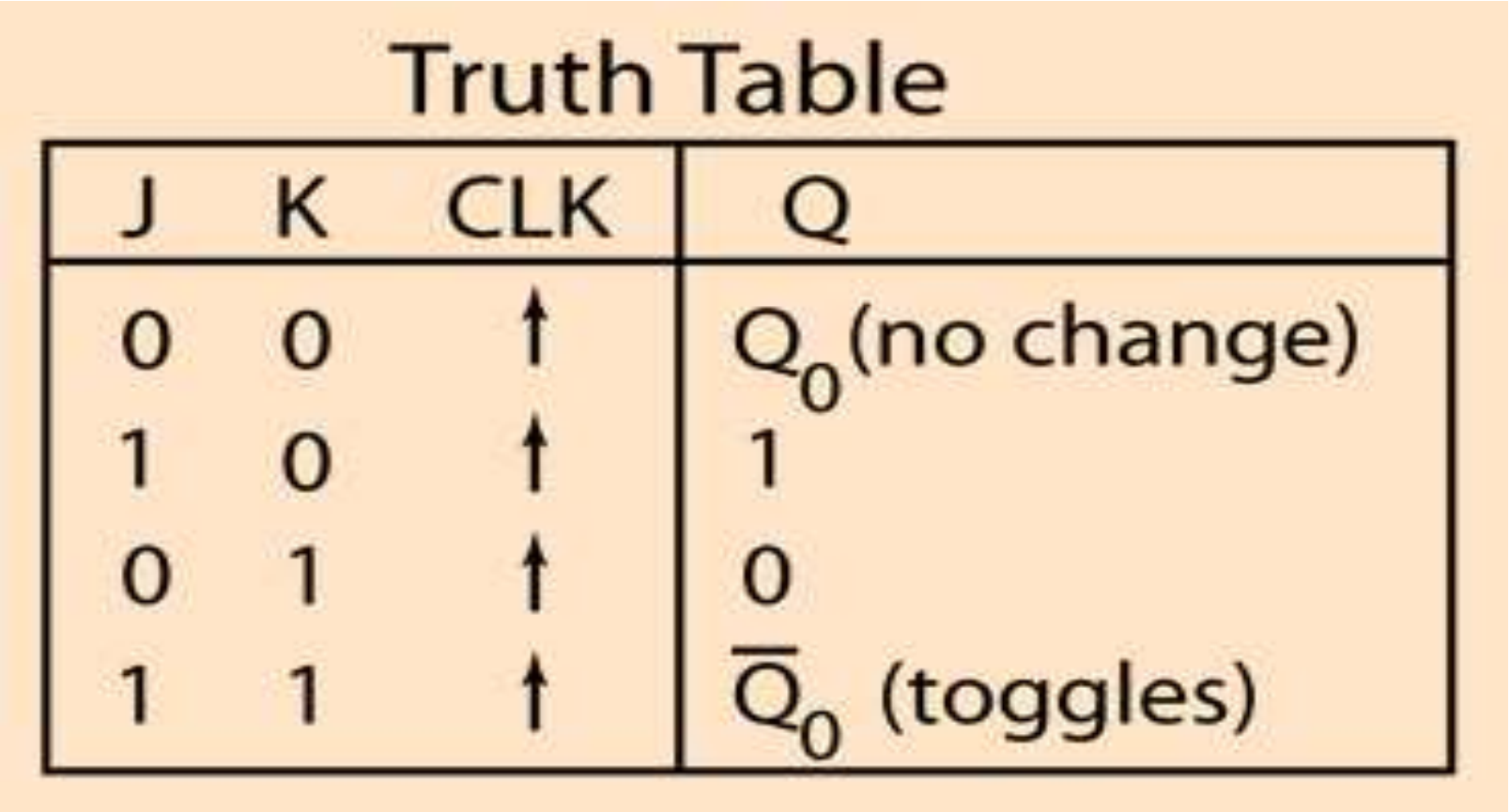
- The simple **JK flip Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The two inputs labelled “J” and “K” are not shortened abbreviated letters of other words, such as “S” for Set and “R” for Reset, but are themselves autonomous letters chosen by its inventor Jack Kilby to distinguish the flip-flop design from other types.

- The sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same “Set” and “Reset” inputs. The difference this time is that the “JK flip flop” has no invalid or forbidden input states of the SR Latch even when S and R are both at logic “1”.
- The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.
- Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”.

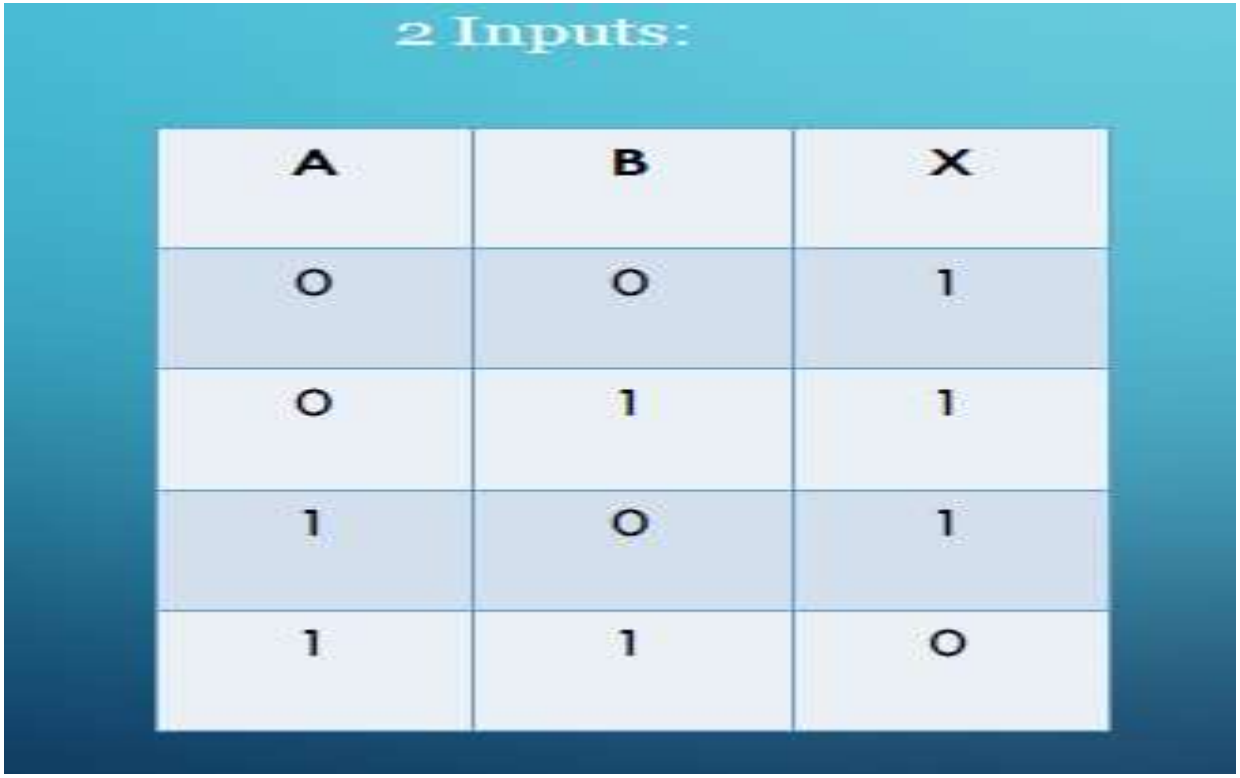
The Basic JK Flip-flop



Truth Table


Truth Table
J K CLK Q
0 0 ↑ Q_0 (no change)
1 0 ↑ 1
0 1 ↑ 0
1 1 ↑ $\overline{Q}_0$ (toggles)

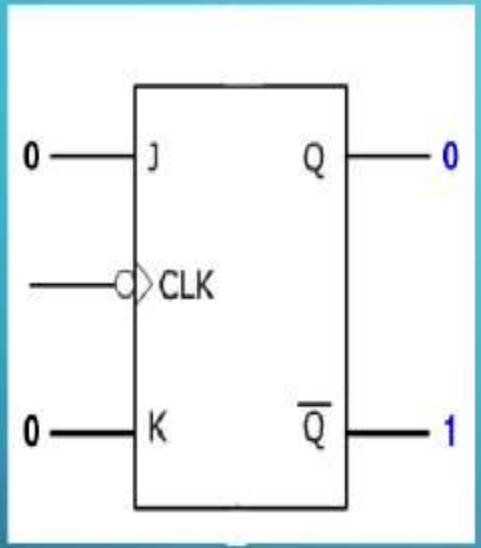
TRUTH TABLE FOR NAND

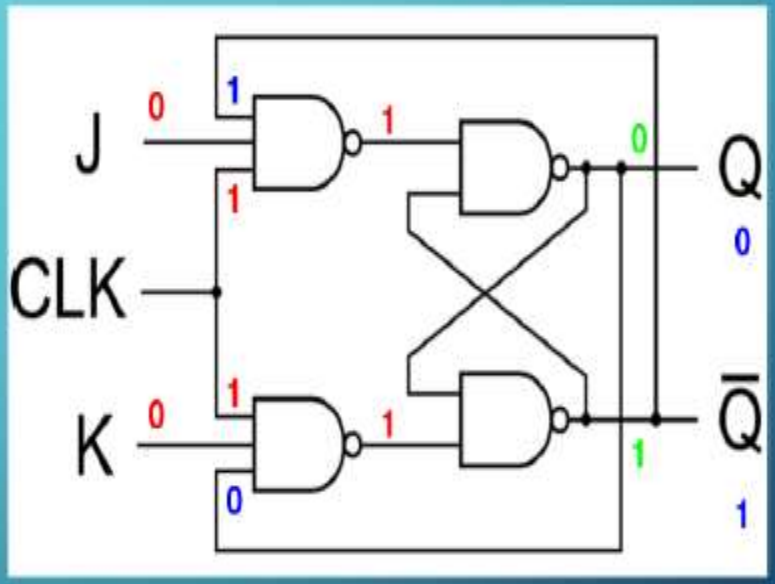


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

MODE OF OPERATION: HOLD

Hold: no change in Q.

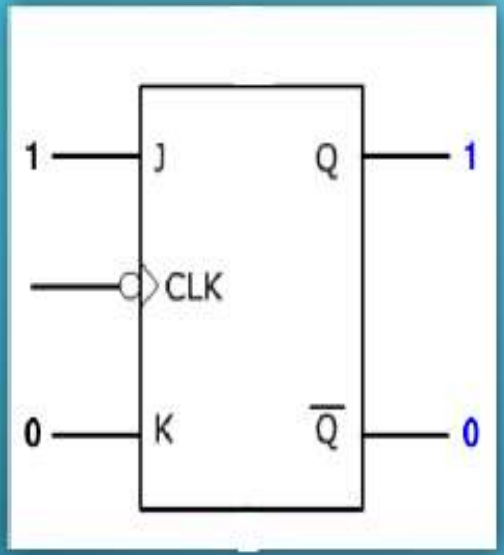


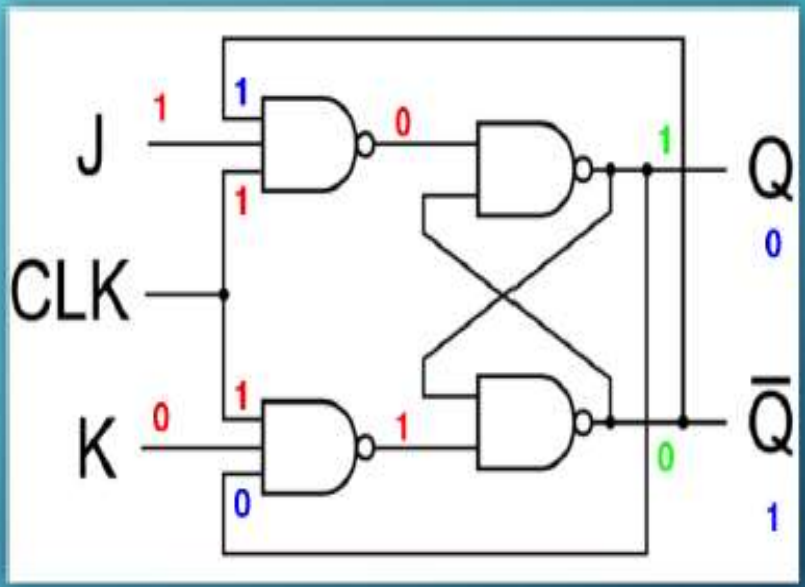


J	K	Q	Q'	Orig. Q	Orig. Q'
0	0	0	1	0	1

MODE OF OPERATION: SET

Set: Q = 1.

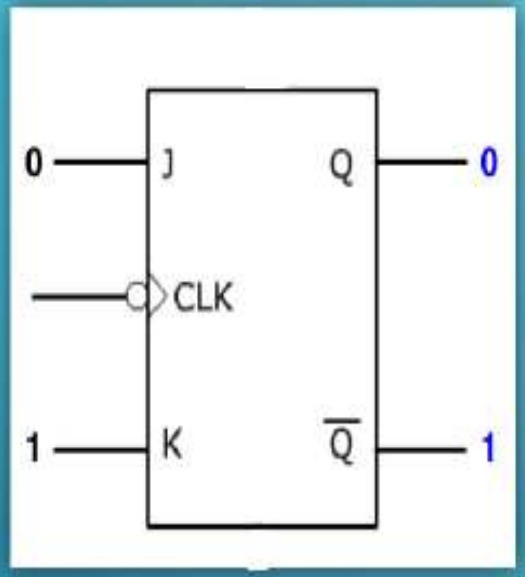


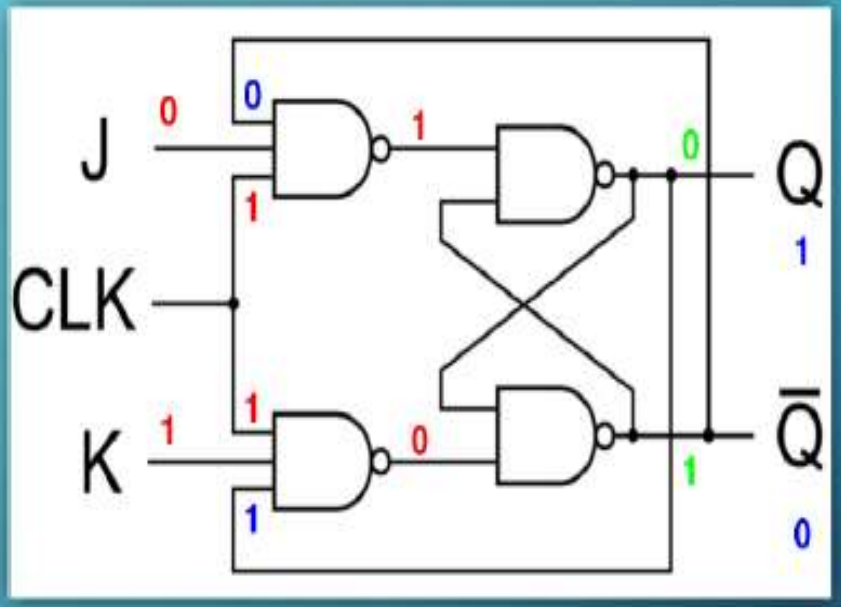


J	K	Q	Q'	Orig. Q	Orig. Q'
1	0	1	0	0	1

MODE OF OPERATION: RESET

Reset: Q = 0.

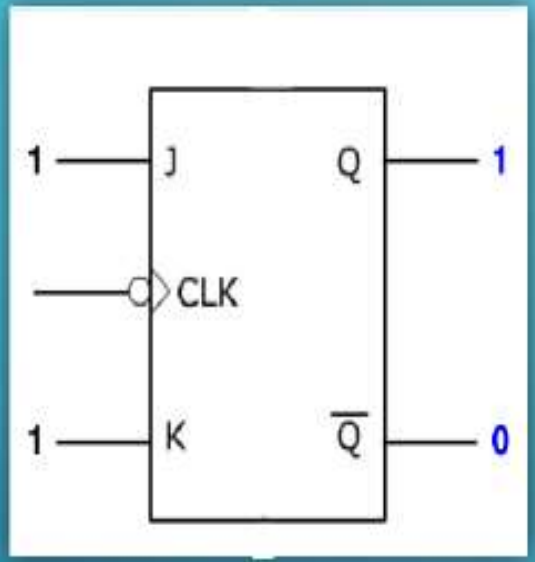


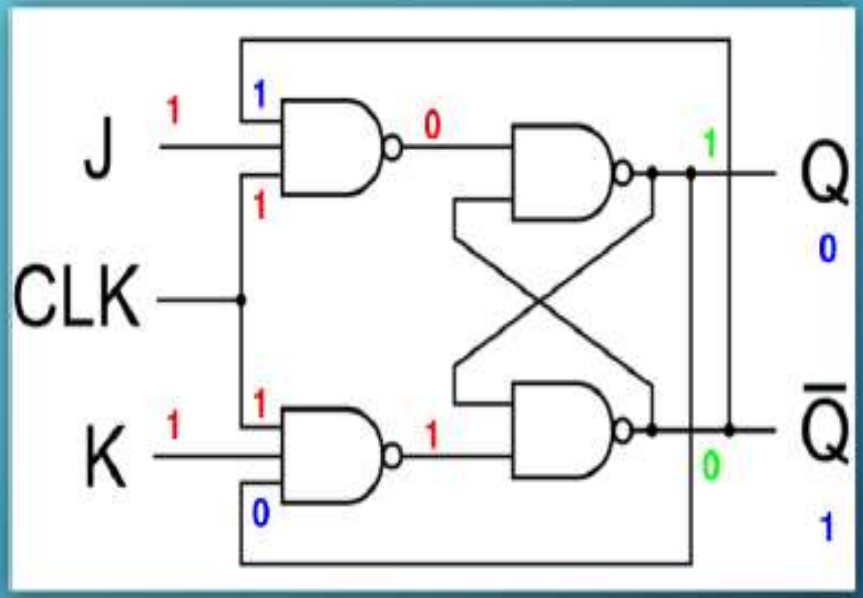


J	K	Q	Q'	Orig. Q	Orig. Q'
0	1	0	1	1	0

MODE OF OPERATION: TOGGLE

Toggle: Q = Q'.

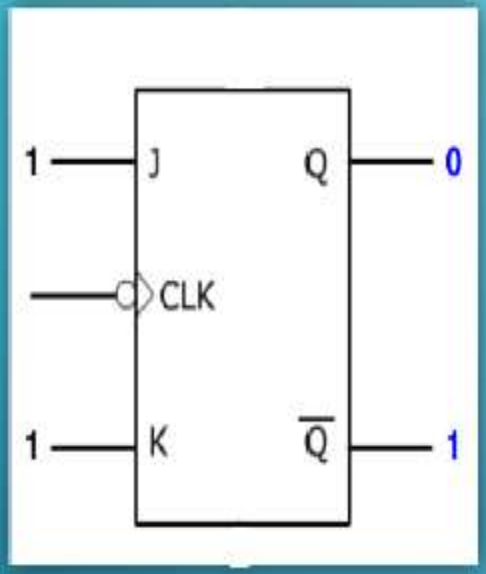


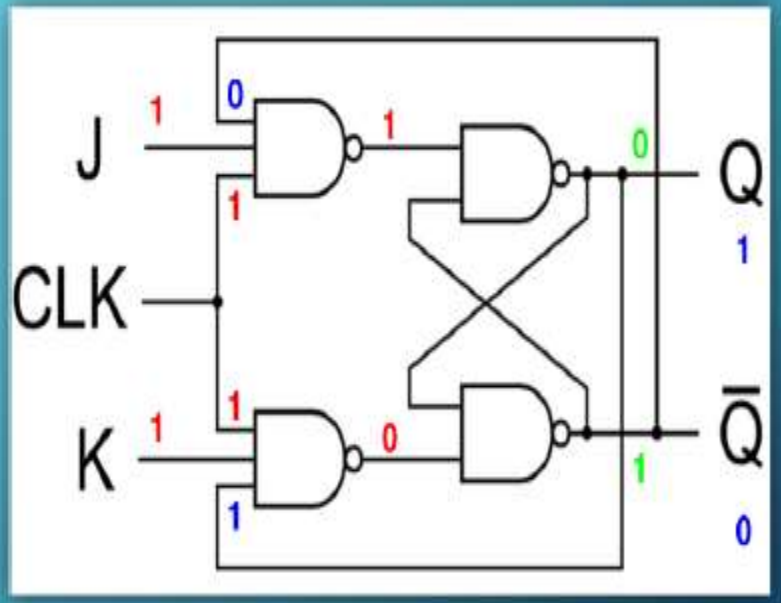


J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	1	0	0	1

MODE OF OPERATION: TOGGLE AGAIN

Toggle: Q = Q'.





J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	0	1	1	0

Quick Quiz (Poll 1)

- A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?

  a) AND or OR gates
  b) XOR or XNOR gates
  c) NOR or NAND gates
  d) AND or NOR gates

Quick Quiz (Poll 2)

- The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called

  _____

  a) Combinational circuits
  b) Sequential circuits
  c) Latches
  d) Flip-flops

Quick Quiz (Poll 3)

- How many types of sequential circuits are?

  a) 2

  b) 3

  c) 4

  d) 5