DECODER

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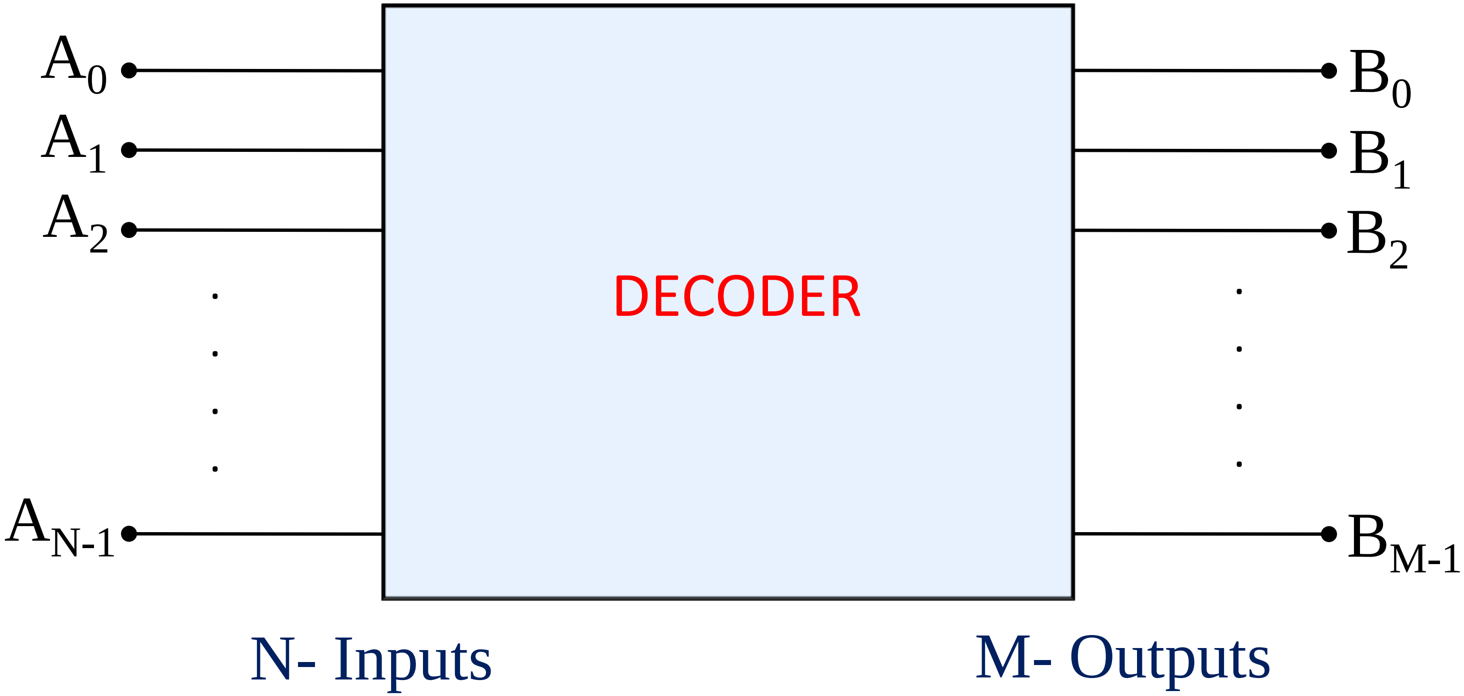
ENCODER

DECODER

- A decoder is a combinational circuit.
- A decoder accepts a set of inputs that represents a binary number and activates only that output corresponding to the input number. All other outputs remain inactive.
- Fig. 1 shows the block diagram of decoder with ‘N’ inputs and ‘M’ outputs.
- There are 2^N possible input combinations, for each of these input combination only one output will be HIGH (active) all other outputs are LOW
- Some decoder have one or more ENABLE (E) inputs that are used to control the operation of decoder.

BLOCK DIAGRAM OF DECODER



Only one output is High for each input

Fig. 1

2 to 4 Line Decoder:

- Block diagram of 2 to 4 decoder is shown in fig. 2
- A and B are the inputs. (No. of inputs =2)
- No. of possible input combinations: $2^2=4$
- No. of Outputs : $2^2=4$, they are indicated by D_0, D_1, D_2 and D_3
- From the Truth Table it is clear that each output is "1" for only specific combination of inputs.

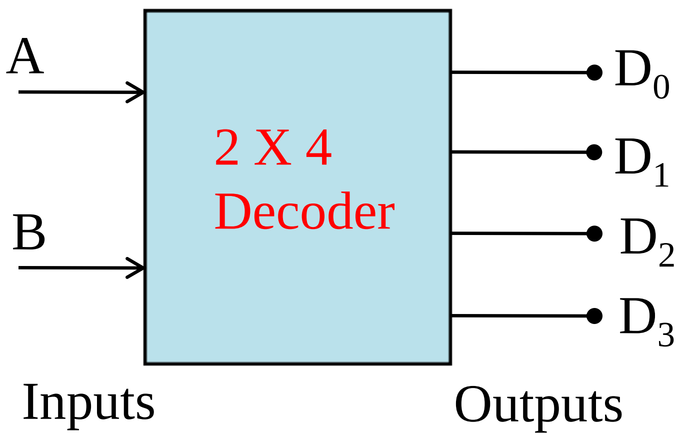


Fig. 2

TRUTH TABLE

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

BOOLEAN EXPRESSION:

From Truth Table

$$D_0 = \overline{A}\,\overline{B} \qquad D_1 = \overline{A}\,B$$

$$D_2 = A\,\overline{B} \qquad D_3 = AB$$

LOGIC DIAGRAM:

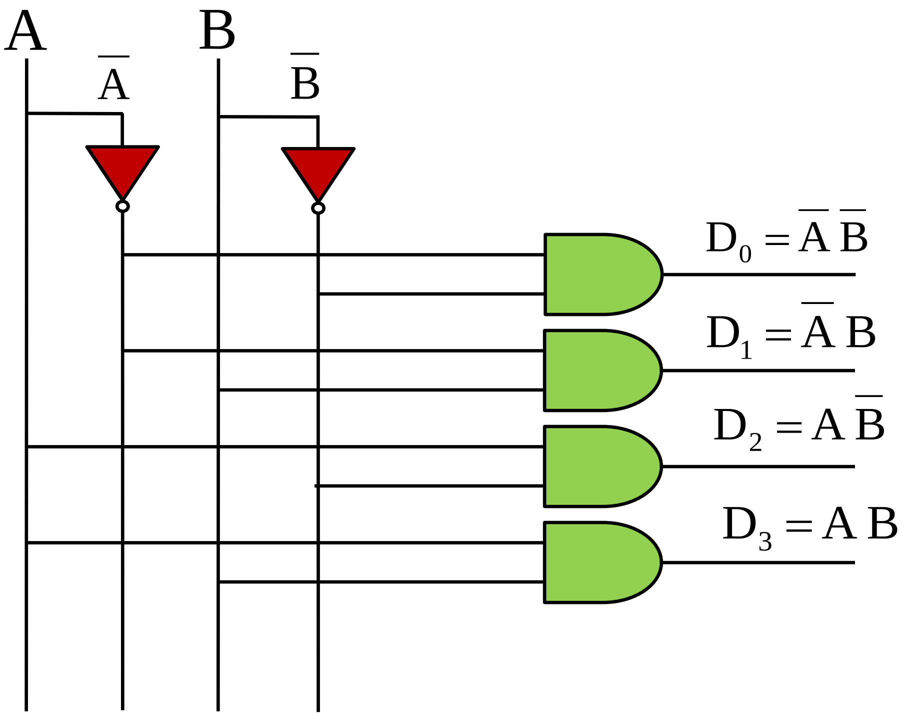


Fig. 3

3 to 8 Line Decoder:

- Block diagram of 3 to 8 decoder is shown in fig. 4
- A , B and C are the inputs. (No. of inputs =3)
- No. of possible input combinations: $2^3=8$
- No. of Outputs : $2^3=8$, they are indicated by D_0 to D_7
- From the Truth Table it is clear that each output is "1" for only specific combination of inputs.

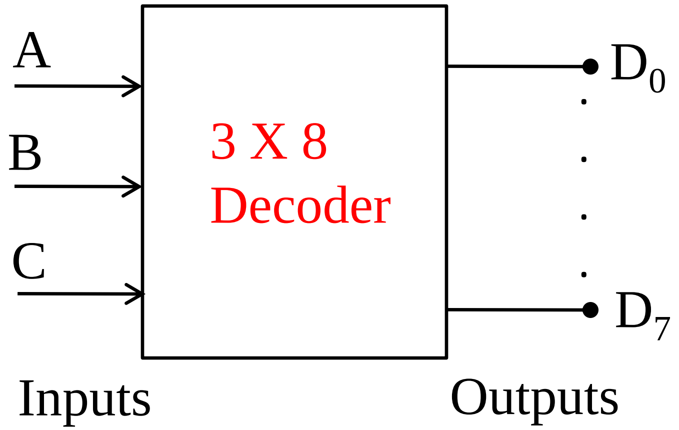


Fig. 4

TRUTH TABLE FOR 3 X 8 DECODER:

INPUTS			OUTPUTS								
A	B	C	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	1	0	0	0	0	0	0	0	$D_0 = \overline{A}\,\overline{B}\,\overline{C}$
0	0	1	0	1	0	0	0	0	0	0	$D_1 = \overline{A}\,\overline{B}\,C$
0	1	0	0	0	1	0	0	0	0	0	$D_2 = \overline{A}\,B\,\overline{C}$
0	1	1	0	0	0	1	0	0	0	0	$D_3 = \overline{A}\,B\,C$
1	0	0	0	0	0	0	1	0	0	0	$D_4 = A\,\overline{B}\,\overline{C}$
1	0	1	0	0	0	0	0	1	0	0	$D_5 = A\,\overline{B}\,C$
1	1	0	0	0	0	0	0	0	1	0	$D_6 = A\,B\,\overline{C}$
1	1	1	0	0	0	0	0	0	0	1	$D_7 = A\,B\,C$

LOGIC DIAGRAM OF 3 X 8 DECODER:

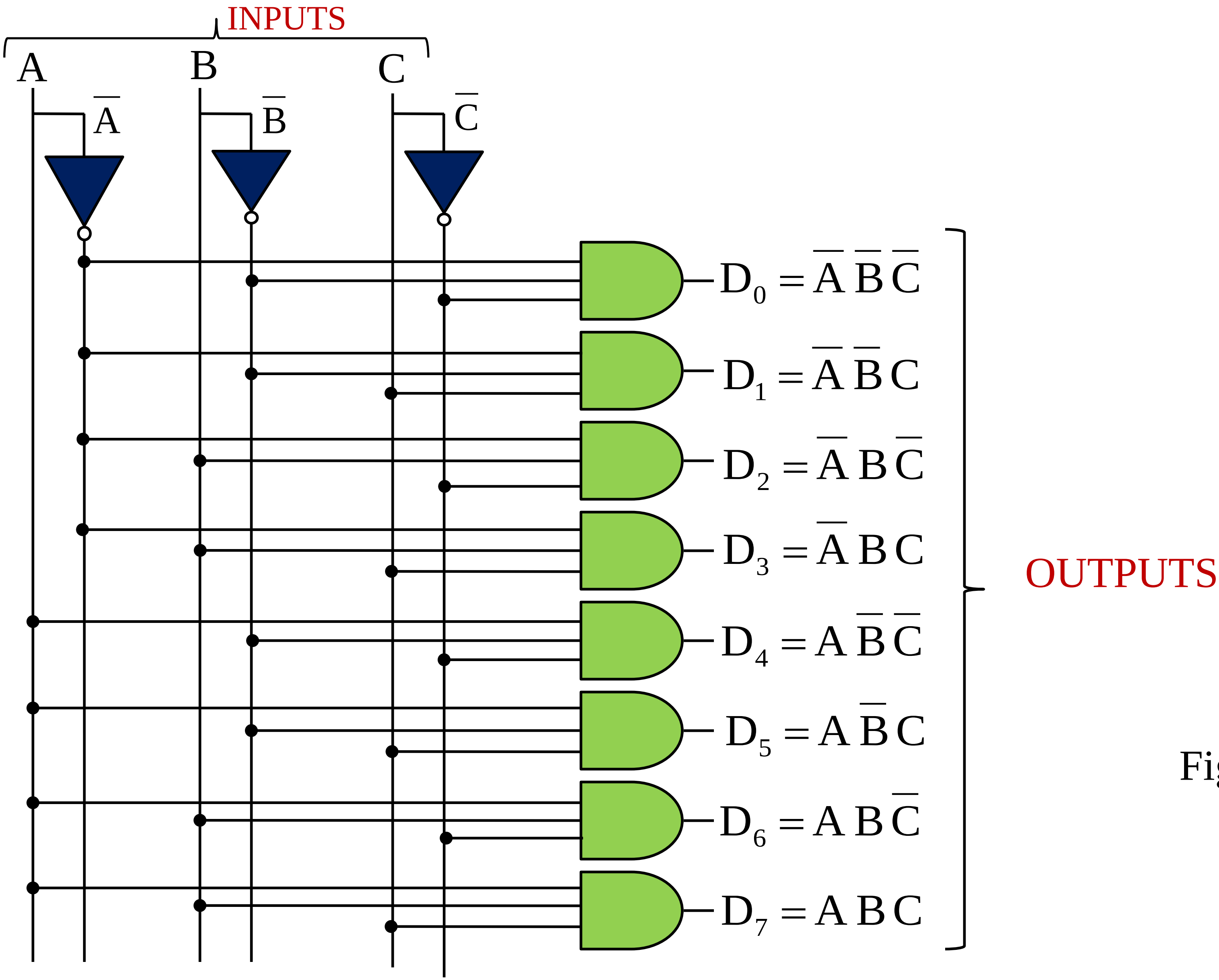


Fig. 5

EXPANSION OF DECODERS:

The number of lower order Decoder for implementing higher order Decoder can be find as

No. of lower order required = m_2/m_1

Where, m_1=No. of Outputs of lower order Decoder

m_2=No. of Outputs of higher order Decoder

3 x 8 Decoder From 2 x 4 Decoder:

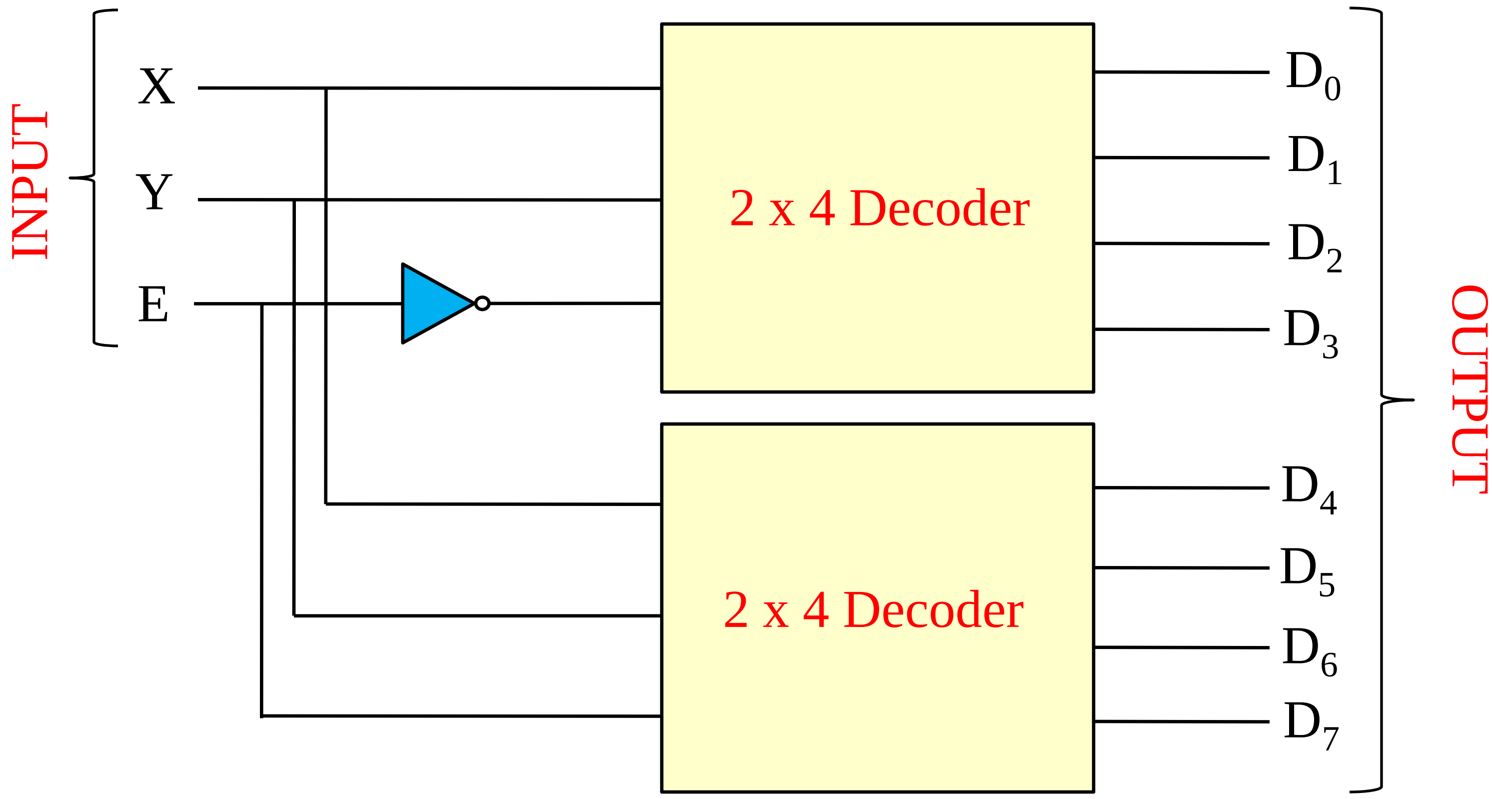


Fig. 6

Example: Implement the following multiple output function using a suitable Decoder.

$f_1(A, B, C) = \sum m(0,4,7) + d(2,3)$

$f_2(A, B, C) = \sum m(1,5,6)$

$f_3(A, B, C) = \sum m(0,2,4,6)$

Solution: f1 consists of don't care conditions. So we consider them to be logic 1.

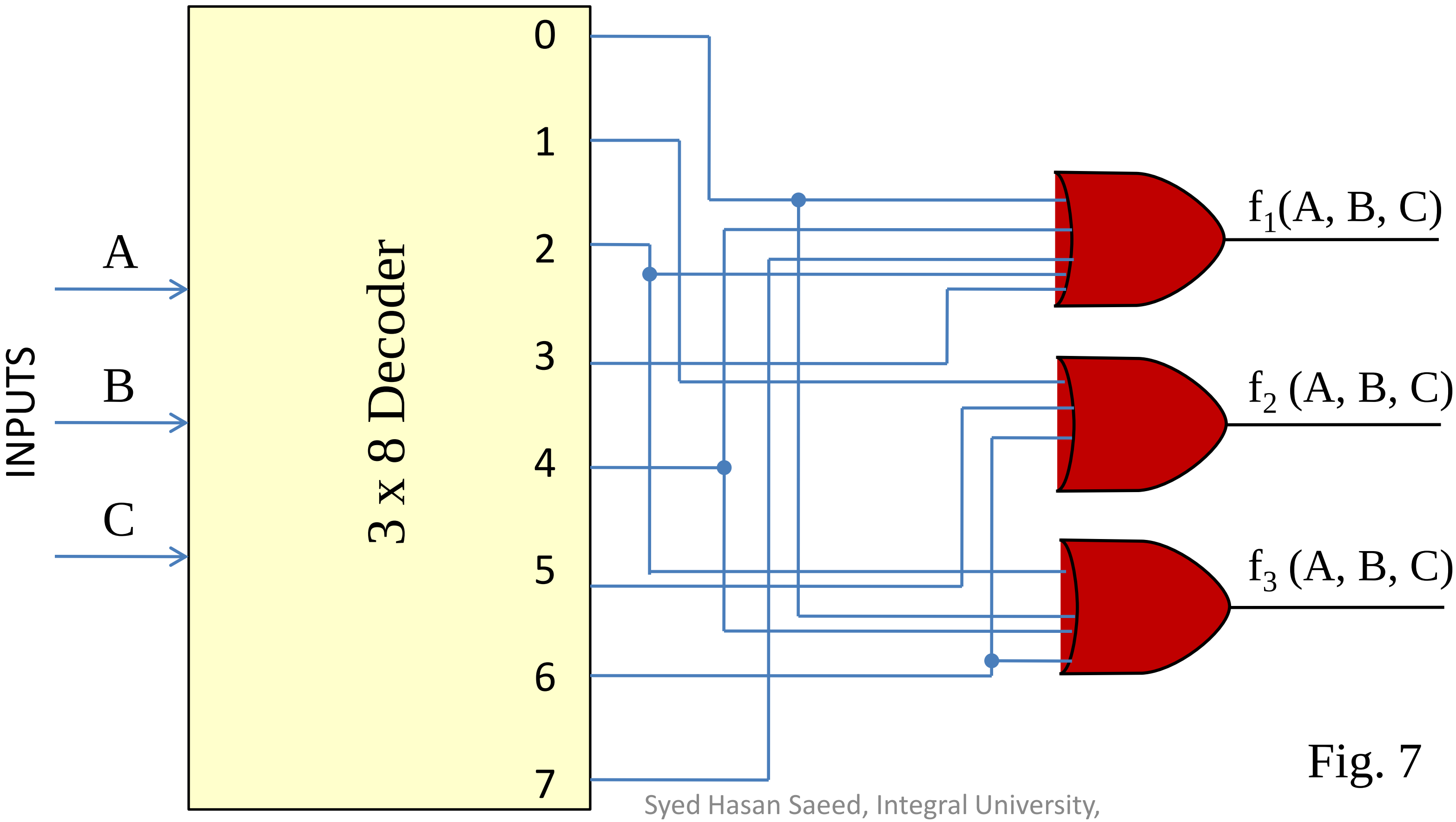


Fig. 7

EXAMPLE: Implement the following Boolean function using suitable Decoder.

$f_1\ (x,y,z)=\sum m(1,5,7)$

$f_2\ (x,y,z)=\sum m(0,3)$

$f_3\ (x,y,z)=\sum m(2,4,5)$

Solution:

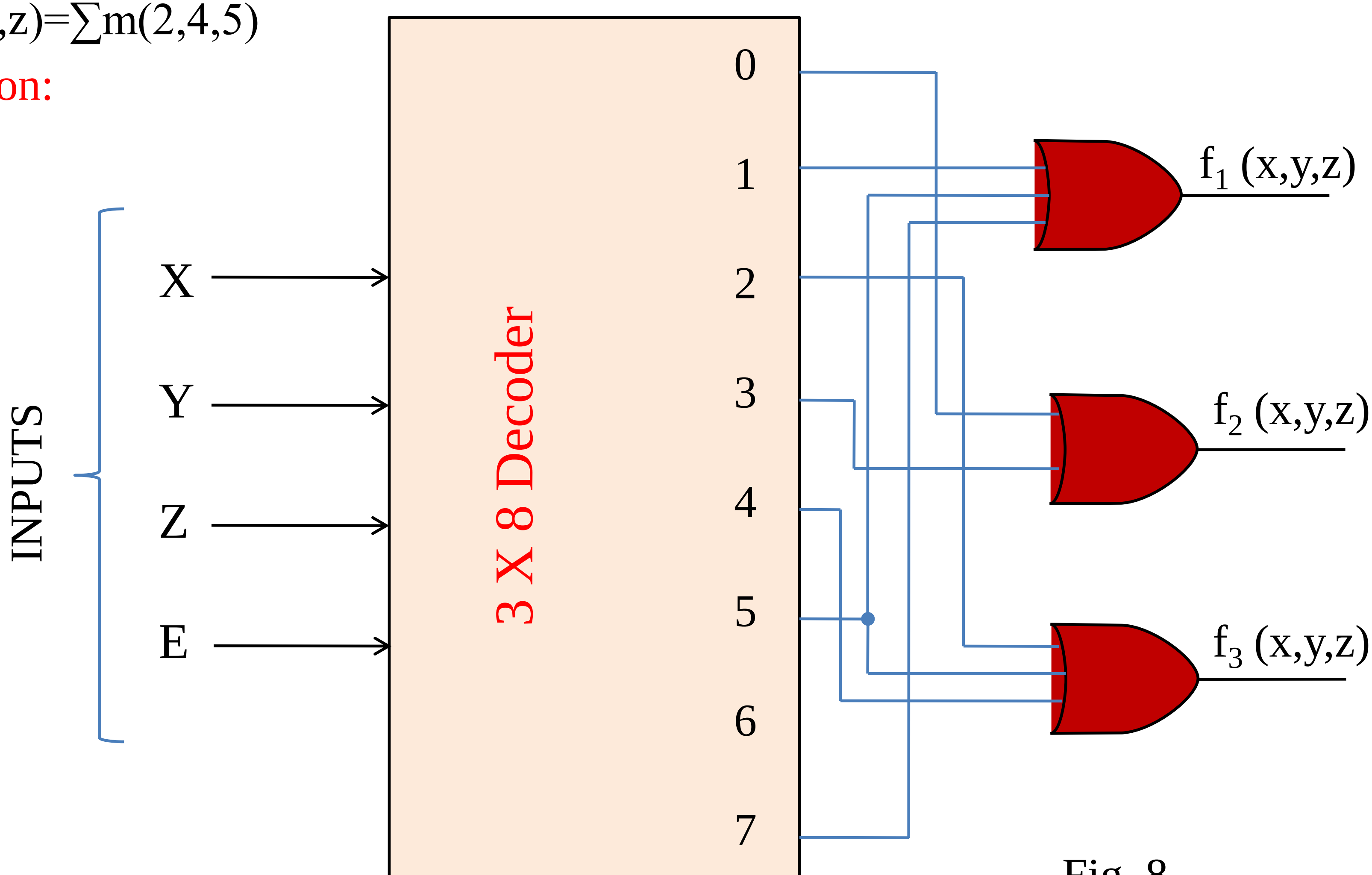


Fig. 8

EXAMPLE: A combinational circuit is defined by the following Boolean function. Design circuit with a Decoder and external gate.

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + x\,z$$

(UPTU, 2004-05)

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,z$$

SOLUTION: STEP 1: Write the given function F_1 in SOP form

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + (y + \bar{y})\,x\,z$$

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + x\,y\,z + x\,\bar{y}\,z$$

$$F_1(x, y, z) = \Sigma m\,(0,5,7)$$

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,z$$

$$F_2(x, y, z) = x\,y\,\bar{z} + (y + \bar{y})\,\bar{x}\,z$$

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,y\,z + \bar{x}\,\bar{y}\,z$$

$$F_2(x, y, z) = \Sigma m\,(1,3,6)$$

Boolean Function using Decoder:

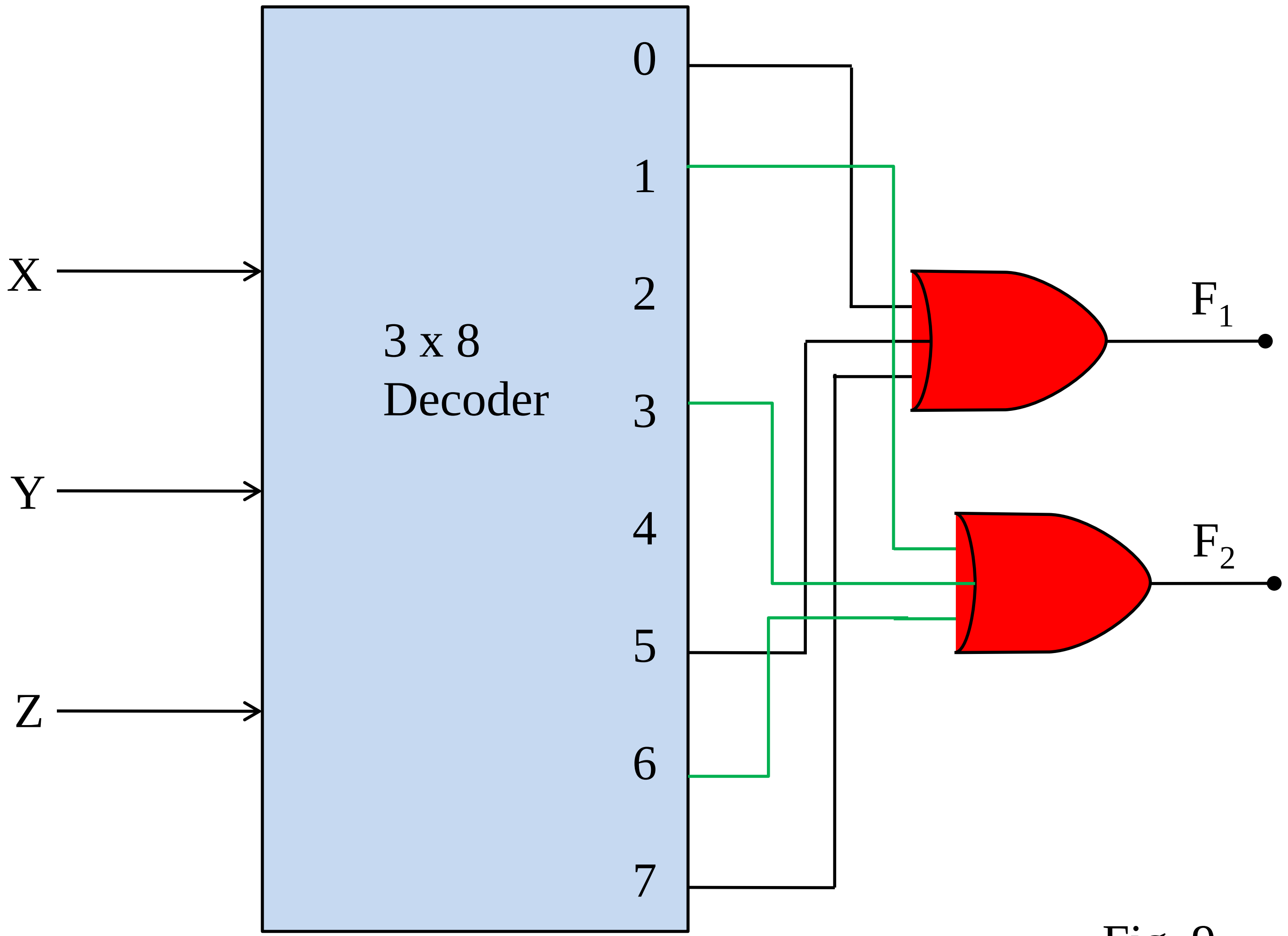


Fig. 9

ENCODER

- An Encoder is a combinational logic circuit.
- It performs the inverse operation of Decoder.
- The opposite process of decoding is known as Encoding.
- An Encoder converts an active input signal into a coded output signal.
- Block diagram of Encoder is shown in Fig.10. It has ‘M’ inputs and ‘N’ outputs.
- An Encoder has ‘M’ input lines, only one of which is activated at a given time, and produces an N-bit output code, depending on which input is activated.

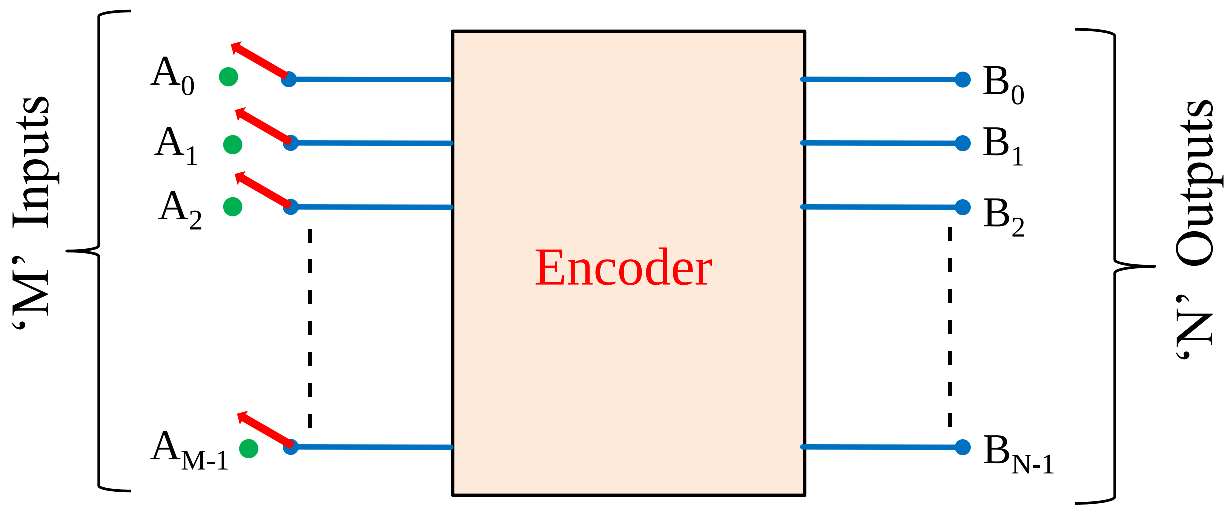


Fig. 10

- Encoders are used to translate the rotary or linear motion into a digital signal.
- The difference between Decoder and Encoder is that Decoder has Binary Code as an input while Encoder has Binary Code as an output.
- Encoder is an Electronics device that converts the analog signal to digital signal such as BCD Code.
- Types of Encoders

i. Priority Encoder
ii. Decimal to BCD Encoder
iii. Octal to Binary Encoder
iv. Hexadecimal to Binary Encoder

ENCODER

M=4
$M=2^2$
$M=2^N$
'M' is the input and
'N' is the output

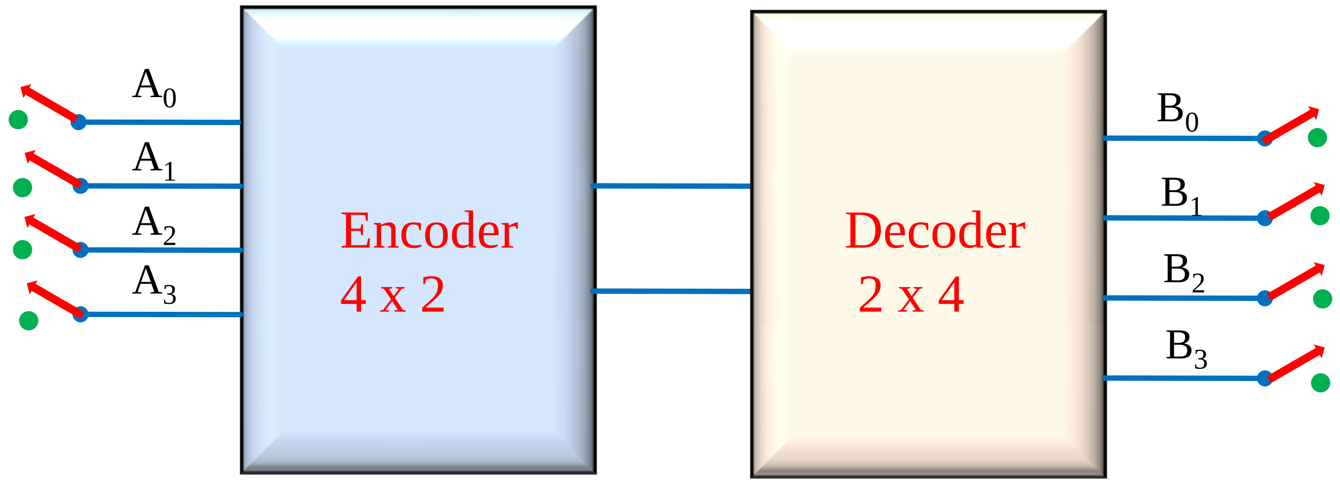


Fig. 11

ENCODER

M=4
$M=2^2$
$M=2^N$
'M' is the input and
'N' is the output

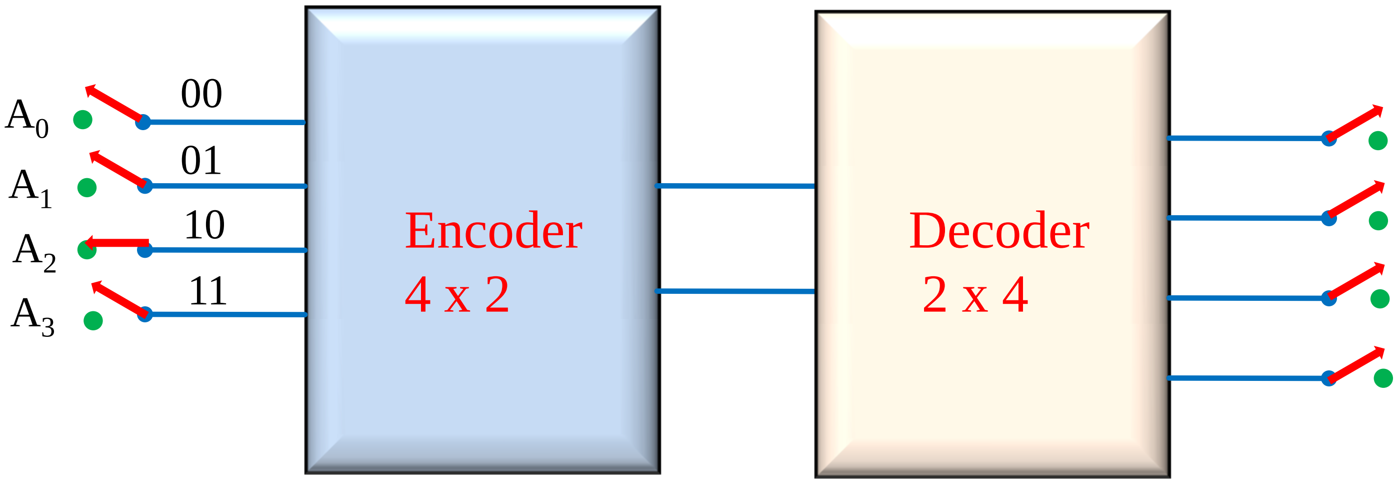


Fig. 12

ENCODER

M=4
$M=2^2$
$M=2^N$
'M' is the input and
'N' is the output

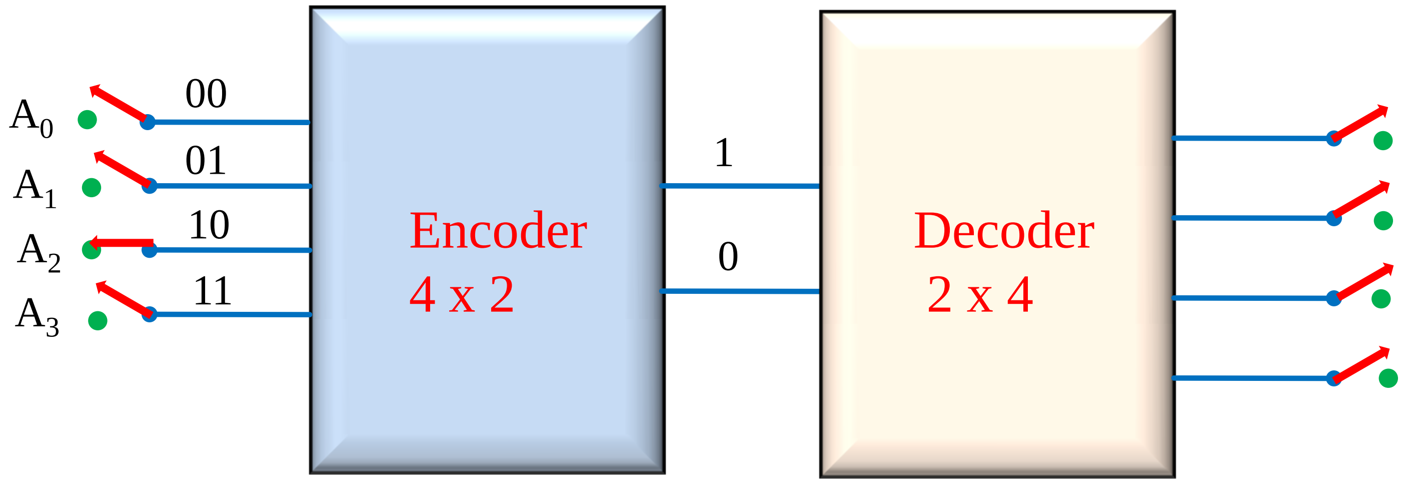


Fig. 13

ENCODER

M=4
$M=2^2$
$M=2^N$
'M' is the input and
'N' is the output

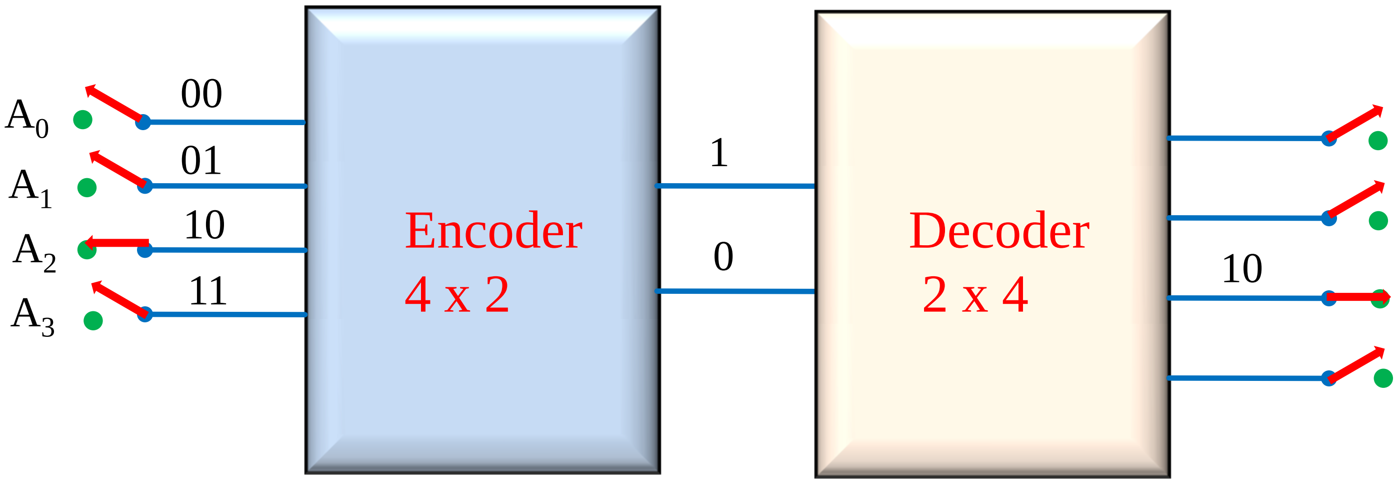
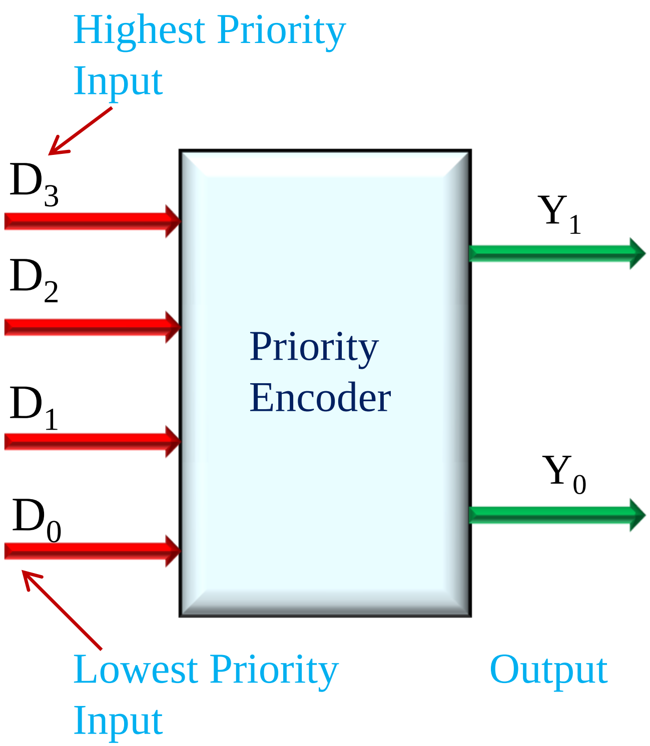


Fig. 14

PRIORITY ENCODER:

- As the name indicates, the priority is given to inputs line.
- If two or more input lines are high at the same time i.e 1 at the same time, then the input line with high priority shall be considered.
- Block diagram and Truth table of Priority Encoder are shown in fig.15



Block Diagram of Priority Encoder

TRUTH TABLE:

INPUTS				OUTPUTS		V
D_3	D_2	D_1	D_0	Y_1	Y_0	
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Fig.15

- There are four inputs D_0, D_1,D_2, D_3 and two outputs Y_1 and Y_2.
- D_3 has highest priority and D_0 is at lowest priority.
- If D_3=1 irrespective of other inputs then output Y_1Y_0=11.
- D_3 is at highest priority so other inputs are considered as don't care.

K-map for Y_1 and Y_0

D_3D_2 \ D_1D_0	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$Y_1 = D_2 + D_3$$

D_3D_2 \ D_1D_0	00	01	11	10
00	X	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$$Y_0 = D_3 + \overline{D_2}\,D_1$$

Fig. 16

LOGIC DIAGRAM OF PRIORITY ENCODER:

$$Y_1 = D_2 + D_3$$

$$Y_0 = D_3 + \overline{D_2}\, D_1$$

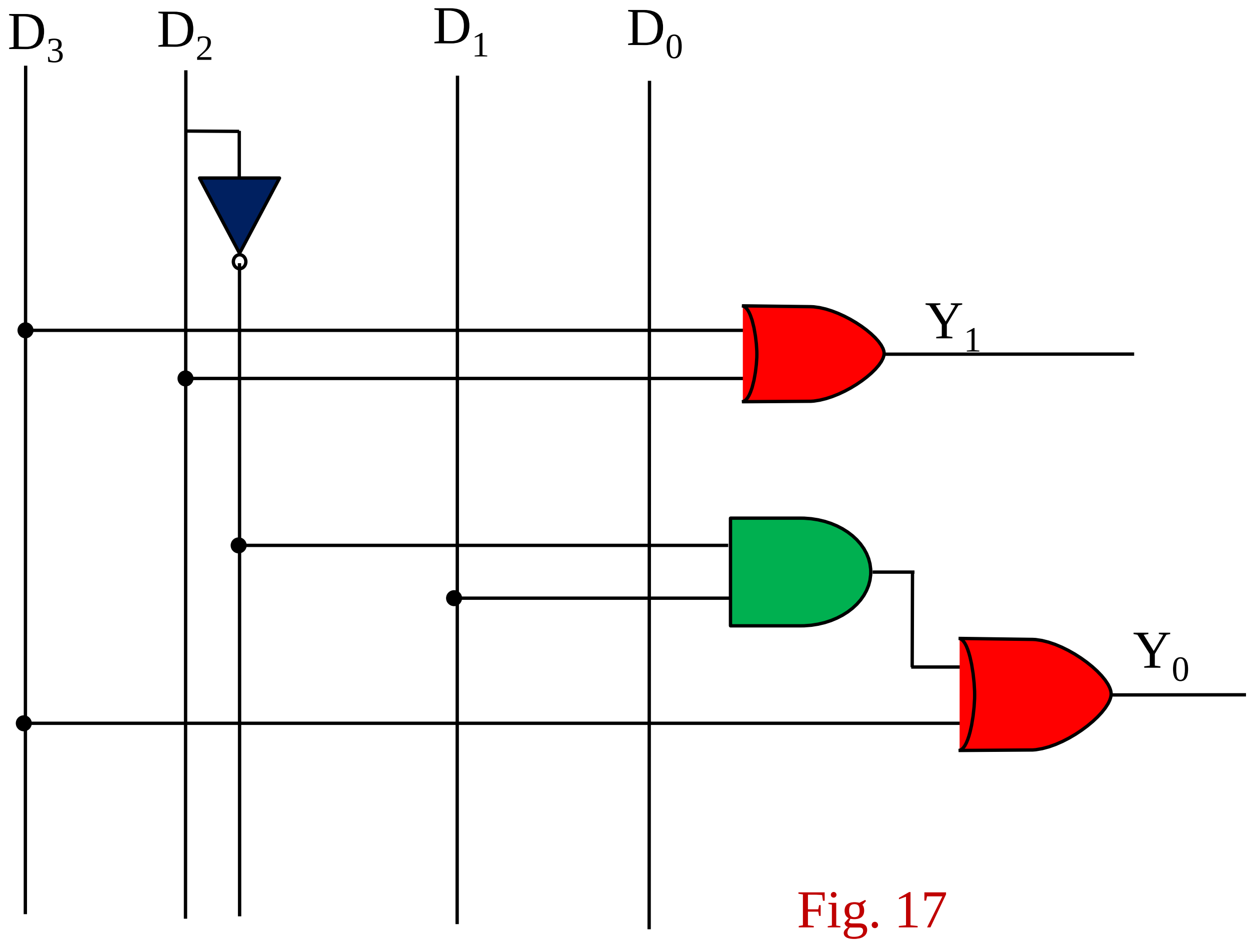


Fig. 17

DECIMAL TO BCD ENCODER:

- It has ten inputs corresponding to ten decimal digits (from 0 to 9) and four outputs (A,B,C,D) representing the BCD.
- The block diagram is shown in fig.18 and Truth table in fig.19

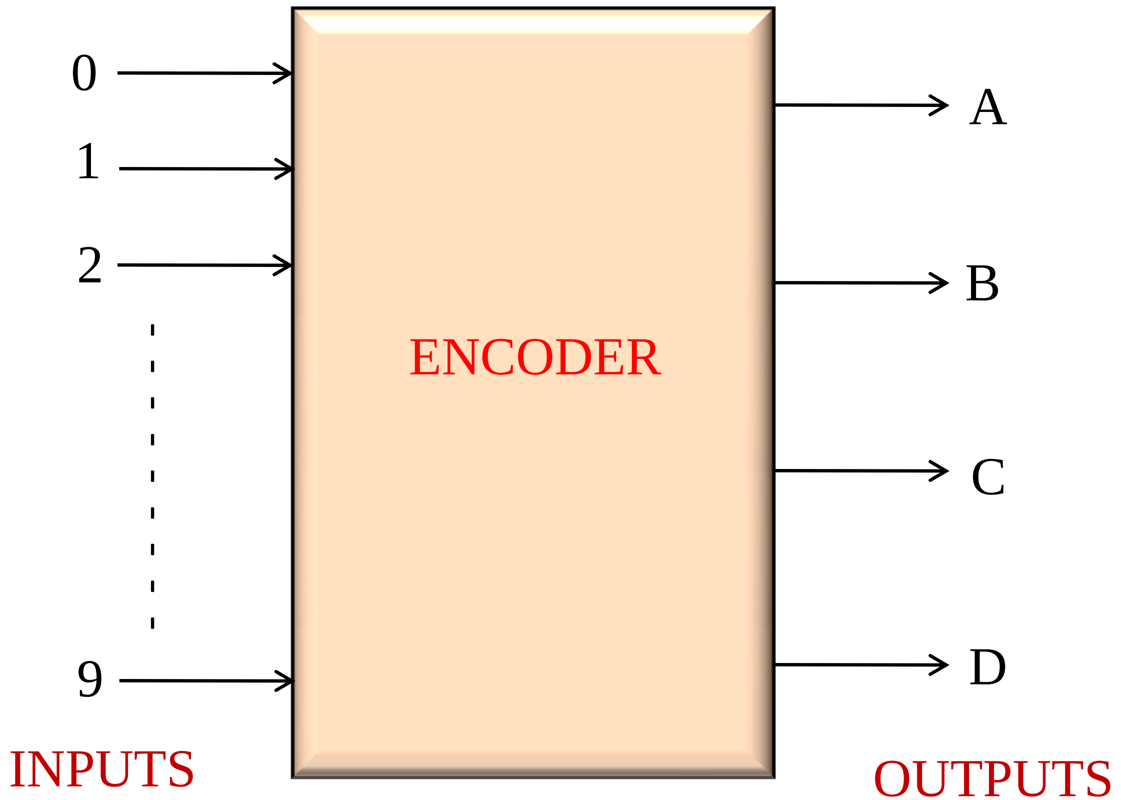


Fig. 18

Truth table:

INPUTS										BCD OUTPUTS			
0	1	2	3	4	5	6	7	8	9	A	B	C	D
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

Fig. 19

- From Truth Table it is clear that the output A is HIGH when input is 8 OR 9 is HIGH

  Therefore A=8+9

- The output B is HIGH when 4 OR 5 OR 6 OR 7 is HIGH

  Therefore B=4+5+6+7

- The output C is HIGH when 2 OR 3 OR 6 OR 7 is HIGH

  Therefore C=2+3+6+7

- Similarly D=1+3+5+7+9

  Logic Diagram is shown in fig.20

DECIMAL TO BCD ENCODER

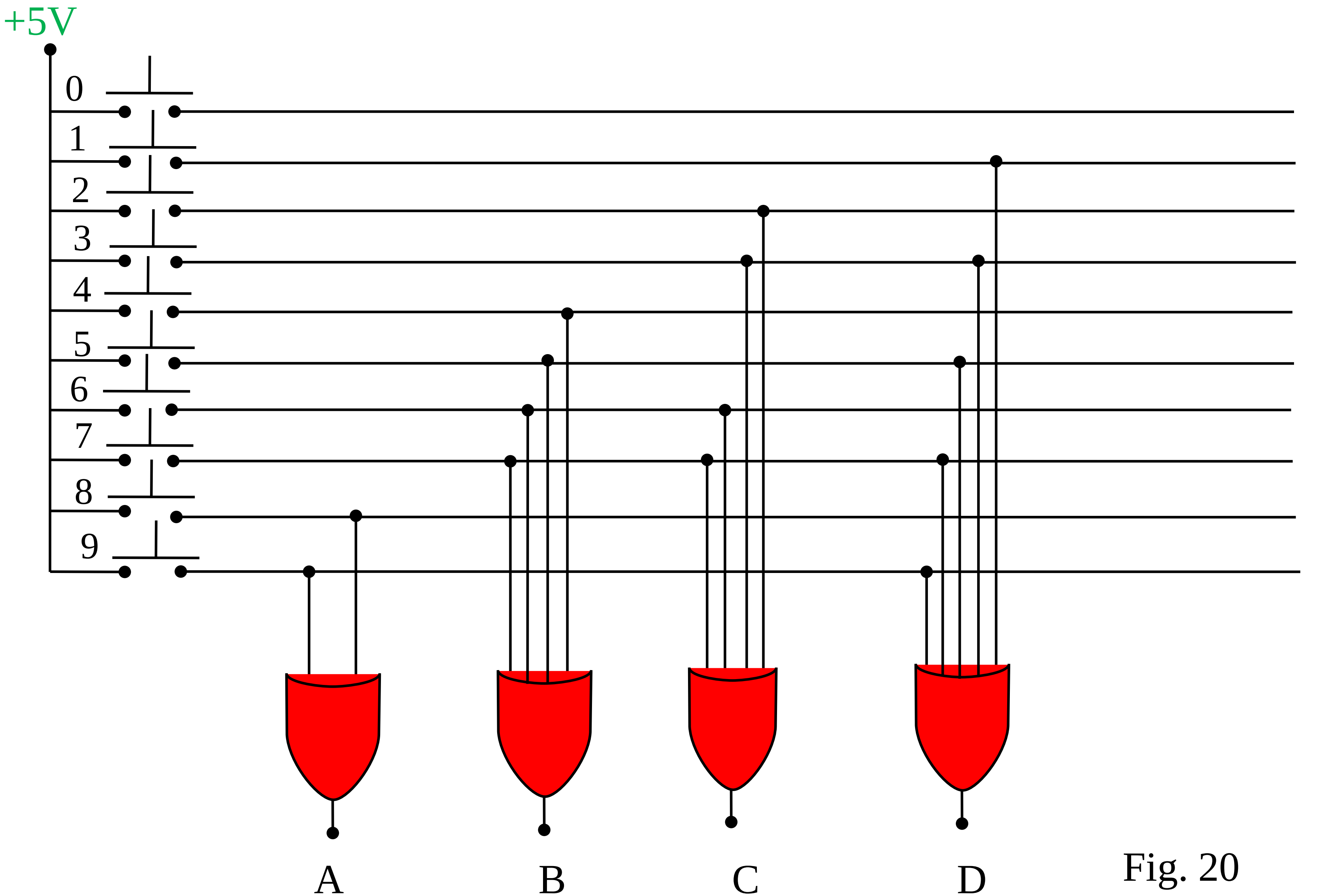


Fig. 20

OCTAL TO BINARY ENCODER:

- Block Diagram of Octal to Binary Encoder is shown in Fig. 21
- It has eight inputs and three outputs.
- Only one input has one value at any given time.
- Each input corresponds to each octal digit and output generates corresponding Binary Code.

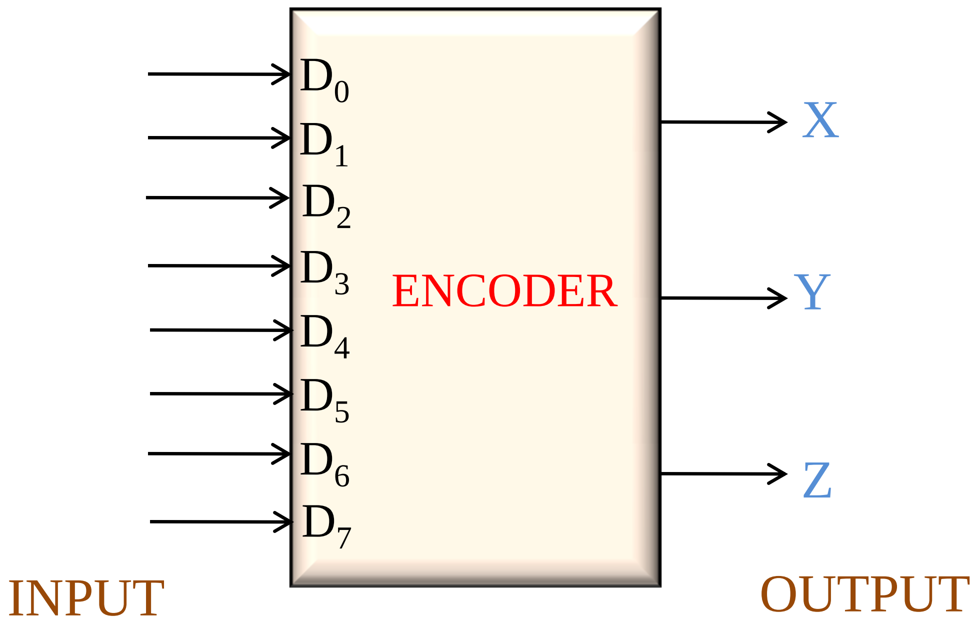


Fig. 21

TRUTH TABLE:

Fig. 22

INPUT								OUTPUT		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

From Truth table:

$$X = D_4 + D_5 + D_6 + D_7$$
$$Y = D_2 + D_3 + D_6 + D_7$$
$$Z = D_1 + D_3 + D_5 + D_7$$

- It is assume that only one input is HIGH at any given time. If two outputs are HIGH then undefined output will produced. For example D_3 and D_6 are HIGH, then output of Encoder will be 111. This output neither equivalent code corresponding to D_3 nor to D_6.
- To overcome this problem, priorities should be assigned to each input.
- Form the truth table it is clear that the output X becomes 1 if any of the digit D_4 or D_5 or D_6 or D_7 is 1.
- D_0 is considered as don't care because it is not shown in expression.
- If inputs are zero then output will be zero. Similarly if D_0 is one, the output will be zero.
-

$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$Z = D_1 + D_3 + D_5 + D_7$$

LOGIC DIAGRAM:

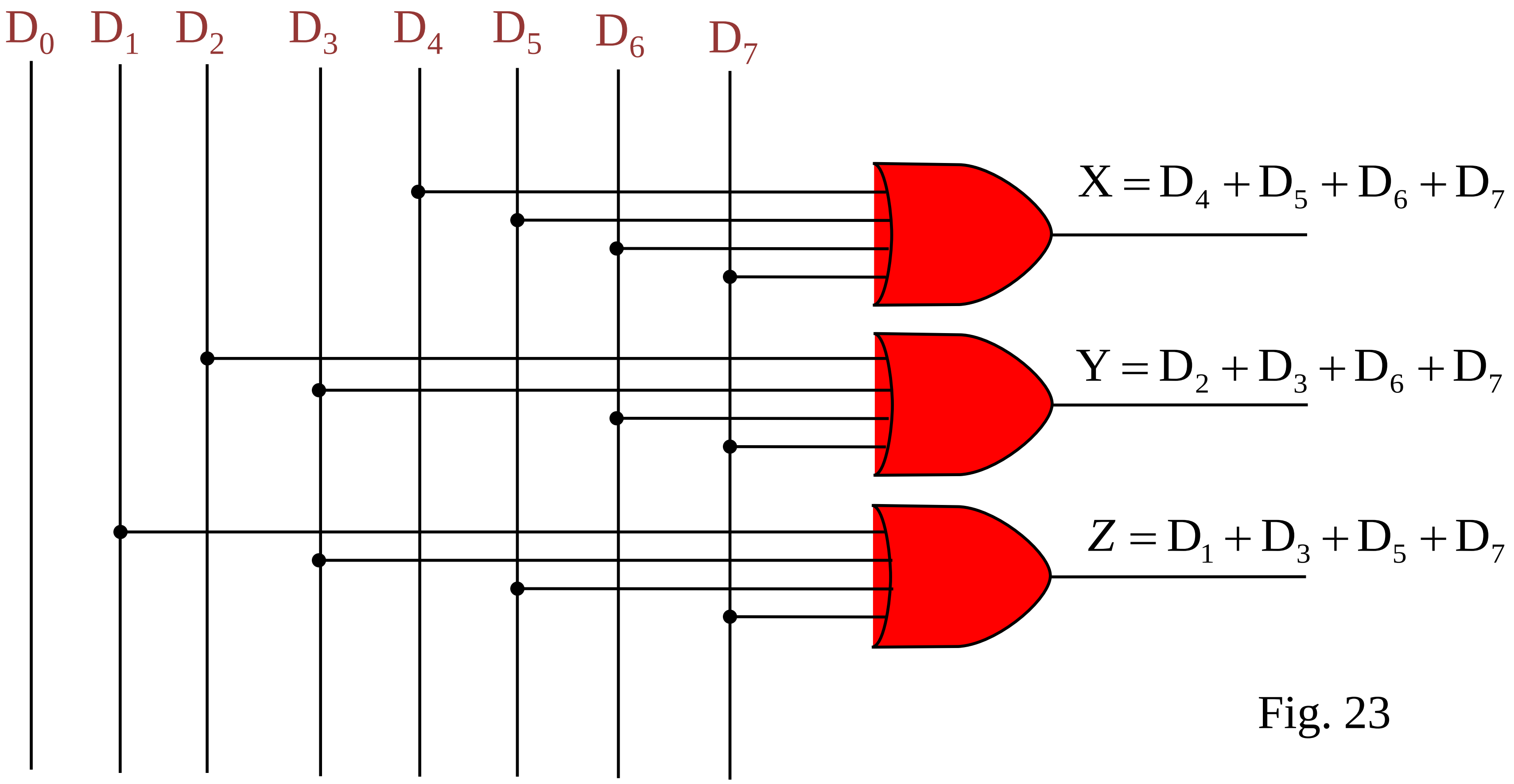


Fig. 23

THANK YOU