

Unit V

Synchronous Counters

by

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How To design Synchronous Counter

- Let us employ these techniques to design a MOD-8 counter to count in the following sequence: 0, 1, 2, 3, 4, 5, 6, 7.
- Step1:** Determined Flip Flop Used and Creating **state transition diagram.** (*Rajah Keadaan*)

$$N = 2^n$$

$$8 = 2^n$$

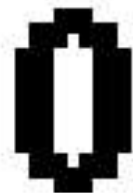
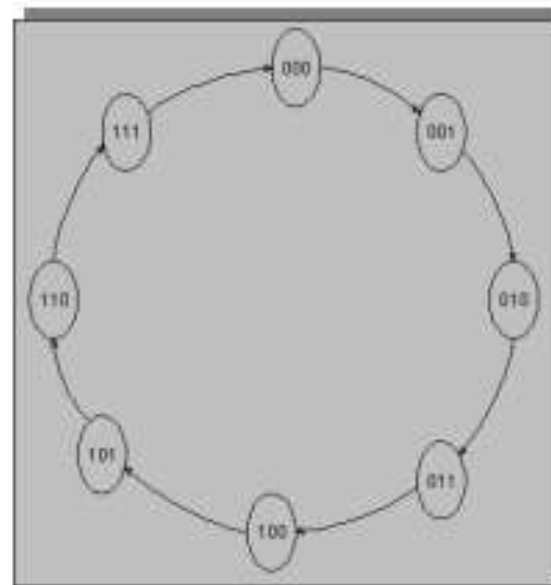
$$n = \log 8 / \log 2$$

$$= 3 \text{ Flip Flop (3 Bit)}$$

$$M = 2^n - 1$$

$$= 2^3 - 1 = 8 - 1 = 7$$

N = Modulo/MOD
n = Flip Flop Used
M = Maximum Number To Be Count



How To design Synchronous Counter

- **Step 2:** Creating present state-next state table

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

$$Q_0 = Q_A$$

$$Q_1 = Q_B$$

$$Q_2 = Q_C$$

How To Design Synchronous Counter

- **Step 3:** Expand the present state-next state table to form the transition table.

Excitation Table
(*Jadual Ujaan Flip Flop JK*)

Q	\bar{Q}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

'X' indicates a "don't care" condition.

Present State			Next State			Present inputs		
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A	$J_C K_C$	$J_B K_B$	$J_A K_A$
0	0	0	0	0	1	0X	0X	1X
0	0	1	0	1	0	0X	1X	X1
0	1	0	0	1	1	0X	X0	1X
0	1	1	1	0	0	1X	X1	X1
1	0	0	1	0	1	X0	0X	1X
1	0	1	1	1	0	X0	1X	X1
1	1	0	1	1	1	X0	X0	1X
1	1	1	0	0	0	X1	X1	X1

How To Design Synchronous Counter

- **Step 4:** Use Karnaugh maps to identify the present state logic functions for each of the inputs.

E.g. for J_2 we get:

		$\overline{Q_C Q_B}$			$Q_C Q_B$	
		00		01	11	10 →
$\overline{Q_A}$	0	0	0	X	X	
Q_A	1	0	1	X	X	

$$J_C = Q_B Q_A$$

Using similar techniques for the other inputs we get:

$$K_C = Q_B Q_A$$

$$J_B = Q_A$$

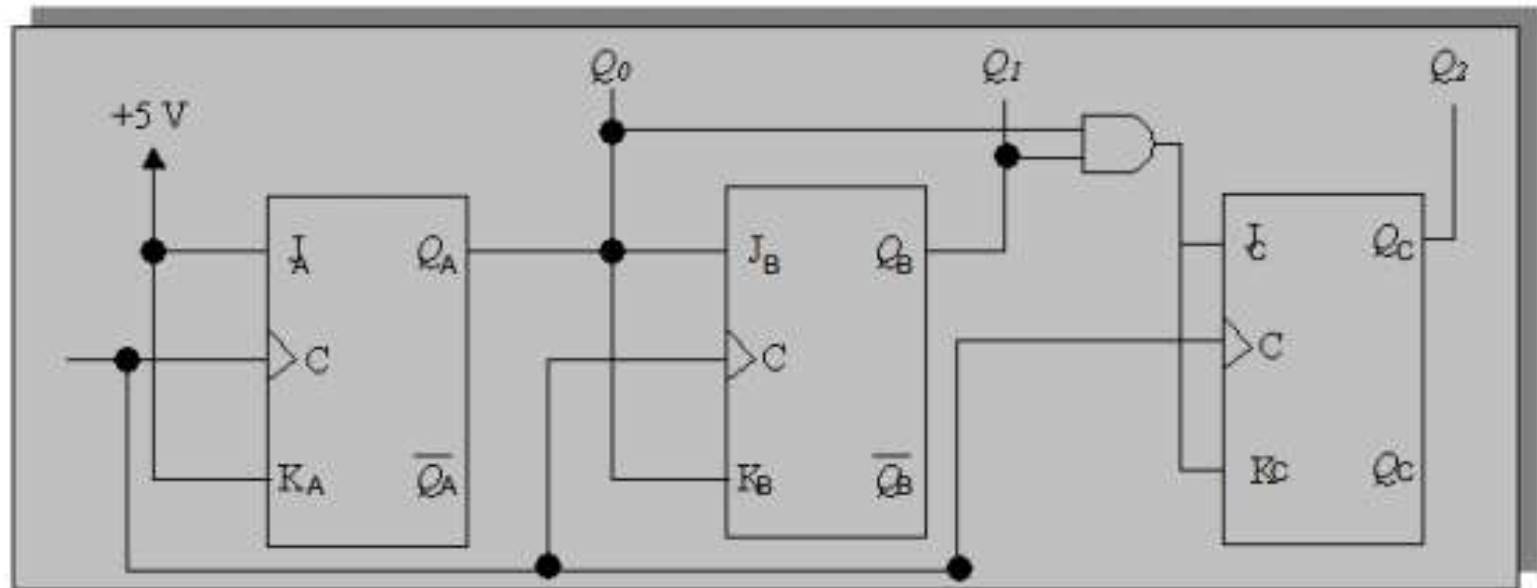
$$K_B = Q_A$$

$$J_A = 1$$

$$K_A = 1$$

How To Design Synchronous Counter

- **Step 5: Constructing Circuit**



Design a mod 6 synchronous up counter using J-K flip flop

Find number of flip-flops required to build the counter

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore n = 3$

i.e. Three flip-flops are required.

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Determine the transition table.

[illegible]

For J_A

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$$J_A = Q_B Q_C$$

For K_A

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X	X	X	X
1	0	1	X	X

$$K_A = Q_C$$

For J_B

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$$J_B = \bar{Q}_A Q_C$$

For K_B

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$$K_B = Q_C$$

For J_C

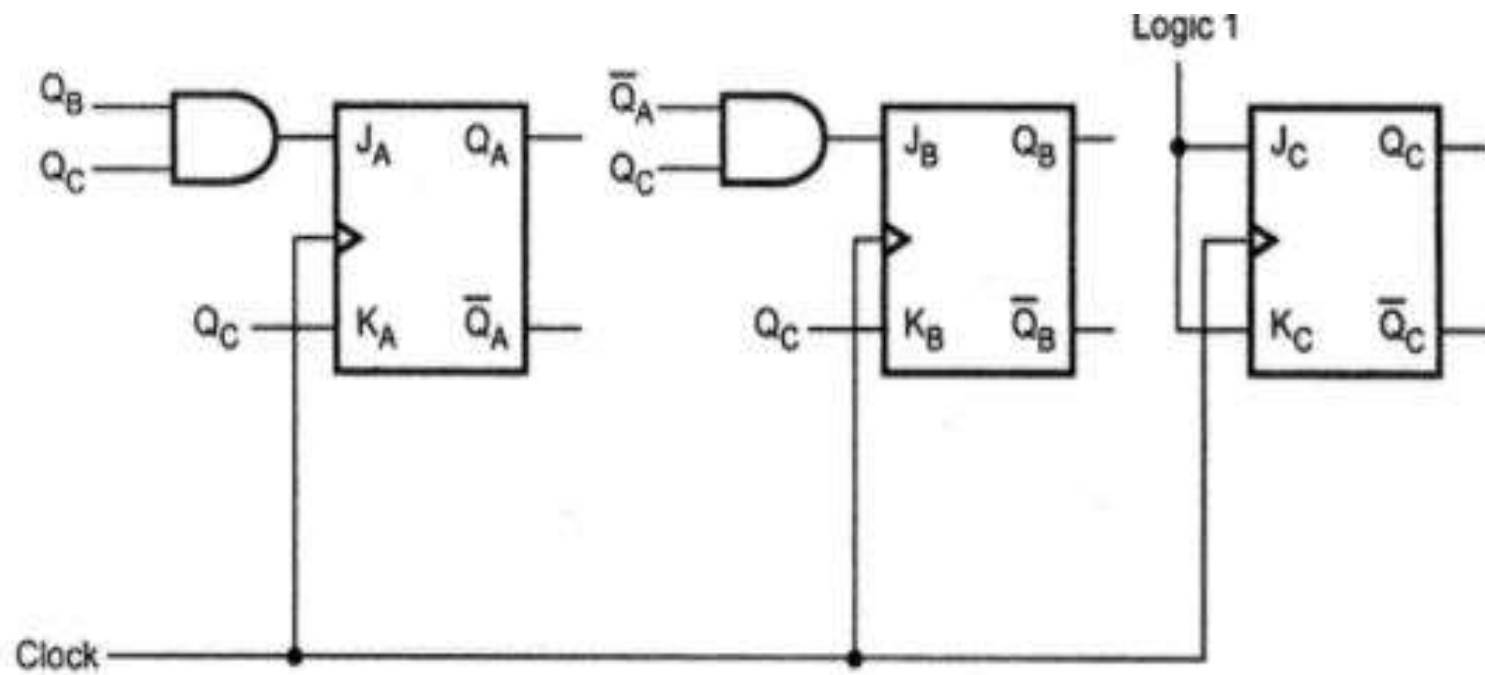
$Q_A \backslash Q_B Q_C$	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$$J_C = 1$$

For K_C

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X	1	1	X
1	X	1	X	X

$$K_C = 1$$



Design a mod 5 synchronous up counter using J-K flip flop

Step 1:

Determine the number of flip flop needed

Flip flop required are

$$2^n \geq N$$

Mod 5 hence $N=5$

$$\therefore 2^n \geq N$$

$$\therefore 2^n \geq 5$$

$N = 3$ i.e. 3 flip flop are required

Step 2:

Type of flip flop to be used: JK flip flop

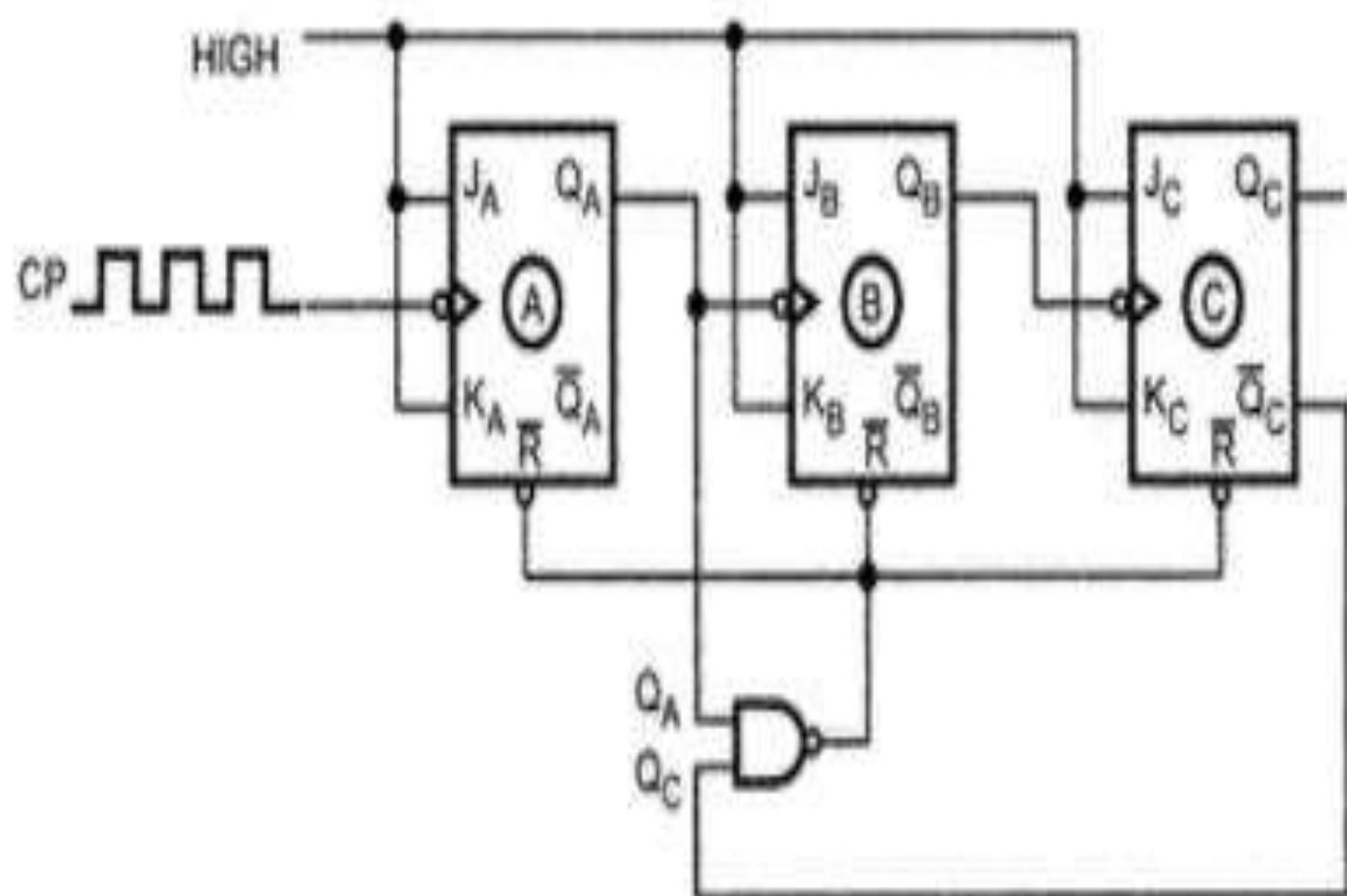
Step 3:

1) Excitation table for JK flip flop

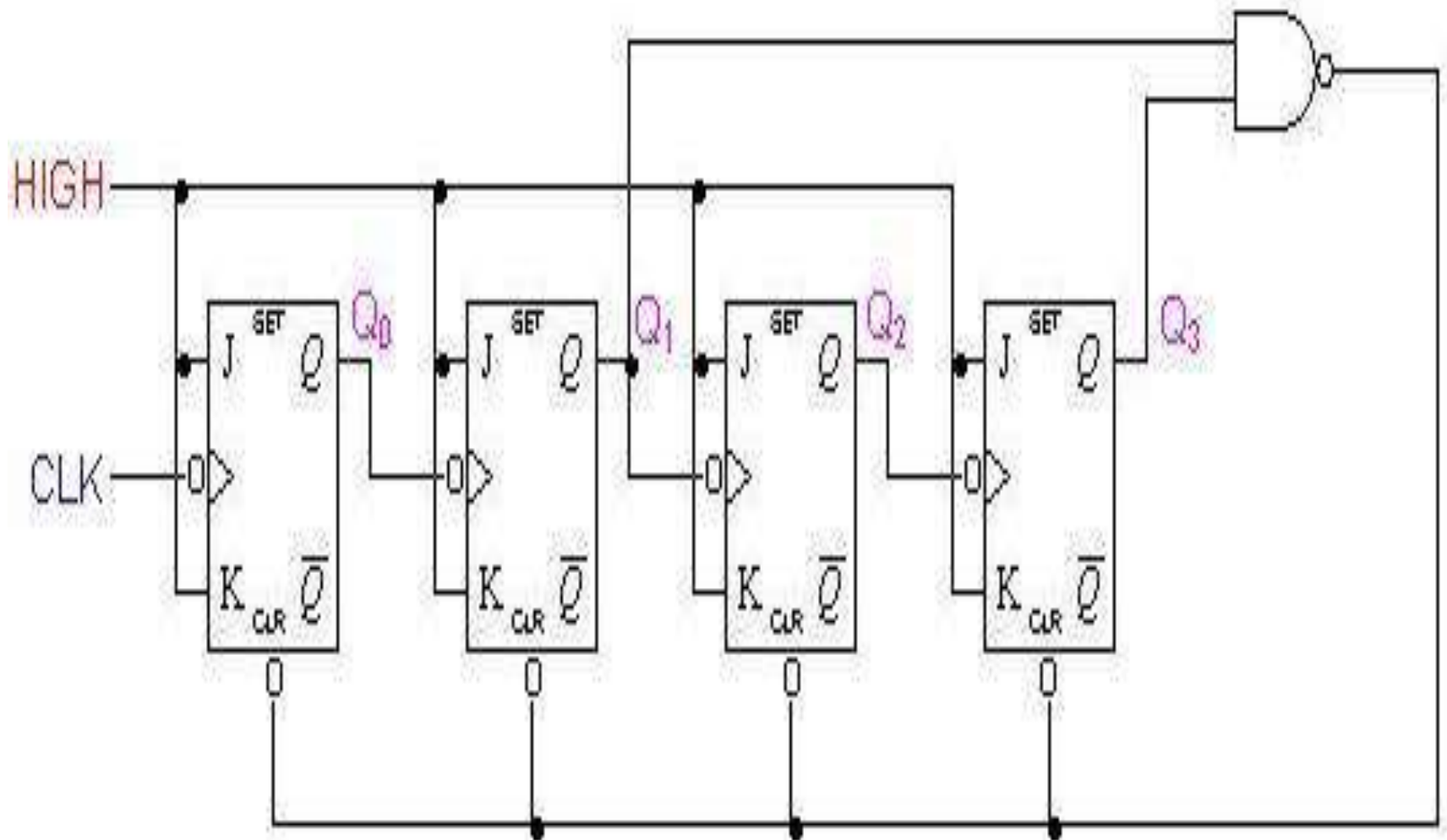
JK flip-flop			
$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

2) Excitation table for counter

[illegible]



Decade Counter



- Once the counter counts to ten (1010), all the flip-flops are being cleared.

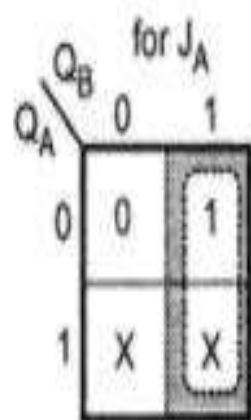
Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



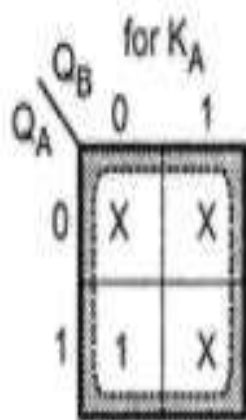
Design synchronous mod-3 counter with the following binary sequence using clocked JK flip-flops.

Count sequence : 0, 1, 2, 0, 1, 2,.....

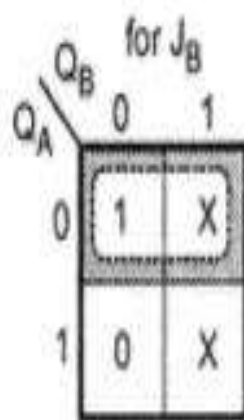
Present state		Next state		Flip-flop inputs			
Q_A	Q_B	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X



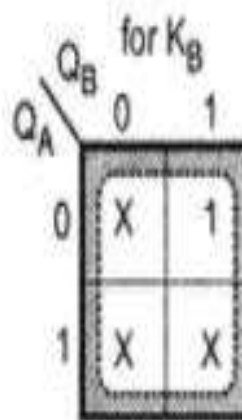
$$J_A = Q_B$$



$$K_A = 1$$



$$J_B = \bar{Q}_A$$



$$K_B = 1$$

