# Control Functions

- **Often actions need to only occur if a certain condition is true**
- **This is similar to an "if" statement in a programming language**
- **In digital systems, this is often done via a *control signal*, called a *control function***
  - **If the signal is 1, the action takes place**
- **This is represented as:**

**P: R2 ← R1**

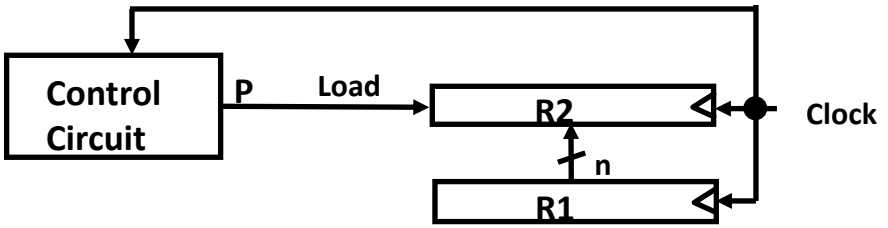
**Which means "if P = 1, then load the contents of register R1 into register R2", i.e., if (P = 1) then (R2 ← R1)**

# Hardware Implementation of Controlled Transfers

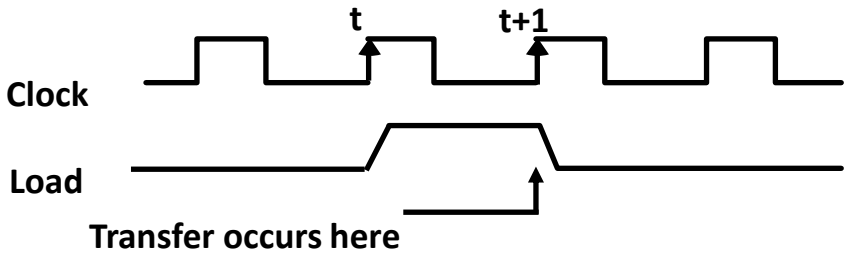
**Implementation of controlled transfer**

**P: R2 ← R1**

**Block diagram**




**Timing diagram**




- **The same clock controls the circuits that generate the control function and the destination register**
- **Registers are assumed to use *positive-edge-triggered* flip-flops**

# Basic Symbols in Register Transfer

| Symbols | Description | Examples |
|---|---|---|
| Capital letters & Numerals | Denotes a register | MAR, R2 |
| Parentheses () | Denotes a part of a register | R2(0-7), R2(L) |
| Arrow ← | Denotes transfer of information | R2 ← R1 |
| Colon : | Denotes termination of control function | P: |
| Comma , | Separates two micro-operations | A ← B, B ← A |

# CSE211

# Computer Organization and Design

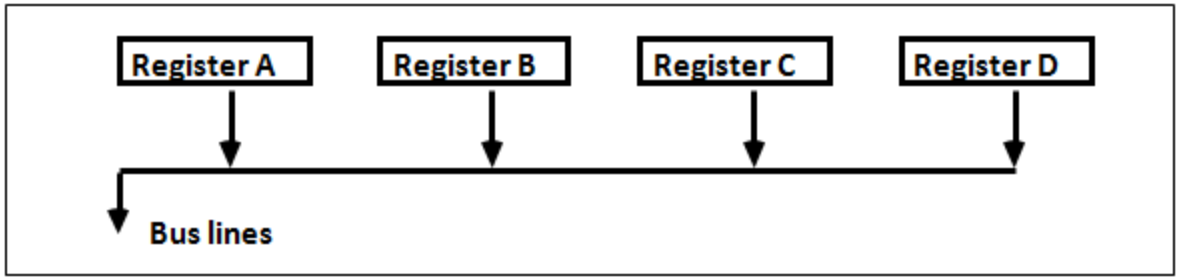
- ***Bus and Memory Transfers***

# Overview

- Register Transfer Language
- Register Transfer
- **Bus and Memory Transfers**
- Logic Micro-operations
- Shift Micro-operations
- Arithmetic Logic Shift Unit

# Connecting Registers - Bus Transfer

**From a register to bus: BUS ← R**




- **One way of constructing common bus system is with multiplexers**
- **Multiplexer selects the source register whose binary information is kept on the bus.**

- **Construction of bus system for 4 register (Next Fig)**
  - **4 bit register X 4**
  - **four 4X1 multiplexer**
  - **Bus selection S0, S1**

- Bus System is used to carry the data from one location to another.

A) True

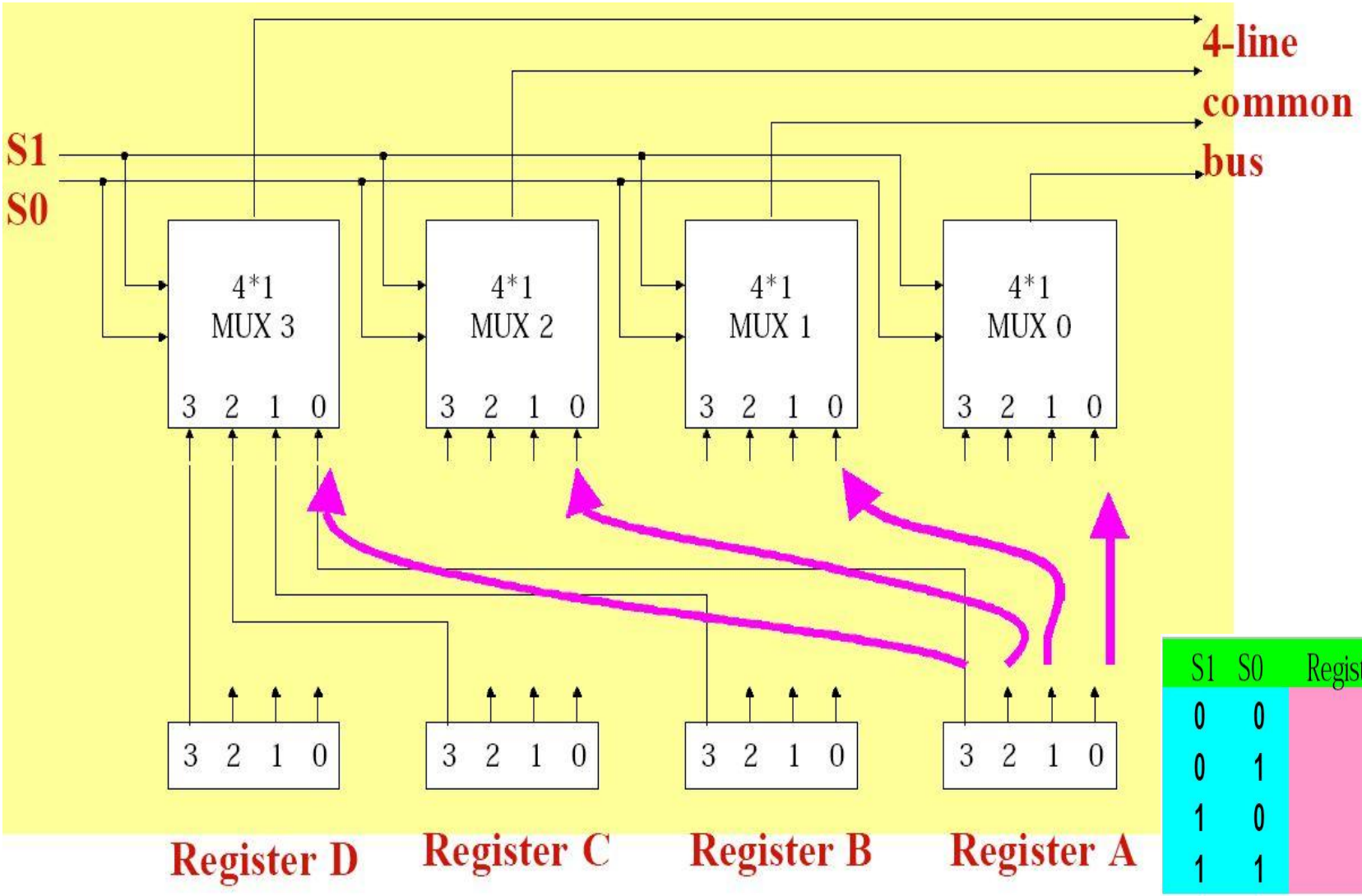
B) False

# Connecting Registers - Bus Transfer

- For a bus system to multiplex k registers of n bits each
  - No. of multiplexer = n
  - Size of each multiplexer = k x 1

- **Construction of bus system for 8 register with 16 bits**
  - **16 bit register X 8**
  - **Sixteen 8X1 multiplexer**
  - **Bus selection S0, S1, S2**

# Connecting Registers - Bus Transfer

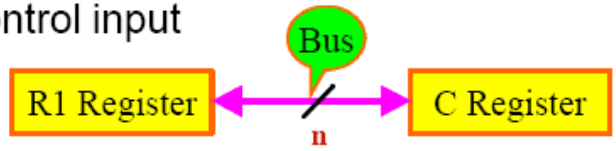



| S1 | S0 | Register selected |
|---|---|---|
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

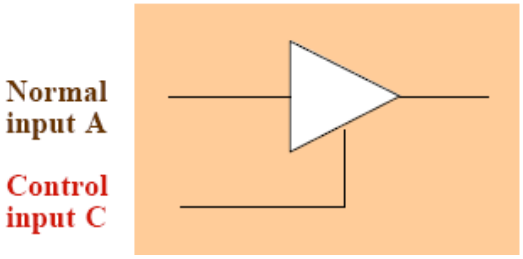
# Connecting Registers - Bus Transfer

- Bus Transfer
  - The content of register C is placed on the bus, and the content of the bus is loaded into register R1 by activating its load control input

$$\left.\begin{array}{l} Bus \leftarrow C,\ R1 \leftarrow Bus \\ R1 \leftarrow C \end{array}\right\} =$$




- Three-State Bus Buffers
  - A bus system can be constructed with ***three-state gates*** *instead of* ***multiplexers***
  - Tri-State : 0, 1, High-impedance(***Open circuit***)
  - Buffer
    - » A device designed to be inserted between other devices to match impedance, to prevent mixed interactions, and ***to supply additional drive or relay capability***
    - » Buffer types are classified as inverting or noninverting
  - Tri-state buffer gate : Fig. 4-4
    - » When control input =1 : The output is enabled(output Y = input A)
    - » When control input =0 : The output is disabled(output Y = high-impedance)

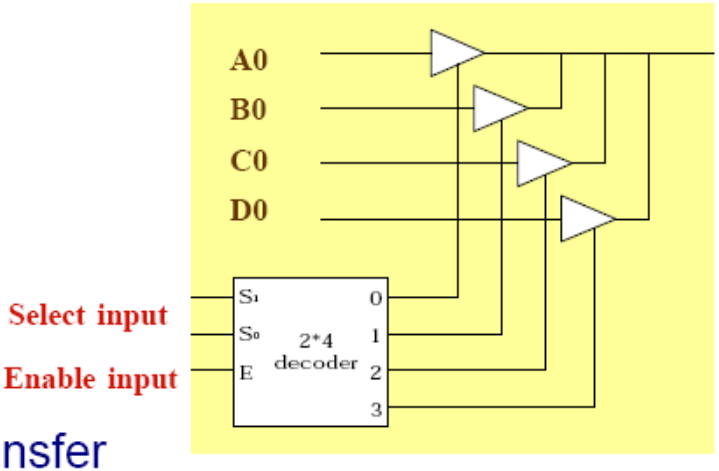



If C=1, Output Y = A

If C=0, Output = High-impedance

# Connecting Registers - Bus Transfer

- The construction of a bus system with tri-state buffer : ***Fig.***
  - The outputs of four buffer are connected together to form a single bus line(Tri-state buffer
  - No more than one buffer may be in the active state at any given time(2 X 4 Decoder
  - To construct a common bus for 4 register with 4 bit : Fig.




AR: Address Reg.
DR: Data Reg.
M : Memory Word(Data)

$READ: \quad DR \leftarrow M[AR]$

$WRITE: \quad M[AR] \leftarrow R1$

- Memory Transfer
  - Memory read : A transfer information into DR from the memory word M selected by the address in AR
  - Memory Write : A transfer information from R1 into the memory word M selected by the address in AR

- Which of the following digital circuit is used for designing the Bus System?

A) With MUX

B) With Decoder and Buffer

C) Both A and B

D) None of the above

# Memory Transfer

**Memory is usually accessed in computer systems by putting the desired address in a special register, the Memory Address Register (MAR, or AR)**