Unit IV

Introduction to Sequential Logic Circuits

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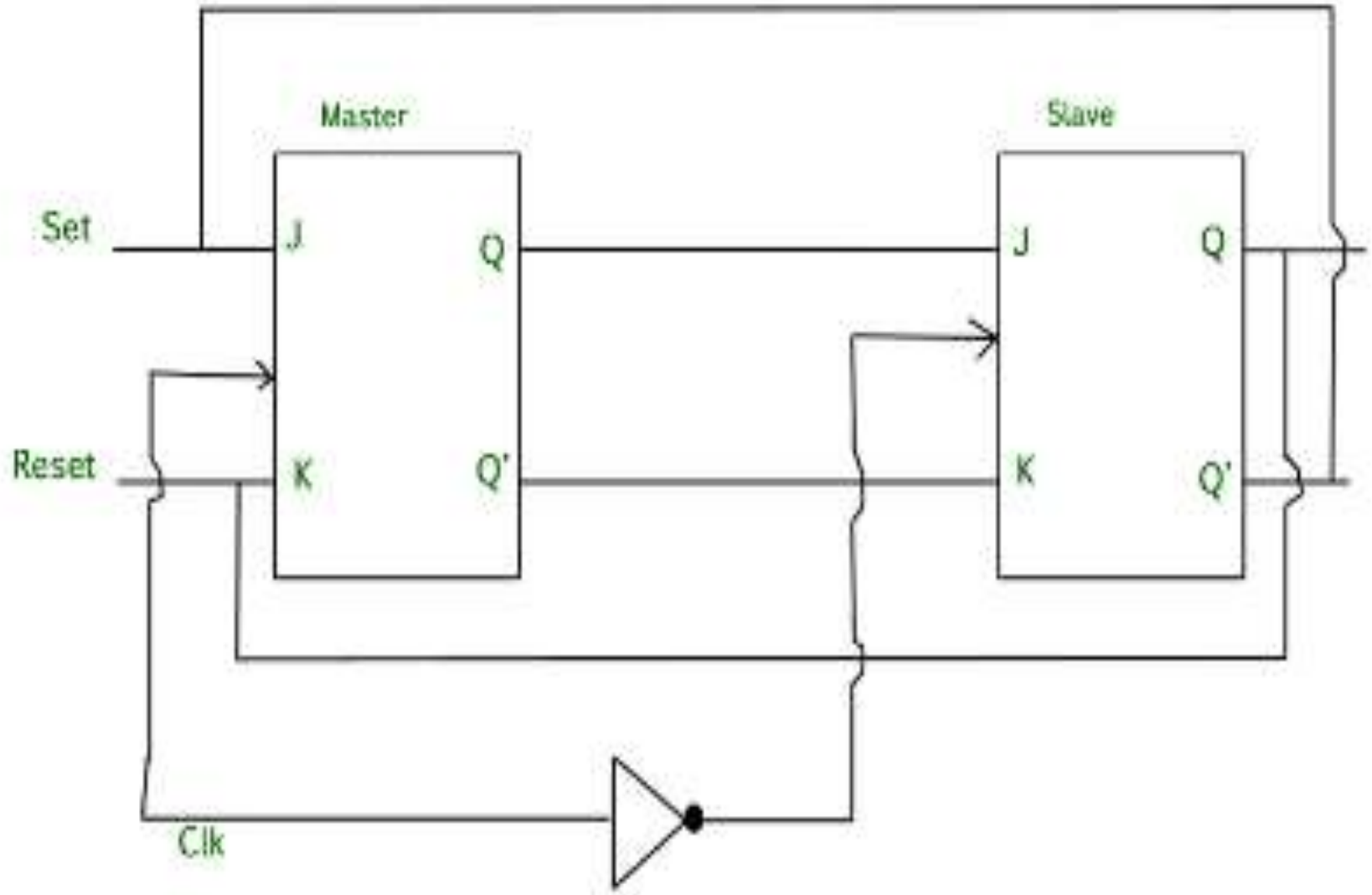
Master Slave JK flip flop

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **“master”** and the other as a **“slave”**. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.

In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.



Master-slave JK Flip-Flop

Working of a master slave flip flop

- When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
- Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
- If J=0 and K=1, the high Q’ output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.

- If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
- If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
- If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

T-Flip Flop: Toggle Flip Flop

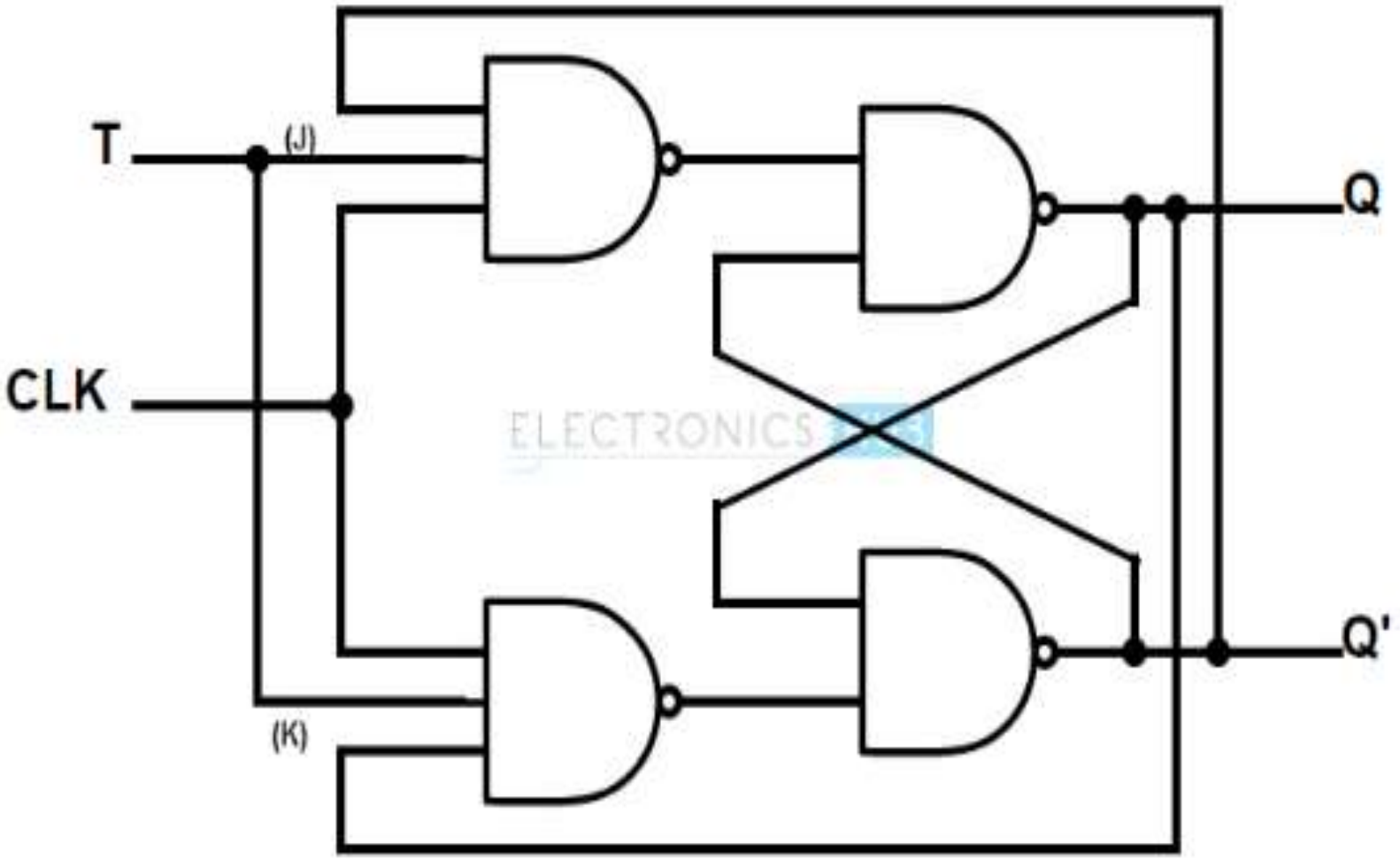
- T flip-flops are similar to JK flip-flops. T flip-flops are single input version of JK flip-flops. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip flop has only one input along with Clock pulse. These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle. So they are called as Toggle flip-flop.
- When J=K=0, then T=0

  If CP=1 the output is same as previous state. It is Memory state of Flip Flop.

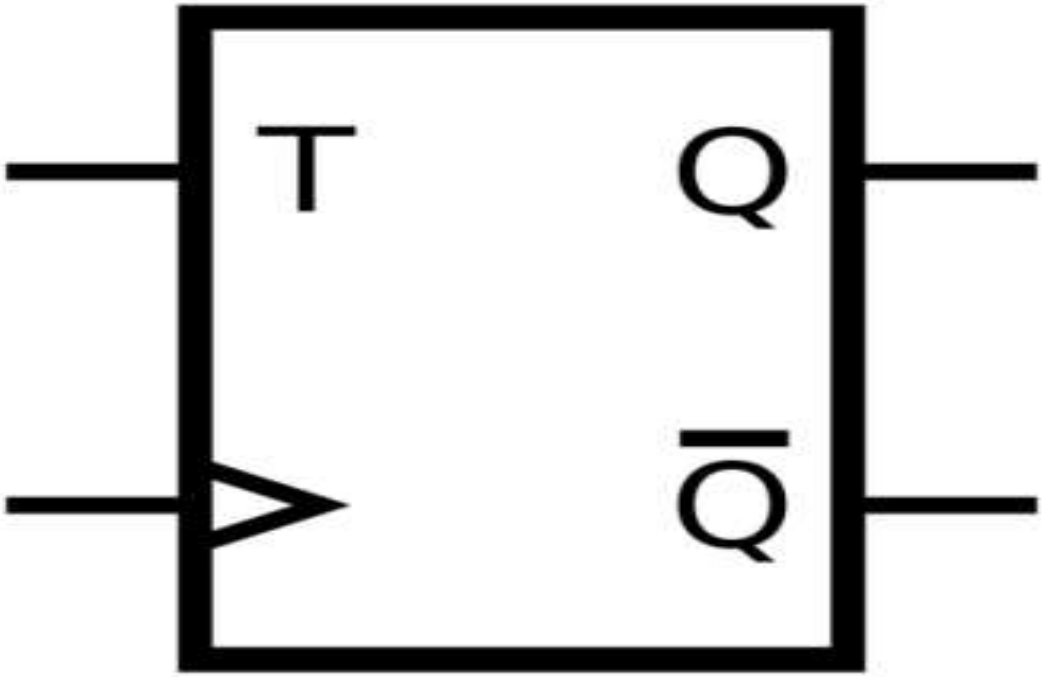
Cont...

- **When J=K=1, then T=1**

  If Clock pulse is high (CP=1) then, the output begins to toggle. So, for a previous value of Q = 1, it switches to Q=0 and for a previous value of Q = 0, it switches to Q=1.
- **Here also the restriction on the pulse width can be eliminated with a master-slave or edge triggered construction. Take a look at the circuit and truth table given for T Flip Flop.**


T
(J)
CLK
(K)
Q
Q'

Block Diagram



CLK	T	Q	Q+1
_↑‾	0	0	0
_↑‾	0	1	1
_↑‾	1	0	1
_↑‾	1	1	0

- Then we can define the switching action of the toggle flip-flop in Boolean form as being:
- $Q+1 = T.Q' + T'.Q$
- Where: Q represents the present steady state of the flip-flop and Q+1 is the next switching state.

Quick Quiz

- In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____

  a) D flip-flop
  b) S-R flip-flop
  c) T flip-flop
  d) S-K flip-flop

Quick Quiz

- The only difference between a combinational circuit and a flip-flop is that _____

  a) The flip-flop requires previous state
  b) The flip-flop requires next state
  c) The flip-flop requires a clock pulse
  d) The flip-flop depends on the past as well as present states

Quick Quiz

- The flip-flop is only activated by _____

  a) Positive edge trigger
  b) Negative edge trigger
  c) Either positive or Negative edge trigger
  d) Sinusoidal trigger

Quick Quiz

- D flip-flop is a circuit having _____
  a) 2 NAND gates
  b) 3 NAND gates
  c) 4 NAND gates
  d) 5 NAND gates

Quick Quiz

- Which of the following is the Universal Flip-flop?
  a) S-R flip-flop
  b) J-K flip-flop
  c) Master slave flip-flop
  d) D Flip-flop