UNIT-IV

Fundamentals of semiconductor devices and digital circuits

Lecture 24

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Voltage Levels and the static discipline

The representations differed not only in the signal type (for example, current versus voltage), but also in the signal values (for example, 5 V versus 4 V to represent a logical 1).

Because we require that digital devices built by various manufacturers talk to each other, the devices must adhere to a common representation.

The representation must allow for large enough design margins so that devices can be built out of a wide range of technologies.

Furthermore, the representation should be such that the devices operate correctly even in the presence of some amount of noise.

The *static discipline* is a specification for digital devices. The static discipline requires devices to adhere to a common representation, and to guarantee that they interpret correctly inputs that are valid logical signals according to the common representation, and to produce outputs that are valid logical signals provided they receive valid logical inputs.

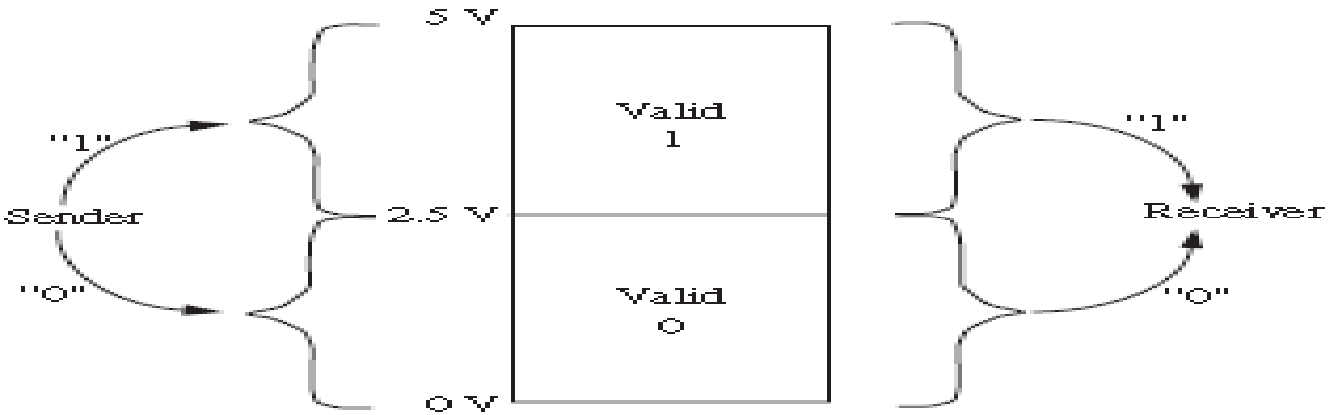
Voltage Levels and the static discipline

One of the representations we saw earlier divided a voltage range into two intervals and associated a logic value with each, namely,

$$\text{Logic } 0 : 0.0 \text{ V} \leq V < 2.5 \text{ V}.$$

$$\text{Logic } 1 : 2.5 \text{ V} \leq V \leq 5.0 \text{ V}.$$

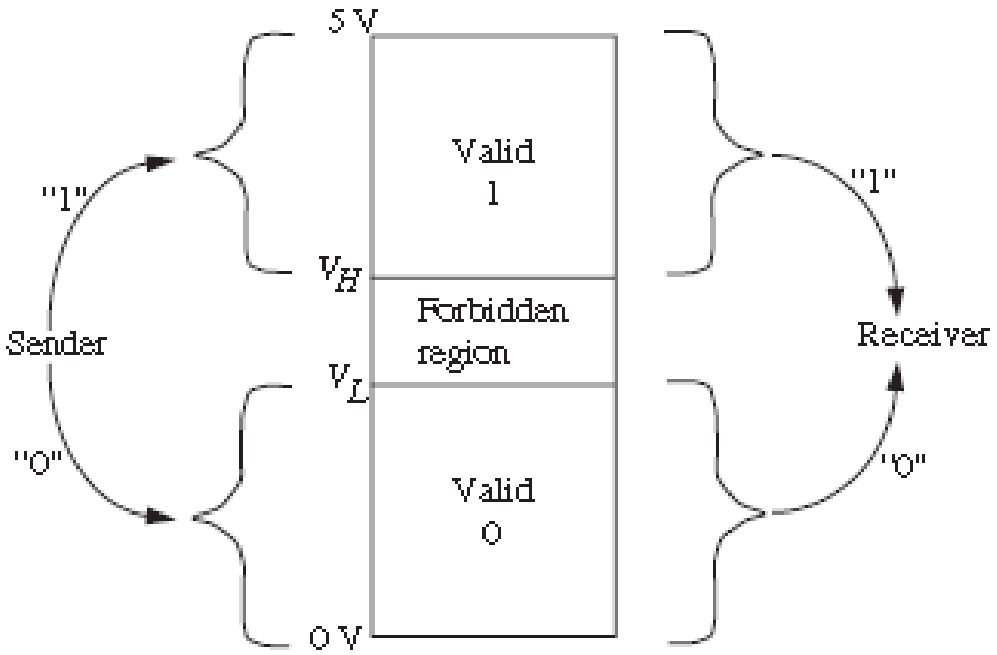
This simple representation is illustrated in Figure. According to this representation, if a receiver saw 2 V on a wire it would interpret it as a 0. Similarly, a receiver would interpret 4 V on a wire as a 1. Assume, for now, that values outside this range are invalid.



There is one problem, however. What does the receiver do if it sees a voltage level of 2.5 V on the wire? Does it interpret this signal value as a logical 0 or as a logical 1?

To eliminate such confusion, we further prescribe a ***forbidden region*** that separates the two valid regions. We further allow the behavior of the receiving device to be undefined if it sees a voltage in the forbidden region.

Thus, the correspondence between voltage levels and logic signals from the viewpoint of a receiver might look like:

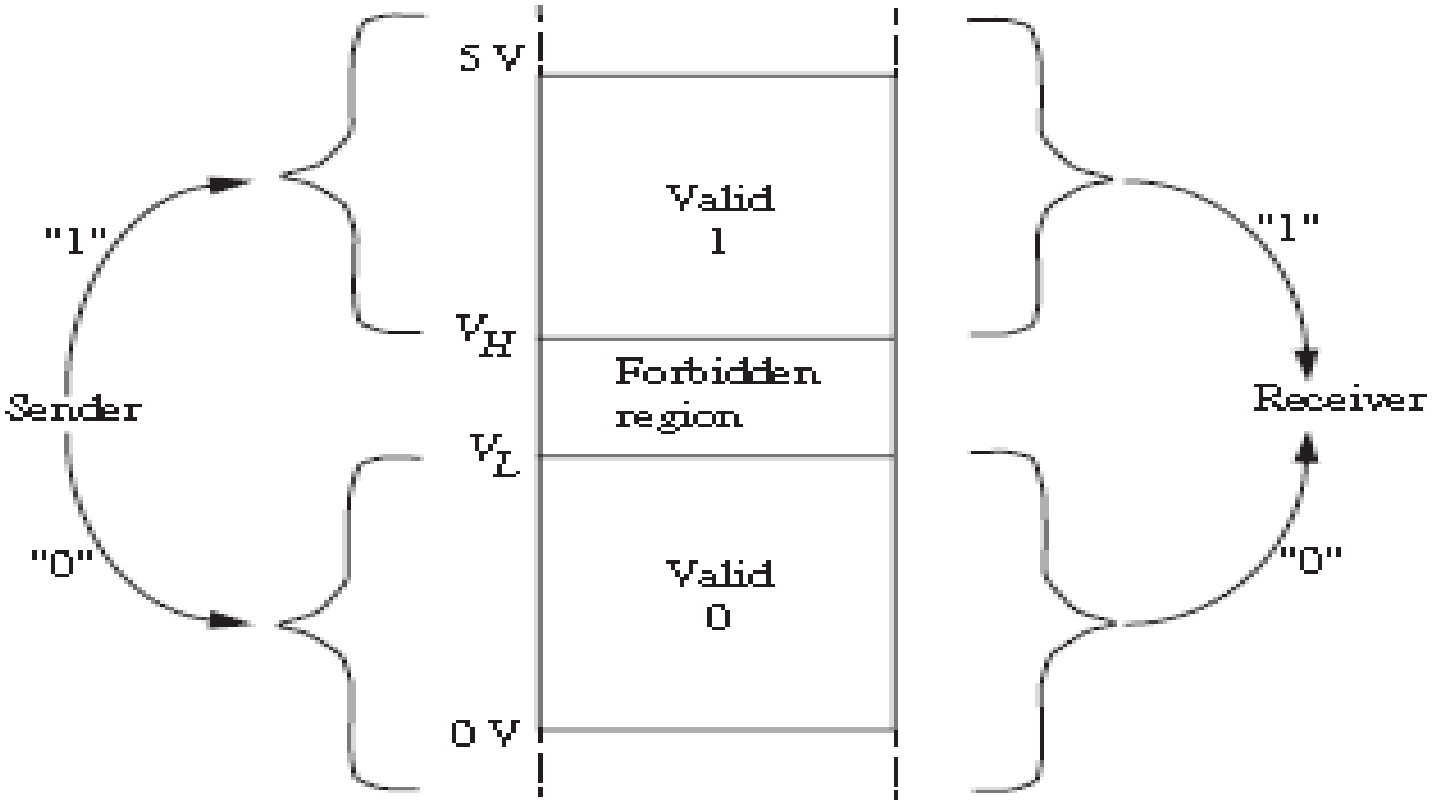


Logic 0 : $0\ V \leq V \leq 2\ V$.

Logic 1 : $3\ V \leq V \leq 5\ V$.

This representation using a forbidden region is illustrated in Figure. In this representation, a receiver interprets signals above 3 V as a logical 1 and voltages below 2 V as a logical 0. Signal voltages between 2 V and 3 V are invalid.

It often turns out that practical circuits are able to correctly interpret values outside the extremum points (below 0 volts for a logical 0 and above 5 V for a logical 1), within certain limits, of course. When devices can make this interpretation, our representation with the forbidden region allows senders to output any voltage value above V_H for a logical 1. Similarly, senders can output any value below V_L for a logical 0 (see Figure).



There is one other problem with our representations illustrated in previous Figures They do not offer any immunity to noise. As an illustration of the notion of noise margins, consider the two situations in Figure.

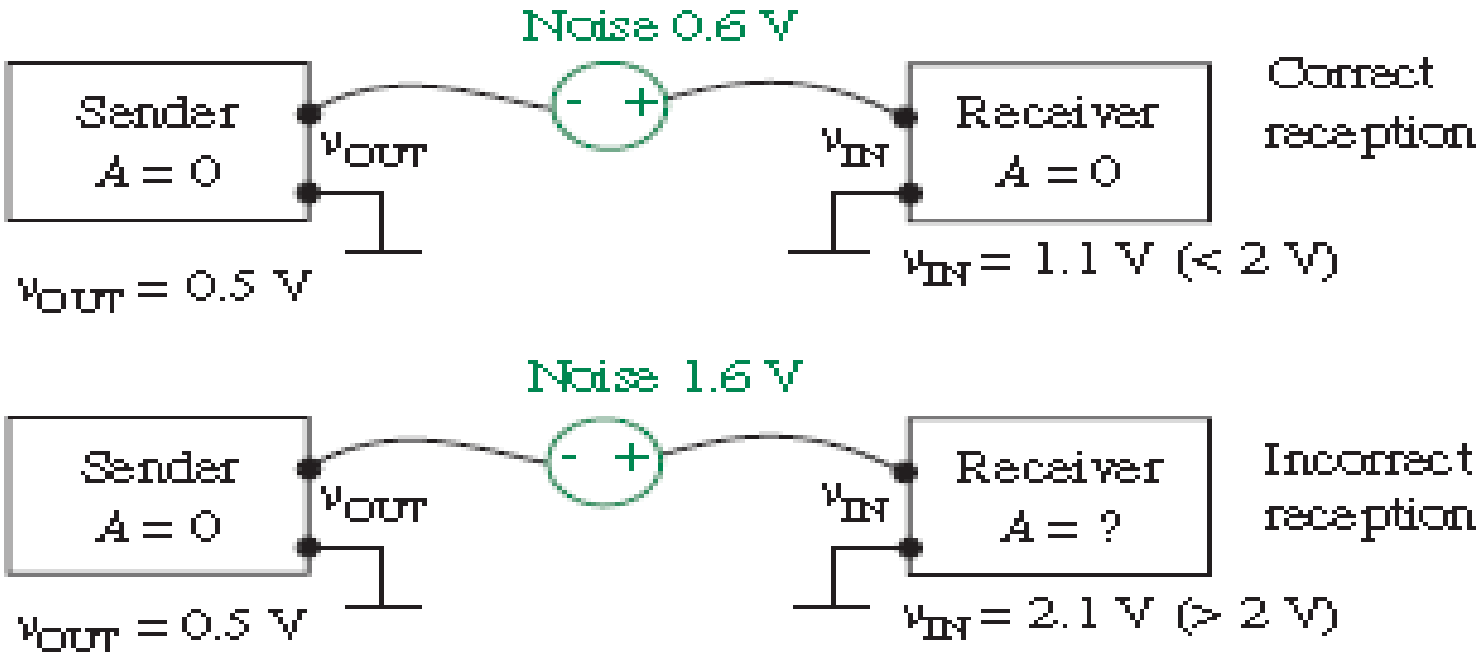
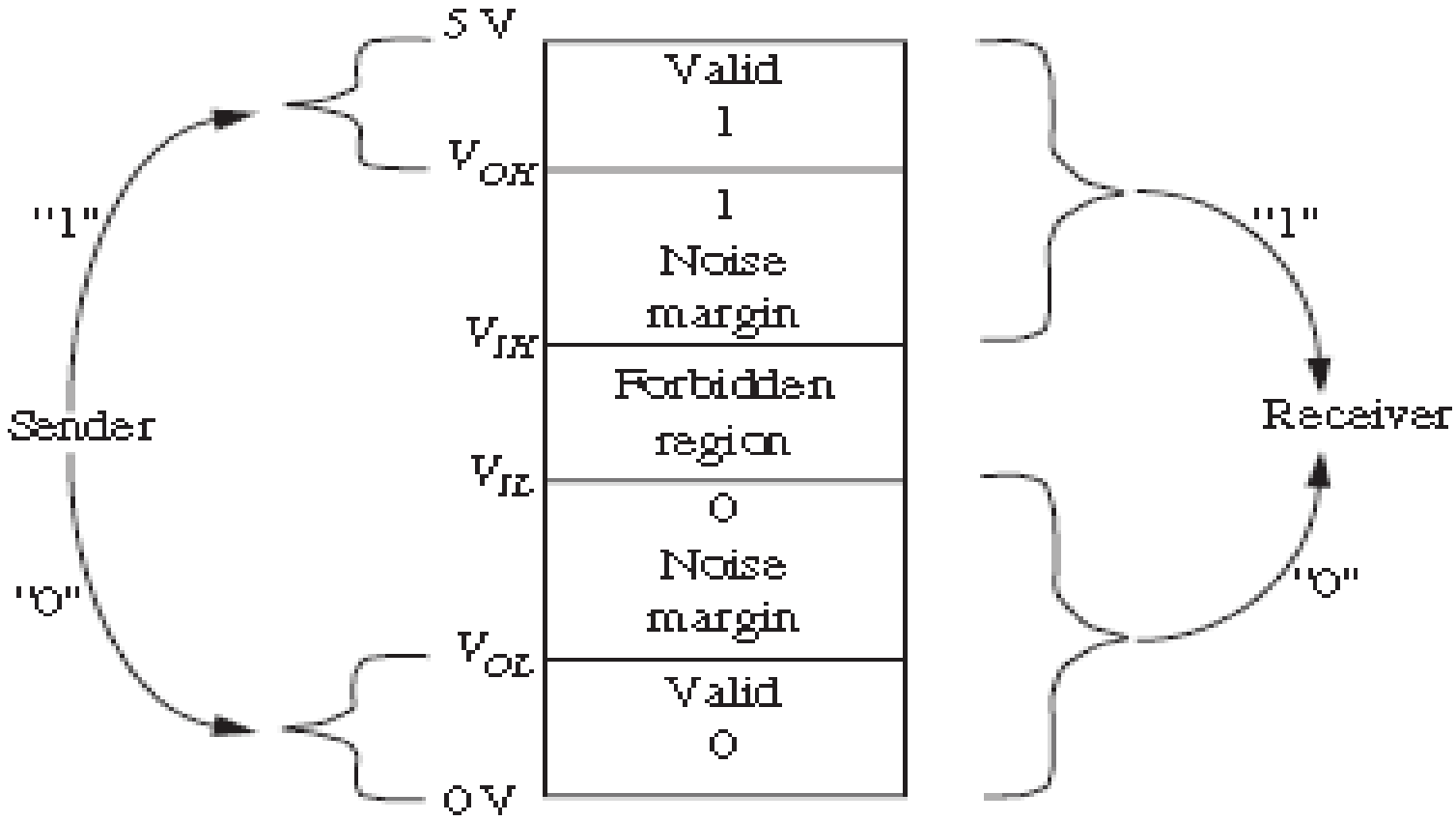


FIGURE Noise margins and signal transmission.

The tighter bounds on the voltage values for a sender compared to those for a receiver result in an asymmetry in input and output voltage thresholds.

This asymmetry is reflected in Figure which shows the correspondence between valid voltage levels and logic signals that is in common use in digital circuits.



To send a logical 0, the sender must produce an *output* voltage value that is less than V_{OL}. Correspondingly, the receiver must interpret *input* voltages below V_{IL} as a logical 0.

Similarly, to send a logical 1, the sender must produce an *output* voltage value that is greater than V_{OH}. Further, the receiver must interpret voltages above V_{IH} as a logical 1.

Quick Quiz (Poll 1)

Noise Margin is:

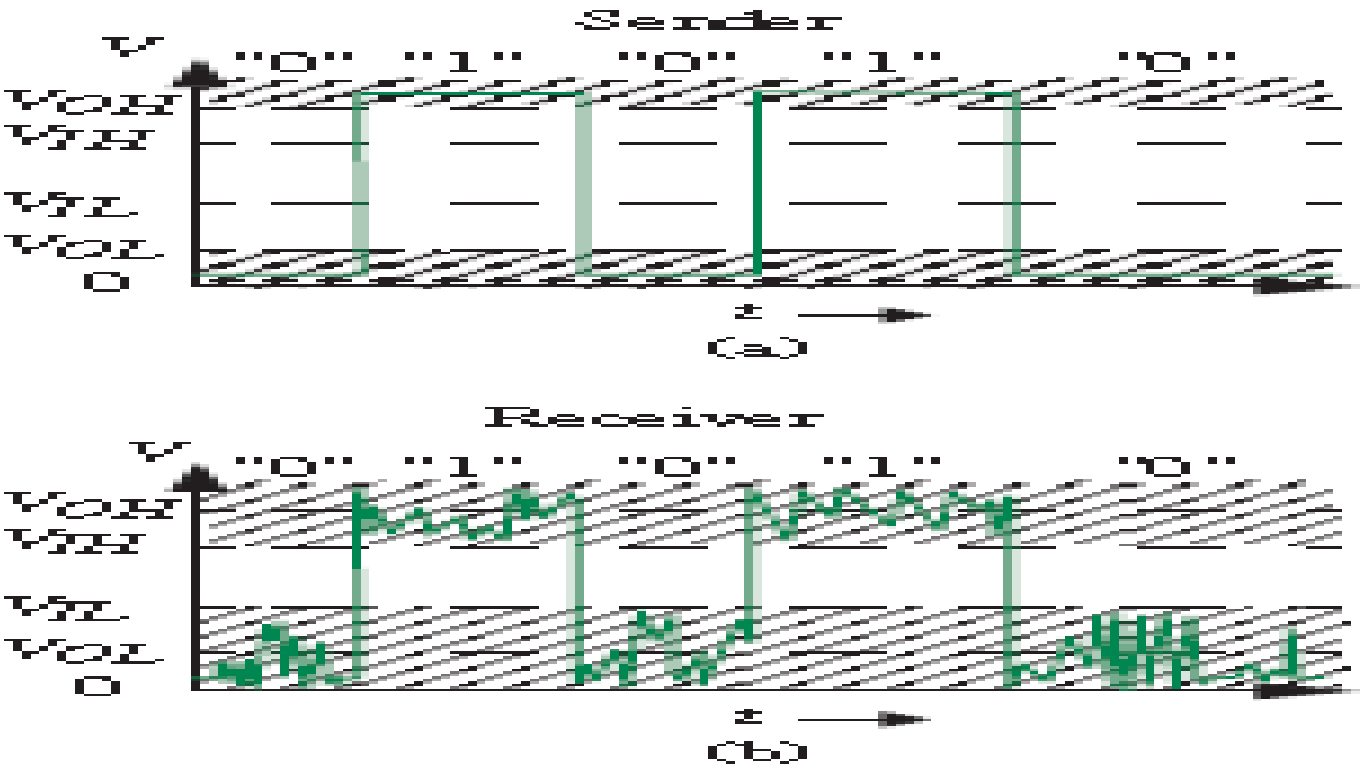
a) Amount of noise the logic circuit can withstand
b) Difference between VOH and VIH
c) Difference between VIL and VOL
d) All of the Mentioned

To allow for a reasonable noise margin, V_{OH} must greater than $V_{IH.}$. We can define both a noise margin for transmitting logical 1's and for transmitting logical 0's.

Noise Margin: The absolute value of the difference between the prescribed output voltage for a given logical value and the corresponding forbidden region voltage threshold for the receiver is called the *noise margin* for that logical value.

Figure a illustrates a scenario in which a sender outputs a 01010 sequence by producing the appropriate output voltage levels (between V_{OH} and 5 V for a logical 1, and between 0 V and V_{OL} for a logical 0).

Provided that the noise does not exceed the noise margins (voltages for a logical 0 do not exceed V_{IL} and voltages for a logical 1 do not fall below V_{IH}), a receiver is able to correctly interpret the signal as illustrated in Figure b.



As illustrated in Figure, the *noise margin for a logical 0* is given by

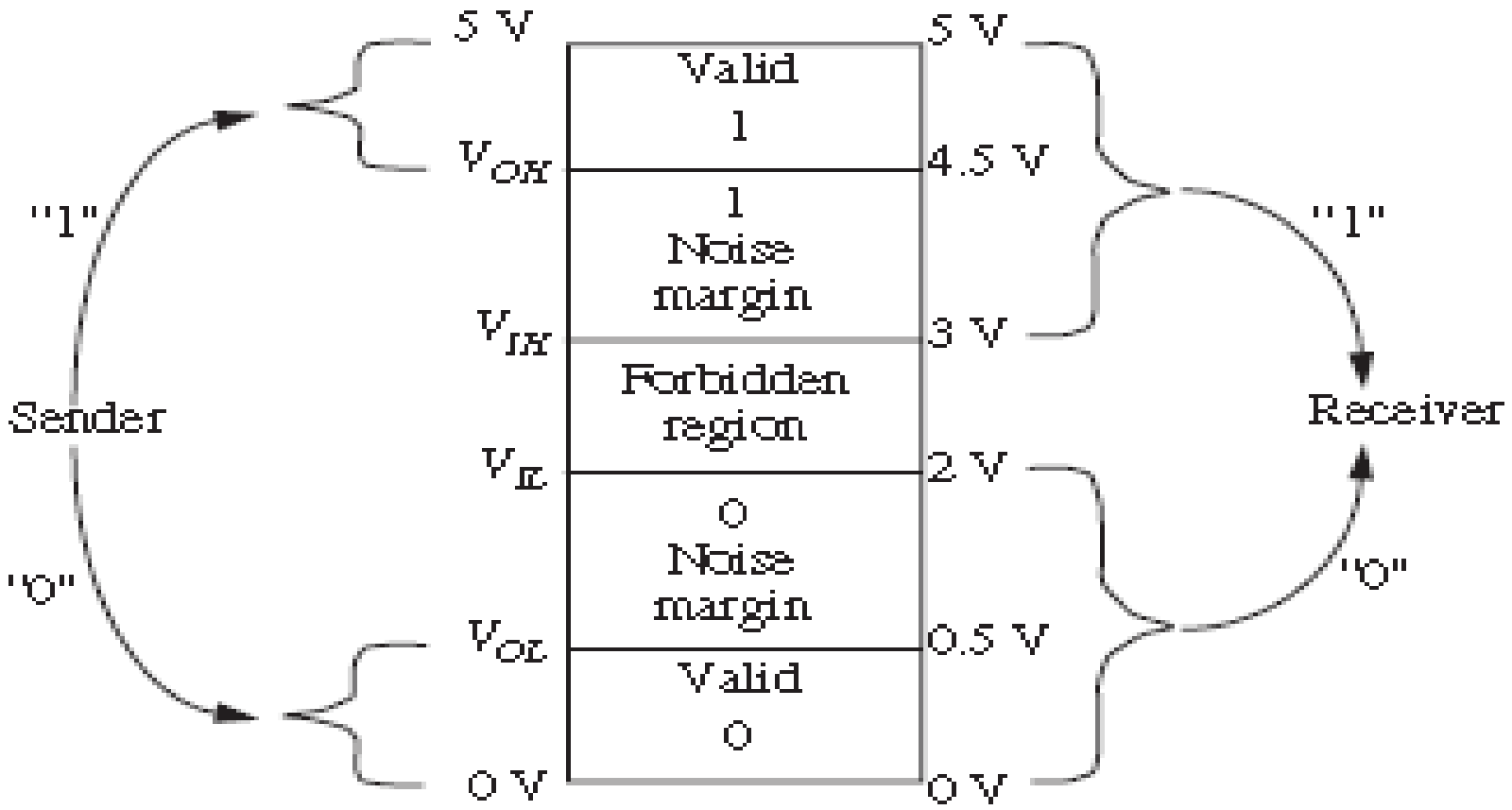
$$\mathrm{NM_0} = V_{IL} - V_{OL}$$

and the *noise margin for a logical 1* is given by

$$\mathrm{NM_1} = V_{OH} - V_{IH}.$$

The region between V_{IL} and V_{IH} is the forbidden region.

Relating the threshold voltage parameters to the numbers used in our example, V_{OH} corresponds to 4.5 V, V_{OL} corresponds to 0.5 V, V_{IH} corresponds to 3 V, and V_{IL} corresponds to 2 V. This mapping is illustrated in Figure .



Quick Quiz (Poll 2)

The noise immunity _____ with noise margin.

a) Decreases
b) Increases
c) Constant
d) None of the Mentioned

Static discipline The *static discipline* is a specification for digital devices. The static discipline requires devices to interpret correctly voltages that fall within the input thresholds (V_{IL} and V_{IH}). As long as valid inputs are provided to the devices, the discipline also requires the devices to produce valid output voltages that satisfy the output thresholds (V_{OL} and V_{OH}).

When designing logic devices, we are often interested in maximizing the noise margins to achieve maximum noise immunity. Referring to Figure 9.8, the 0 noise margin, NM0 = $V_{IL} - V_{OL}$, can be maximized by maximizing V_{IL} and minimizing V_{OL}. Similarly, the 1 noise margin, NM1 = $V_{OH} - V_{IH}$, can be maximized by maximizing V_{OH} and minimizing V_{IH}.

Quick Quiz (Poll 3)

The Lower Noise Margin is given by:

a) VOL – VIL
b) VIL – VOL
c) VIL ~ VOL(Difference between VIL and VOL, depends on which one is greater)
d) All of the Mentioned

Quick Quiz (Poll 4)

The Higher Noise Margin is given by:

a) VOH – VIH
b) VIH – VOH
c) VIH ~ VOH(Difference between VIH and VOH, depends on which one is greater)
d) All of the mentioned

Quick Quiz (Poll 5)

Input Voltage between VIL and VOL is considered as:

a) Logic Input 1
b) Logic Input 0
c) Uncertain
d) None of the mentioned