

UNIT-III

Introduction to Combinational Logic Circuits

Lecture 17

Prepared By:

Dr.Krishan Arora

Assistant Professor and Head

What is Adder?

- Adder : In electronics an adder is digital circuit that perform addition of numbers. In modern computer adder reside in the arithmetic logic unit (ALU).

Adders

Adders are important not only in the computer but also in many types of digital systems in which the numeric data are processed.

Types of adder:

Half adder

Full adder

Half adder

- The half adder accepts two binary digits on its inputs and produce two binary digits outputs, a sum bit and a carry bit.
- The half adder is an example of a simple, functional digital circuit built from two logic gates. The half adder adds two one-bit binary numbers x and y . The output is the sum of the two bits (S) and the carry (C).

The truth table for the half adder is listed below:

Table 4-3
Half Adder

| <i>x</i> | <i>y</i> | <i>C</i> | <i>S</i> |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

S: Sum
C: Carry

$$S = x'y + xy'$$

$$C = xy$$

K-map for half adder

| A \ B | 0 | 1 |
|-------|---|---|
| 0 | 0 | 1 |
| 1 | 2 | 1 |

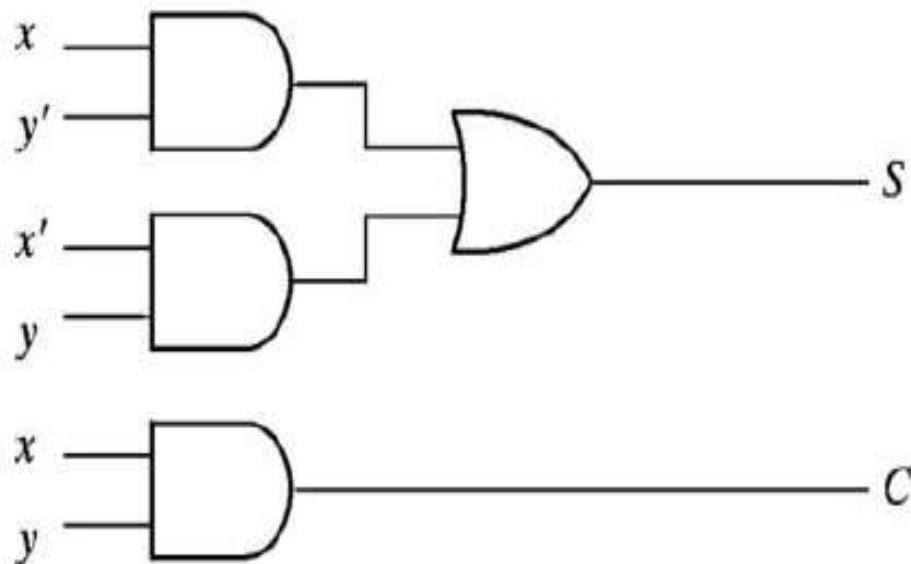
K-map for Carry

| A \ B | 0 | 1 |
|-------|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 2 |

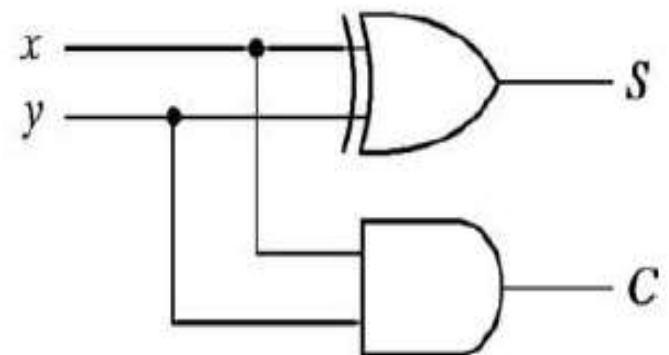
K-map for Sum

Carry $C = AB$ and Sum $C = A\bar{B} + \bar{A}B$.

Implementation of Half-Adder



$$\begin{aligned} \text{(a) } S &= xy' + x'y \\ C &= xy \end{aligned}$$



$$\begin{aligned} \text{(b) } S &= x \oplus y \\ C &= xy \end{aligned}$$



Full-Adder

- One that performs the addition of three bits (two significant bits and a previous carry) is a **full adder**.

Table 4-4
Full Adder

| <i>x</i> | <i>y</i> | <i>z</i> | <i>C</i> | <i>S</i> |
|----------|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Full Adder

- A combinational circuit that adds 3 input bits to generate a Sum bit and a Carry bit

| X | Y | Z | C | S |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Sum

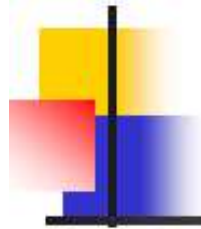
| X \ YZ | 00 | 01 | 11 | 10 |
|--------|----|----|----|----|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

$$\begin{aligned}
 S &= X'Y'Z + X'YZ' \\
 &\quad + XY'Z' + XYZ \\
 &= X \oplus Y \oplus Z
 \end{aligned}$$

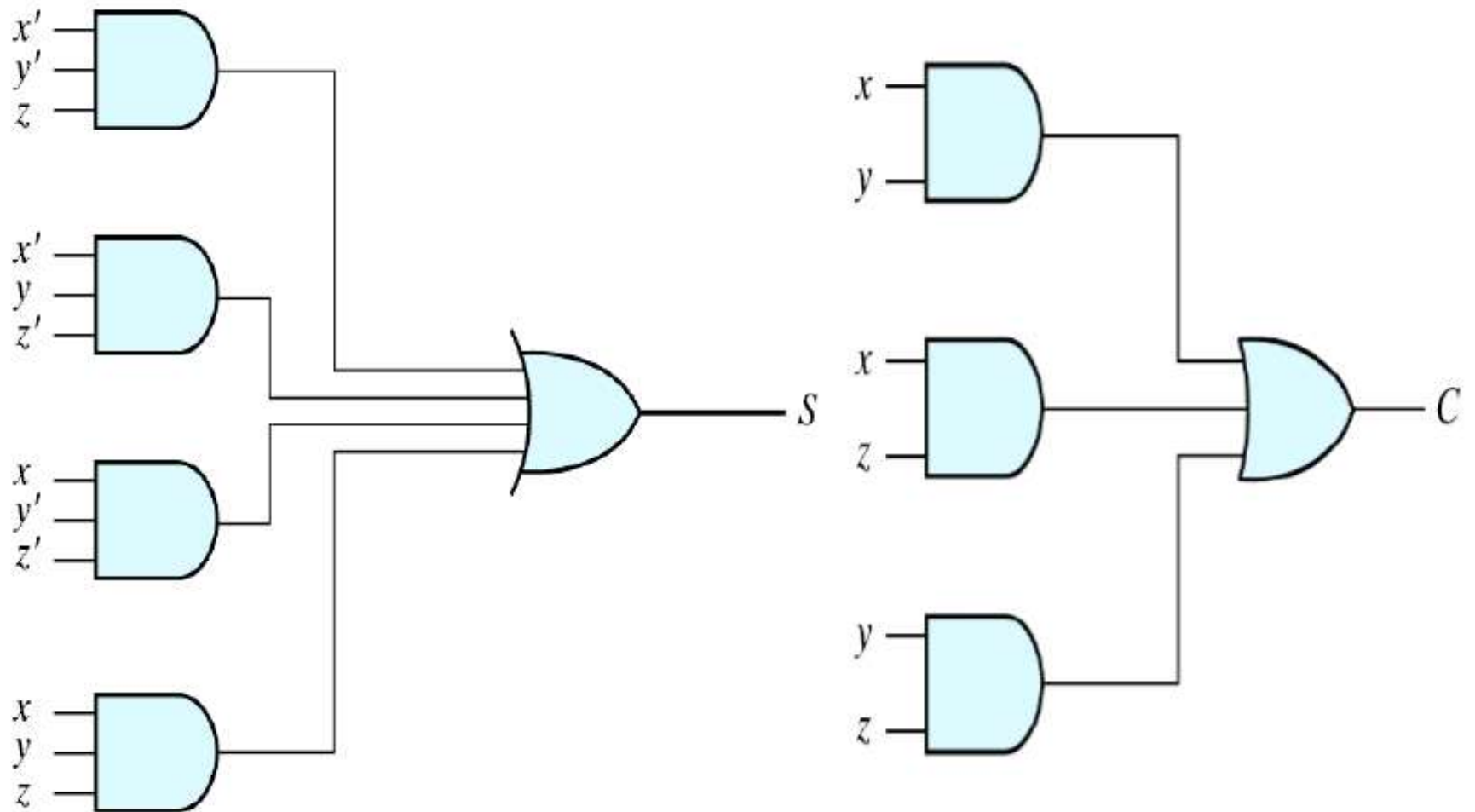
Carry

| X \ YZ | 00 | 01 | 11 | 10 |
|--------|----|----|----|----|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

$$C = XY + YZ + XZ$$



Logic Diagram of Full Adder

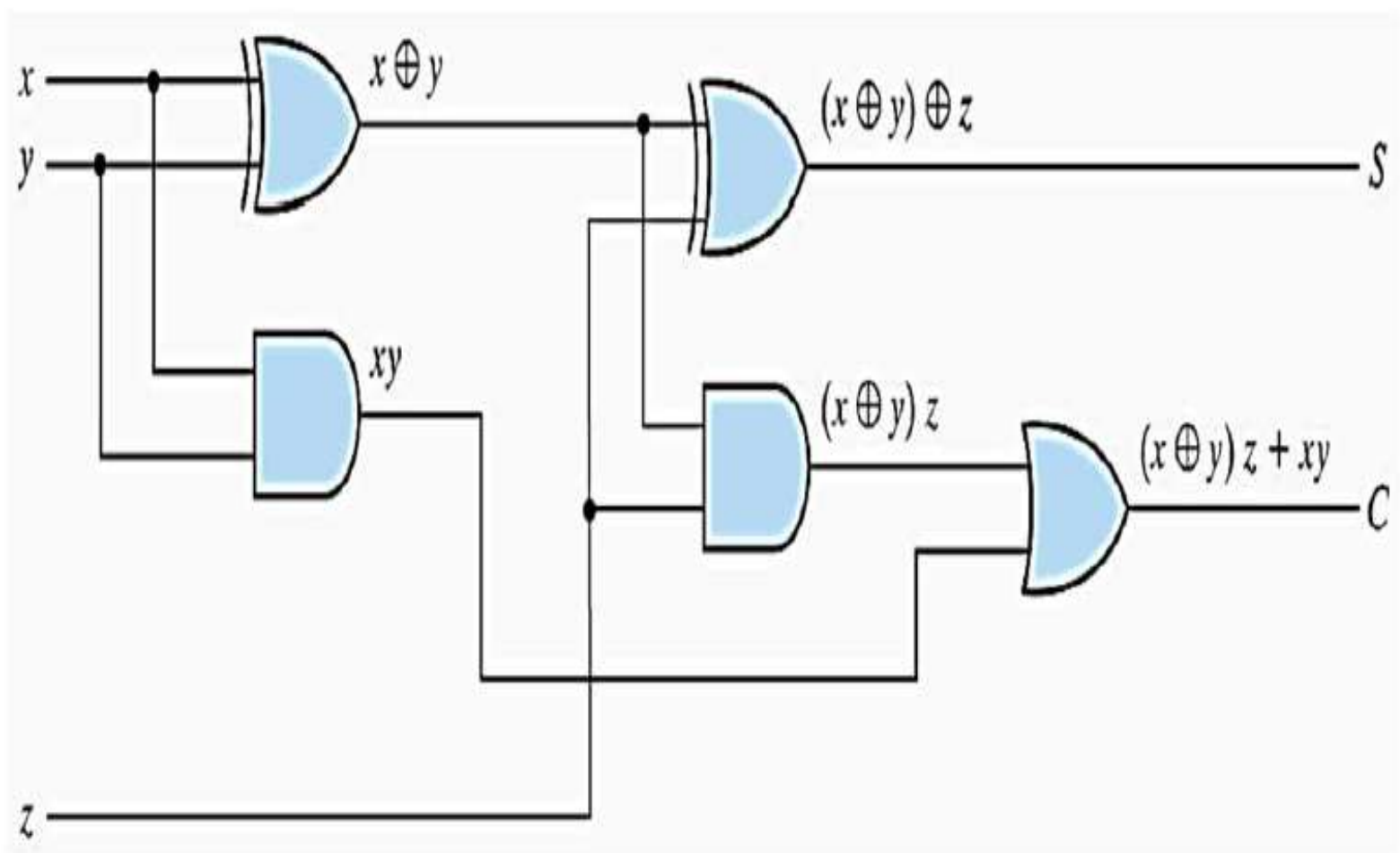




Logic Diagram of Full Adder

$$\begin{aligned} S &= \Sigma m(1,2,4,7) \\ &= X' Y' C_{in} + X' Y C_{in}' + X Y' C_{in}' + X Y C_{in} \\ &= X' (Y' C_{in} + Y C_{in}') + X (Y' C_{in}' + Y C_{in}) \\ &= X' (Y \oplus C_{in}) + X (Y \oplus C_{in})' \\ &= X \oplus Y \oplus C_{in} \end{aligned}$$

$$\begin{aligned} C_{out} &= \Sigma m(3,5,6,7) \\ &= X' Y C_{in} + X Y' C_{in} + X Y C_{in}' + X Y C_{in} \\ &= (X' Y + X Y') C_{in} + XY(C_{in}' + C_{in}) \\ &= (X \oplus Y) C_{in} + XY \end{aligned}$$



What is the difference between half adder and a full adder circuit?

The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. When a full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

The output carry is designated as COUT and the normal output is designated as S.

Quick Quiz (Poll 1)

- Total number of inputs in a half adder is

a) 2

b) 3

c) 4

d) 1

Quick Quiz (Poll 2)

- In which operation carry is obtained?
 - a) Subtraction
 - b) Addition
 - c) Multiplication
 - d) Both addition and subtraction

Quick Quiz (Poll 3)

- If A and B are the inputs of a half adder, the sum is given by _____
 - a) A AND B
 - b) A OR B
 - c) A XOR B
 - d) A EX-NOR B

Quick Quiz (Poll 4)

- The difference between half adder and full adder is _____
 - a) Half adder has two inputs while full adder has four inputs
 - b) Half adder has one output while full adder has two outputs
 - c) Half adder has two inputs while full adder has three inputs
 - d) All of the Mentioned