

Unit V

Synchronous Counters

by

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Design of a Synchronous Mod-6 Counter using Clocked SR Flip-Flop

[illegible]

For S_A

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0	0	1	0
1	X	0	X	X

$$S_A = Q_B Q_C$$

For R_A

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X	X	0	X
1	0	1	X	X

$$R_A = \overline{Q}_B Q_C$$

For S_B

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0	1	X	0
1	0	0	X	X

$$S_B = \overline{Q}_A Q_C$$

For R_B

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X	0	1	0
1	X	X	X	X

$$R_B = Q_B Q_C$$

For S_C

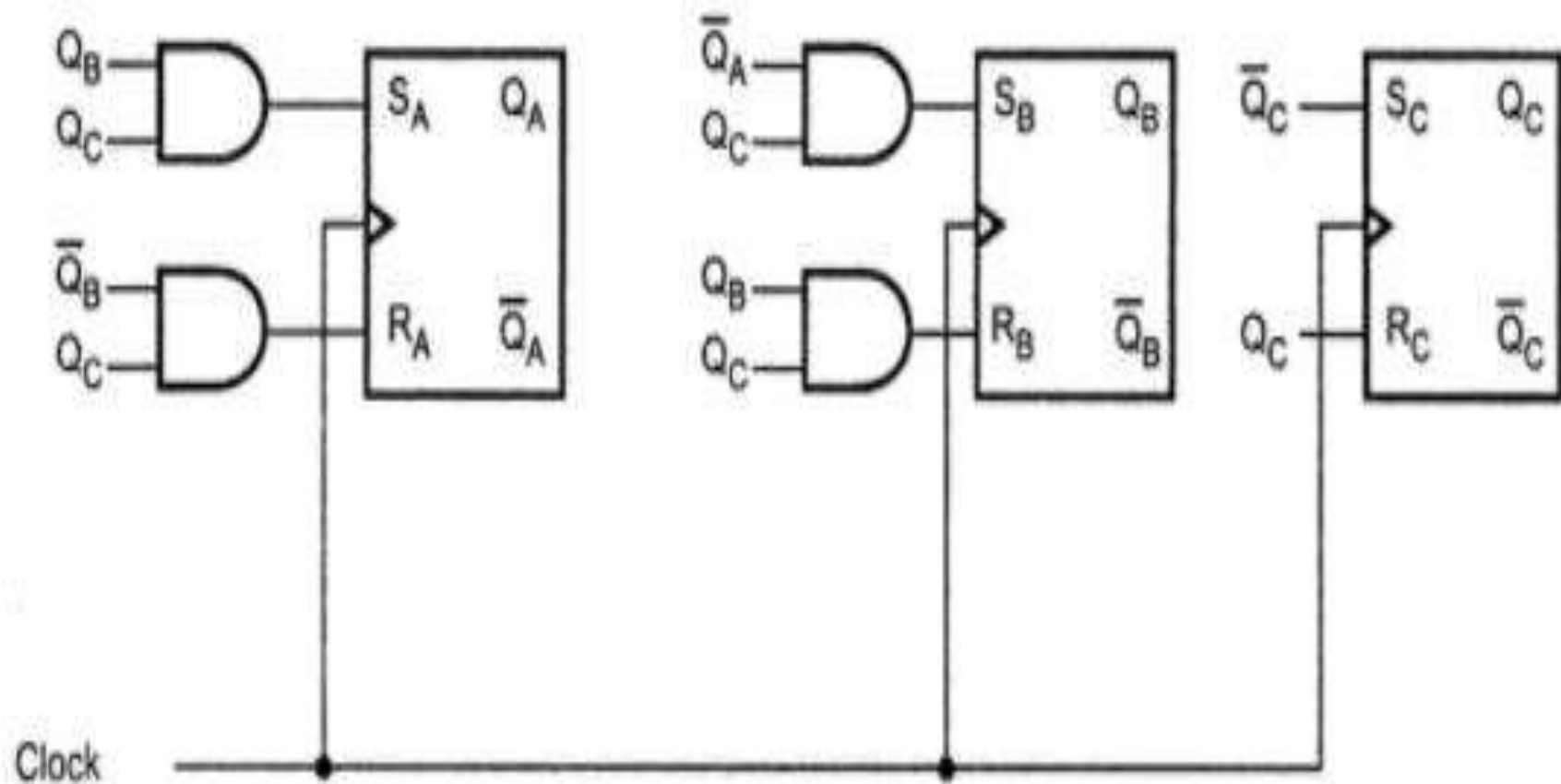
$Q_A \backslash Q_B Q_C$	00	01	11	10
0	1	0	0	1
1	1	0	X	X

$$S_C = \overline{Q}_C$$

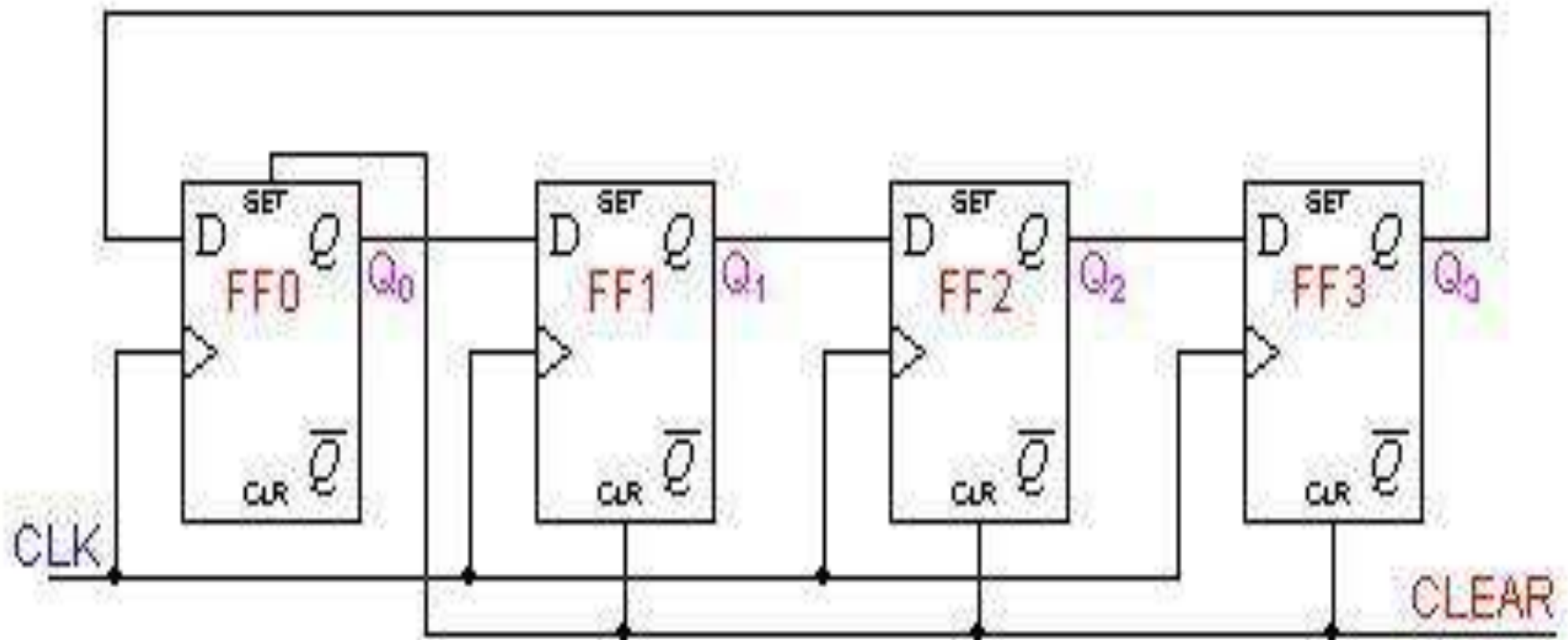
For R_C

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	0	1	1	0
1	0	1	X	X

$$R_C = Q_C$$



4- bit Ring Counter



Ring Counter

- **Operation of Ring Counter**
- Initially, all the flip flops in ring counter are reset to 0 by applying CLEAR signal. Before applying the clock pulse, we apply the PRESET pulse to the flip flops which assigns the value '1' to the ring counter circuit. For each clock signal, the data circulates among all the 4 flip flop stages of ring counter.
- This 4 staged ring counter is called Mod 4 ring counter or 4 bit ring counter. To circulate the data correctly in the ring counter, we must load the counter with required values like all 0's or all 1's.

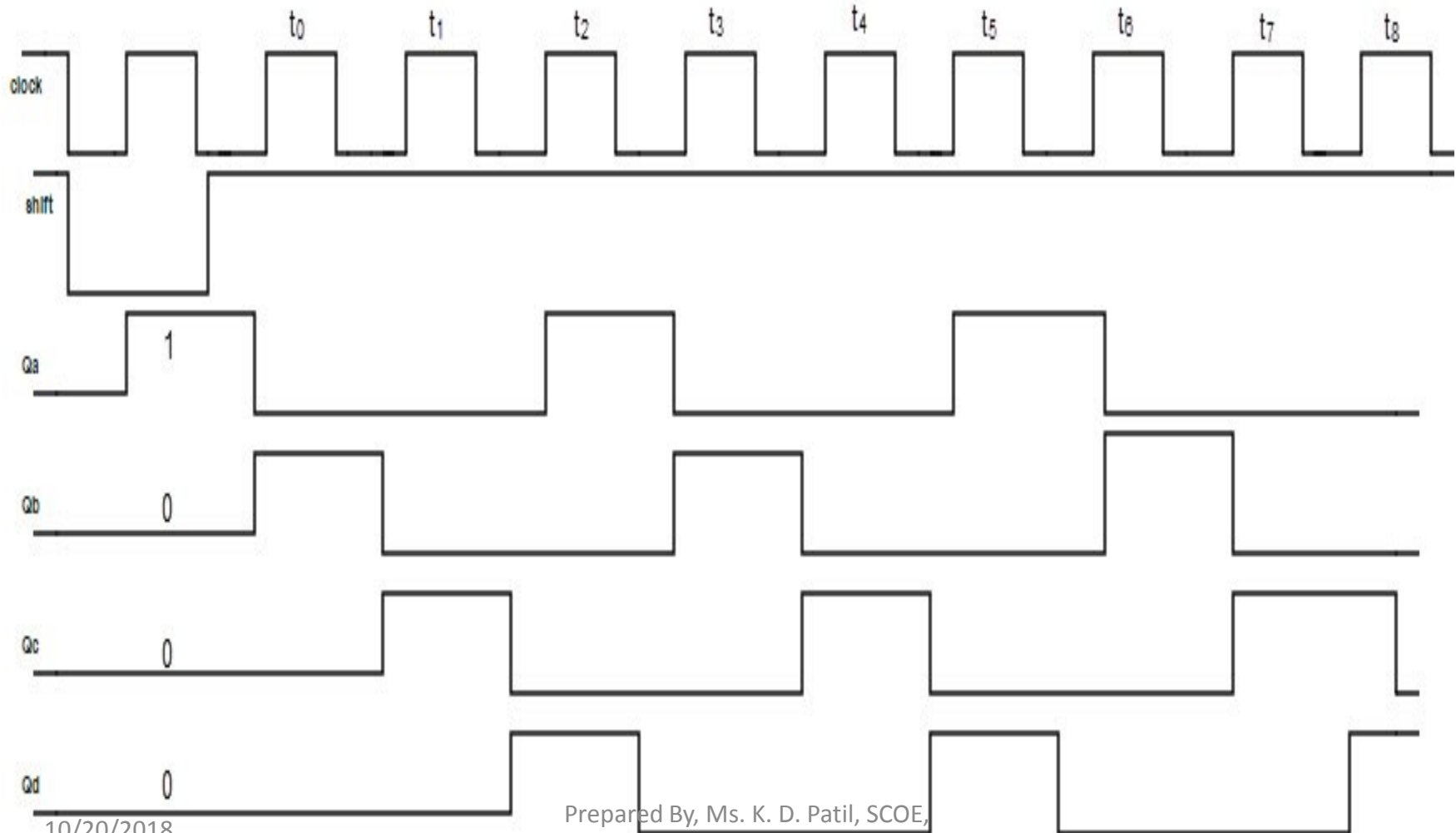
Ring Counter

- Truth table of ring counter

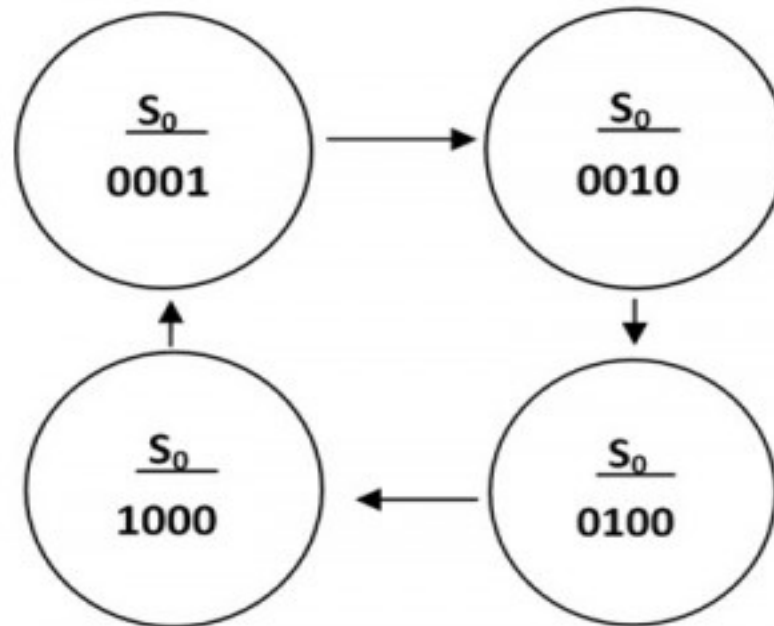
Q_0	Q_1	Q_2	Q_3
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

- When CLEAR input CLR = 0, then all flip flops are set to 1. When CLEAR input CLR = 1, the ring counter starts its operation. For one clock signal, the counter starts its operation. On next clock signal, the counter again resets to 0000. Ring counter has 4 sequences: 0001, 0010, 0100, 1000, 0000.

Ring Counter



- **State diagram of ring counter**



- It denotes that the position of the preset digit (in this case preset digit is 1) is changing its position from LSB to MSB, for one clock signal.

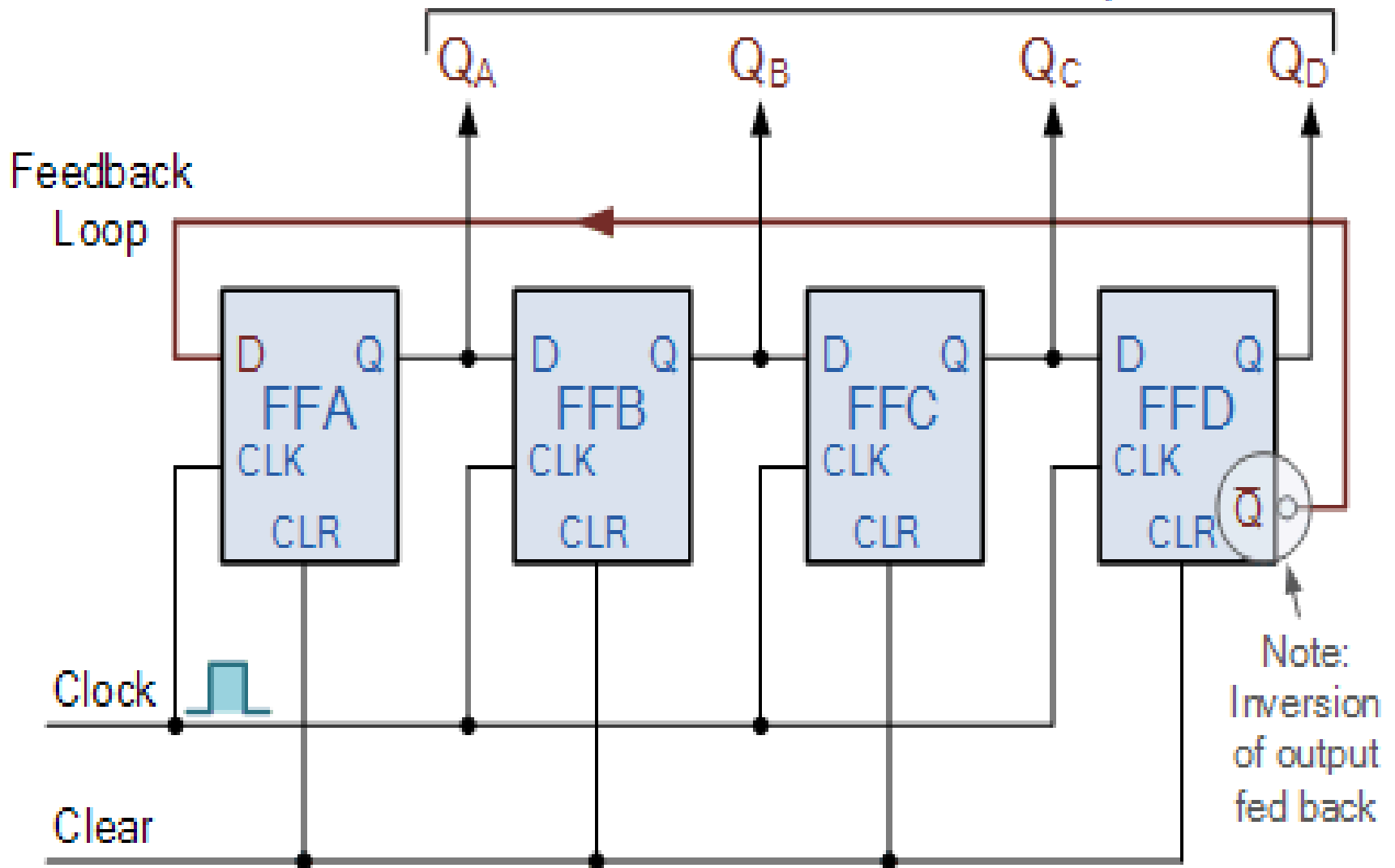
Ring Counter

- **Advantages**
- Can be implemented using D and JK flip-flops.
- It is a self-decoding circuit. It doesn't need a decoder
- **Disadvantages**
- Only four of the 15 states are being utilized.

Johnson/Twisted Ring Counter

- The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as $2n$ bit Johnson counter or Mod $2n$ Johnson counter.
- This is an advantage of the Johnson counter that it requires only half number of flip flops that of a ring counter uses, to design the same Mod.
- The main difference between the 4 bit ring counter and the Johnson counter is that, in ring counter, we connect the output of last flip flop directly to the input of first flip flop. But in Johnson counter, we connect the inverted output of last stage to the first stage input.
- The Johnson counter is also known as Twisted Ring Counter, with a feedback. In Johnson counter the input of the first flip flop is connected from the inverted output of the last flip flop.
- The Johnson counter or switch trail ring counter is designed in such a way that it overcomes the limitations of ring counter. Mainly it reduces the number of flip flops required for designing the circuit.

4-bit Parallel Data Output

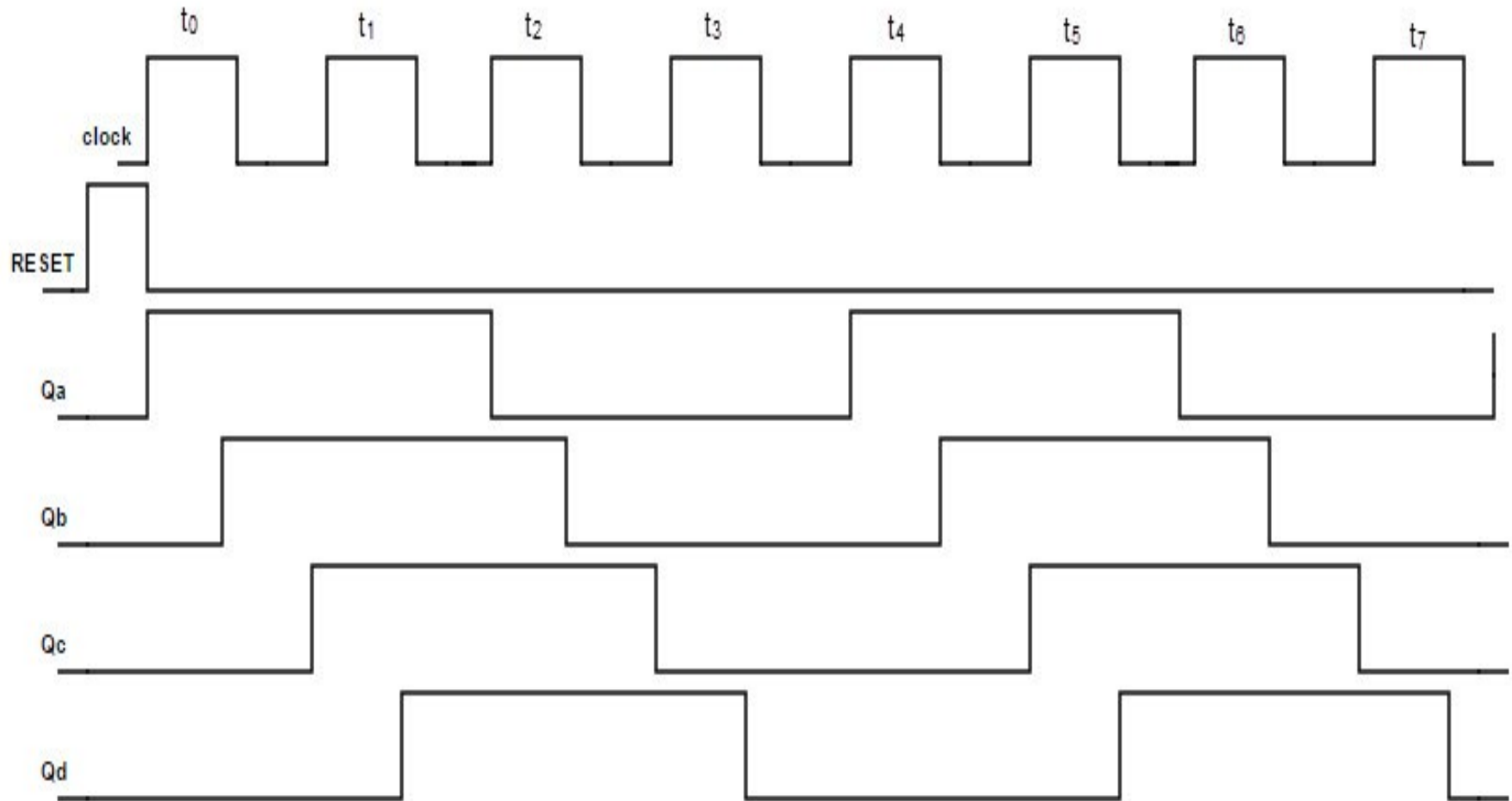


- **Operation of johnson counter**
- The Johnson counter designed with D flip flop is shown in figure. It has four stages i.e. four flip flops connected in series type or cascaded. Initially zero / Null is fed to the Johnson counter and on applying the clock signal, outputs will change to “1000”, “1100”, “1110”, “1111”, “0111”, “0011”, “0001”, “0000” in a sequence and the sequence will repeat for next clock signal.
- The Johnson counter produces a special pattern by passing four 0's and then four 1's and thus it produces a special pattern by counting up down.

Truth table of johnson counter

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			

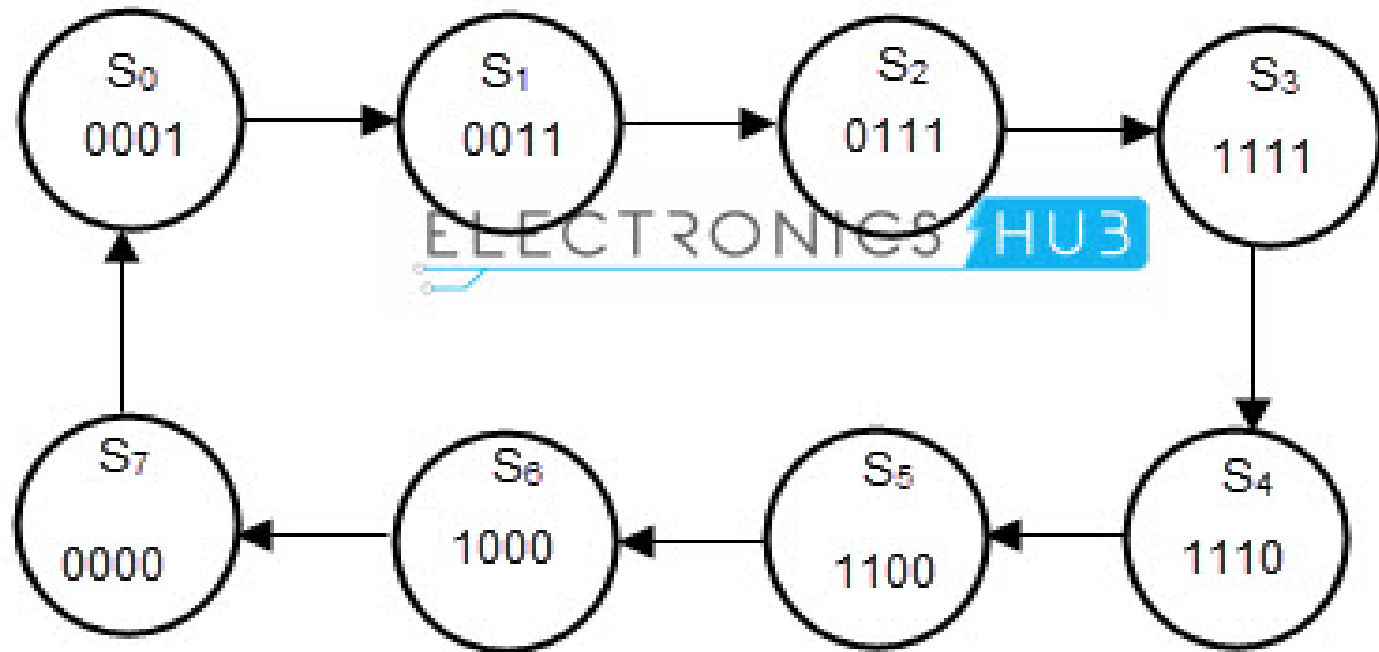
Timing Diagram of Johnson Ring Counter



State Diagram

- The timing diagram of the johnson counter will explain that the clock signal changes the output of every stage of the counter, so that CLK signal will help the data to circulate from one flip flop to another.
- The state diagram indicates that how the data transfers from one flip flop to another for every clock pulse. The 4 stage Johnson ring counters are used as frequency dividers, by varying their feedback connections. So they can be used as frequency divider circuits also.

State Diagram



Johnson/Twisted Ring Counter

- When $CLR = 0$, all outputs and inputs of flip flops are preset to 0 (cleared) except the data input of right most FF which sets to 1.
- When $CLR = 1$, Johnson counter starts its operation. On every clock edge, the output of last flip flop (1) shifts left to the third flip flop. As the first flip flop is connected to serial input i.e. 1, the input of third flip flop is 1.
- In next cycle, $QA = 0$ so 0 rotates in ring form in second half cycle. Johnson counter has 8 sequences: 0001, 0011, 0111, 1111, 1110, 1100, 1000, and 0000.

Johnson/Twisted Ring Counter

- **Advantages**
- More outputs as compared to ring counter.
- It has same number of flip flop but it can count twice the number of states the ring counter can count.
- It count the data in a continuous loop
- It only needs half the number of flip-flops compared to the standard ring counter for the same MOD
- **Disadvantages**
- Only 8 of the 15 states are being used.
- It doesn't count in a binary sequence.

Applications of Ring counters

- Ring counters are used to count the data in a continuous loop.
- They are also used to detect the various numbers values or various patterns within a set of information, by connecting AND & OR logic gates to the ring counter circuits.
- 2 stage, 3 stage and 4 stage ring counters are used in frequency divider circuits as divide by 2 and divide by 3 and divide by 4 circuits, respectively.
- The 3 stage Johnson counter is used as a 3 phase square wave generator which produces 120° phase shift.
- The 5 stage Johnson counter circuit is generally used as synchronous decade (BCD) counter and also as divider circuit.
- The 2 stage Johnson counters are also known as “Quadrature oscillator” which is used to produce 4 level individual outputs which are out of phase with 90° with each other. This quadrature generator is used to produce 4 phase timing signal.