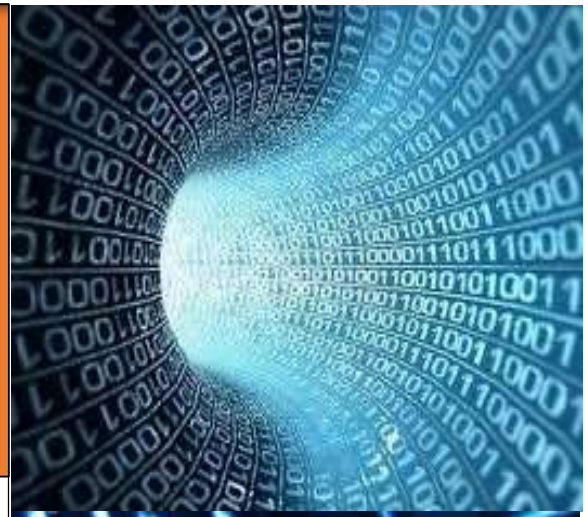
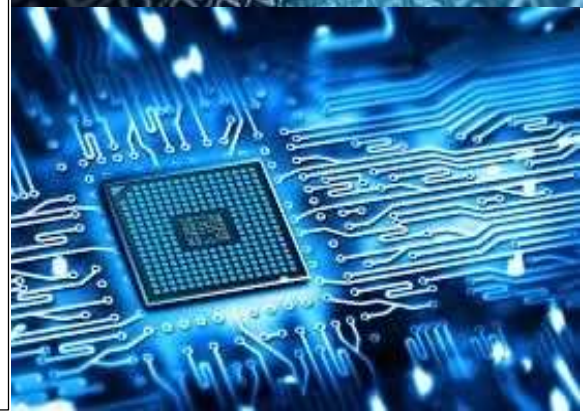
DIGITAL ELECTRONICS: ECE 213

Topic: IC LOGIC FAMILIES

UNIT III: Introduction to Combinational Logic Circuits and Logic Families

Lecture No.: 23





Parity Generator Circuit

Even Parity Generator

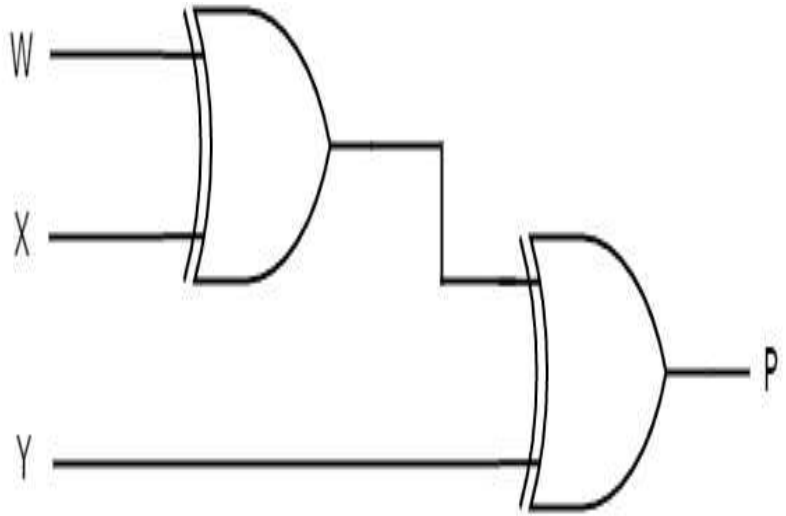
If odd number of ones present in the input, then even parity bit, P should be '1' so that the resultant word contains even number of ones.

Binary Input WXY	Even Parity bit P
000	0
001	1
010	1
011	0
100	1
101	0
110	0
111	1

$$P = W'X'Y + W'XY' + WX'Y' + WXY$$

$$\Rightarrow P = W'(X'Y + XY') + W(X'Y' + XY)$$

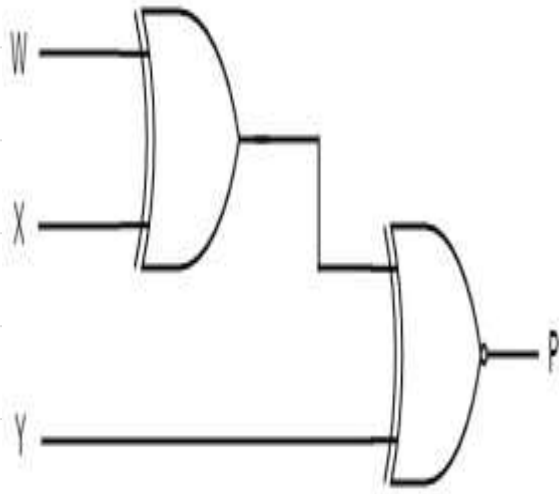
$$\Rightarrow P = W'(X \oplus Y) + W(X \oplus Y)' = W \oplus X \oplus Y$$



Odd Parity Generator

If even number of ones present in the input, then odd parity bit, P should be '1' so that the resultant word contains odd number of ones

Binary Input WXY	Odd Parity bit P
000	1
001	0
010	0
011	1
100	0
101	1
110	1
111	0

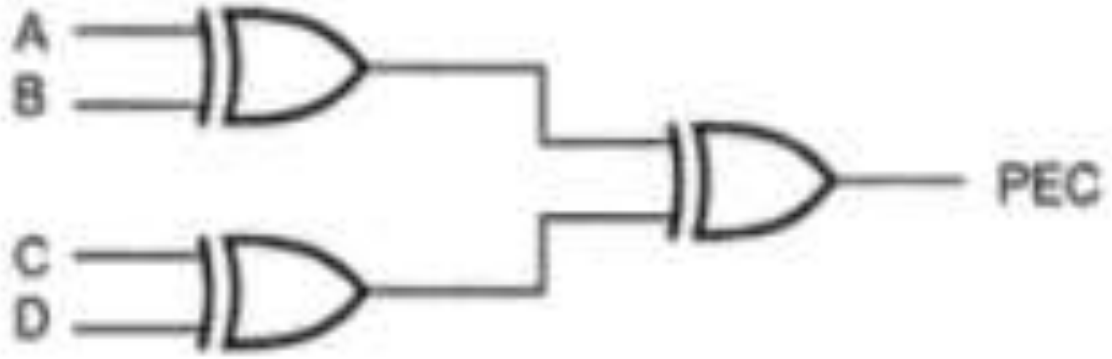


Parity Checker Circuit

Even parity checker checks error in the transmitted data, which contains message bits along with even parity.

Four Bits Received				Parity Error Check
A	B	C	D	PEC
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	1
1	1	1	1	0

$$
\begin{aligned}
PEC &= \bar{A}\bar{B}(\bar{C}D + C\bar{D}) + \bar{A}B(\bar{C}\bar{D} + CD) \\
&\quad + AB(\bar{C}D + C\bar{D}) + A\bar{B}(\bar{C}\bar{D} + CD) \\
&= \bar{A}\bar{B}(C \oplus D) + \bar{A}B(\overline{C \oplus D}) \\
&\quad + AB(C \oplus D) + A\bar{B}(\overline{C \oplus D}) \\
&= (\bar{A}\bar{B} + AB)(C \oplus D) + (\bar{A}B + A\bar{B})(\overline{C \oplus D}) \\
&= (\overline{A \oplus B})(C \oplus D) + (A \oplus B)(\overline{C \oplus D}) \\
&= (A \oplus B) \oplus (C \oplus D)
\end{aligned}
$$



DIGITAL IC LOGIC FAMILIES:

Logic Families

OBSOLETE ONES:

1. Diode Logic.
2. Diode Transistor Logic (DTL).
3. Resistor Transistor Logic (RTL).

CURRENT ONES:

1. TTL (Transistor Transistor Logic)
2. ECL (Emitter Coupled Logic)
3. CMOS (Complementary Metal Oxide Semiconductor)

IC Families

Logic family are digital integrated circuit devices which are constructed with a combination of electronic gates.

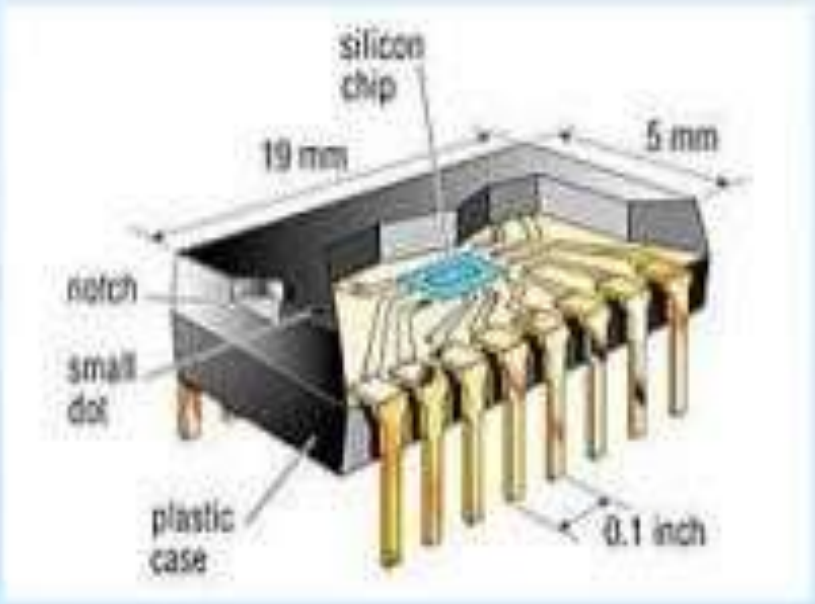
A family has its own power supply voltage and group potential; distinct logic levels.

- Diode Logic (DL) logic is implemented with the use of resistors and diodes.
- Resistor-Transistor Logic (RTL) logic is implemented with the use of transistors and resistors
- Diode-Transistor Logic (DTL) logic is implemented with the use of diodes and transistors.
- Transistor-Transistor Logic (TTL) logic are implemented with transistors
- Emitter Coupled Logic (ECL) logic are implemented with transistors
- Complementary Metal Oxide Semiconductor Logic (CMOS) logic are implemented with MOSFET

Characteristics of an Ideal Logic Family

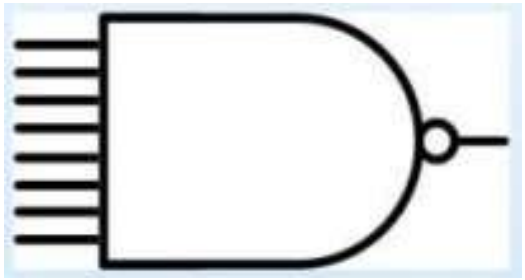
The most important parameters for evaluating and comparing logic families include :

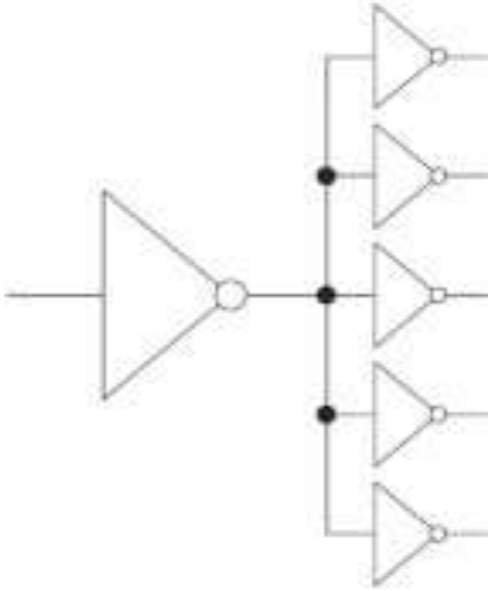
- Logic Levels
- Power Dissipation
- Propagation delay
- Noise margin
- Fan-out (loading)

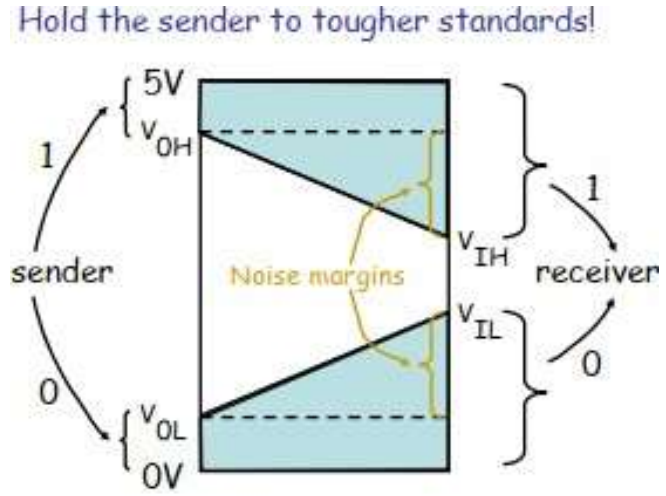


Characteristics of Logic Family

- Fan in : The number of inputs that the gate can handle properly with out disturbing the output level.
- Fan out : The number of inputs that can driven simultaneously by the output with out disturbing the output level.
- Noise immunity : Noise immunity is the ability of the logic circuit to tolerate the noise voltage.







"1" noise margin: $V_{IH} - V_{OH}$

"0" noise margin: $V_{IL} - V_{OL}$

As illustrated in Figure the *noise margin for a logical 0* is given by

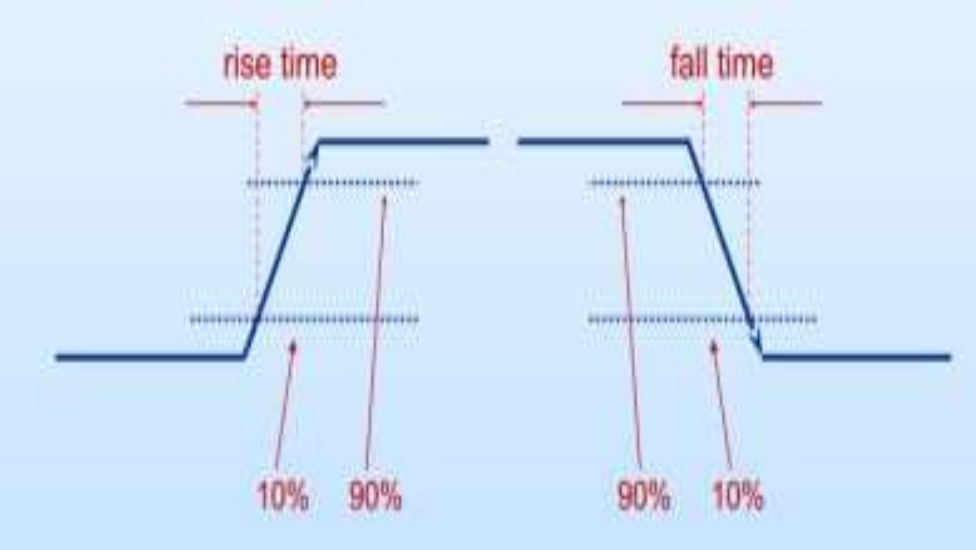
$$NM_0 = V_{IL} - V_{OL}$$

and the *noise margin for a logical 1* is given by

$$NM_1 = V_{OH} - V_{IH}.$$

Characteristics of Logic Family

- Noise Margin : The quantative measure of noise immunity is called noise margin.
- Propagation Delay : The propagation delay of gate is the average transition delay time for the signal to propagate from input to output
- Threshold Voltage : The voltage at which the circuit changes from one state to another state
- Operating Speed : The speed of operation of the logic gate is the time that elapses between giving input and getting output.
- Power Dissipation : The power dissipation is defined as power needed by the logic circuit.



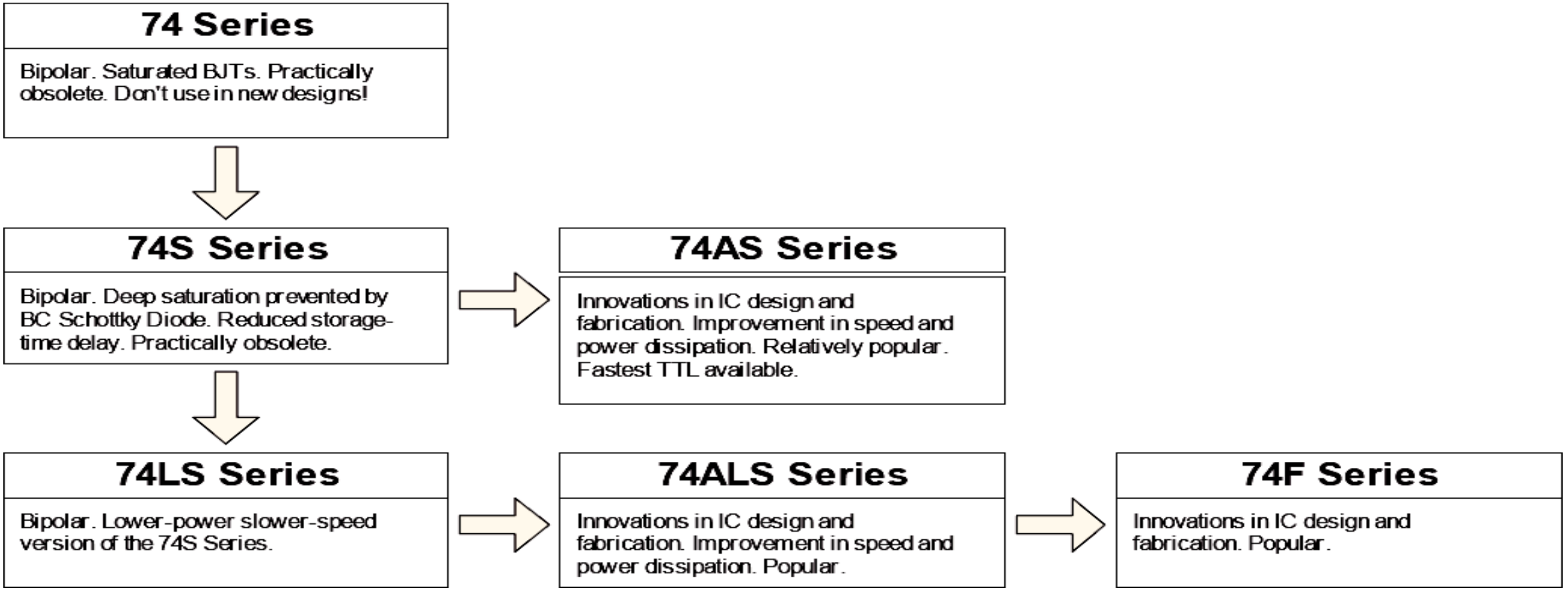
TTL IC Family

- In Transistor-Transistor logic or just TTL, logic gates are built only around transistors
- TTL was developed in 1965
- Through the years basic TTL has been improved to meet performance requirements. There are many versions or families of TTL. For example
  - Standard TTL
  - High Speed TTL (twice as fast, twice as much power)
  - Low Power TTL (1/10 the speed, 1/10 the power of "standard" TTL)
  - Schhottky TTL etc. (for high-frequency uses)

TTL IC Family

- **Transistor-Transistor Logic Families:**
  - 74L — Low power
  - 74H — High speed
  - 74S — Schottky
  - 74LS — Low power Schottky
  - 74AS — Advanced Schottky
  - 74ALS — Advance Low power Schottky

TTL IC Family Evolution



Legacy: don't use in new designs

Widely used today

ECL IC Family

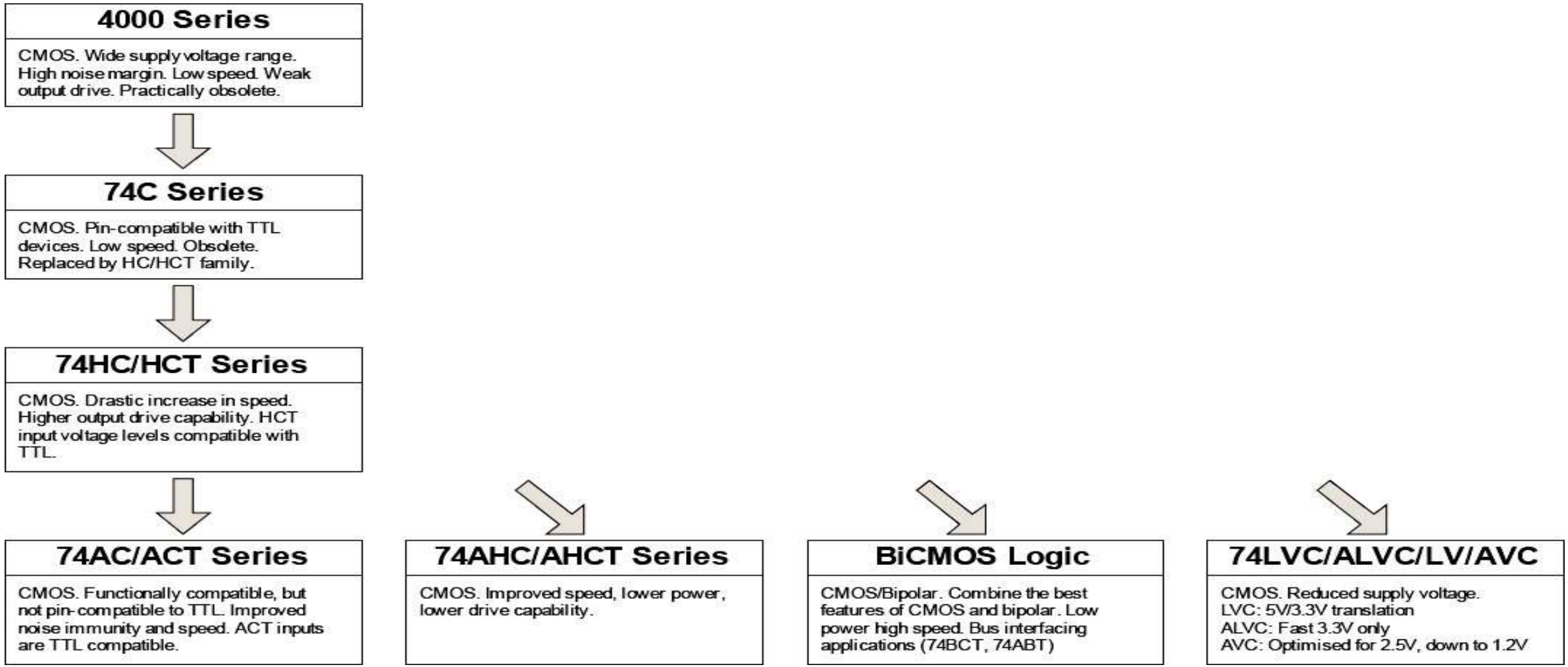
- PROS: Fastest logic family available (~1ns)
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. "0": –1.7V. "1": –0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families

CMOS IC Family

Complementary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output

CMOS Family Evolution



TTL vs CMOS

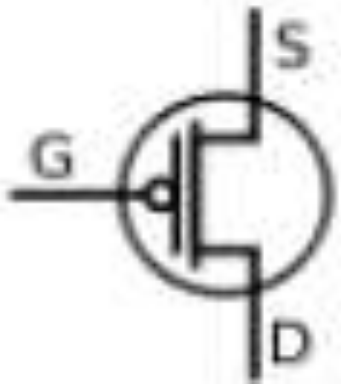
- TTL
  - faster (some versions)
  - strong drive capability
  - rugged
- CMOS
  - lower power consumption
  - simpler to make
  - greater packing density
  - better noise immunity

CMOS as a Switch

PMOS

ON → Gate input Low

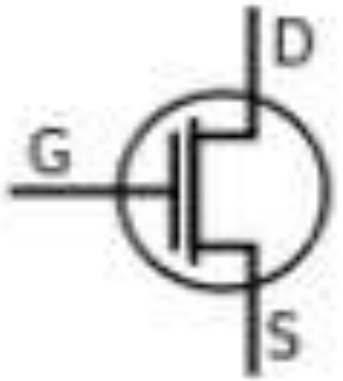
OFF → Gate input High



NMOS

OFF → Gate input Low

ON → Gate input High



Comparison of Logic Families

	TTL	ECL	CMOS
Base Gate	NAND	OR/NOR	NAND/NOR
Fan-in	12-14	>10	>10
Fan-out	10	25	50
Power dissipation (mW)	10	175	0.001
Noise Margin	0.5V	0.16V (lowest)	1.5V (Highest)
Propagation Delay (ns)	10	<3 lowest	15 Highest
Noise immunity	Very good	good	excellent