DIGITAL ELECTRONICS

Counters(Asynchronous & synchronous)

Counters

- Introduction: Counters
- Asynchronous (Ripple) Counters
- Asynchronous UP/ Down Counters

Introduction: Counters

- Counters are circuits that cycle through a specified number of states.
- Two types of counters:
  - synchronous (parallel) counters
  - asynchronous (ripple) counters
- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Synchronous counters apply the same clock to all flip-flops.

Difference

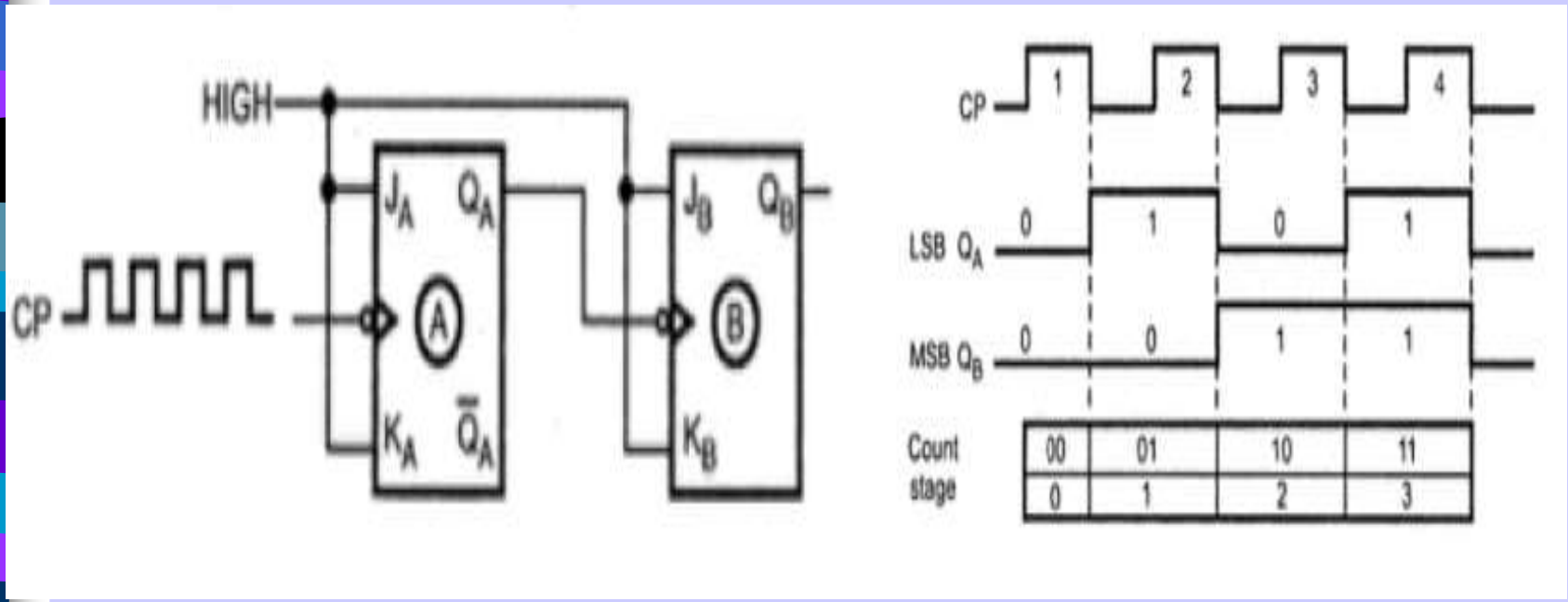
Sr. No.	Asynchronous Counters	Synchronous Counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

Asynchronous (Ripple) Counters

- Asynchronous counters: the flip-flops do not change states at exactly the same time as they do not have a common clock pulse.
- Also known as ripple counters, as the input clock pulse “ripples” through the counter – cumulative delay is a drawback.
- *n* flip-flops $\rightarrow$ a MOD (modulus) 2^n counter. (Note: A MOD-*x* counter cycles through *x* states.)
- Output of the last flip-flop (MSB) divides the input clock frequency by the MOD number of the counter, hence a counter is also a *frequency divider*.

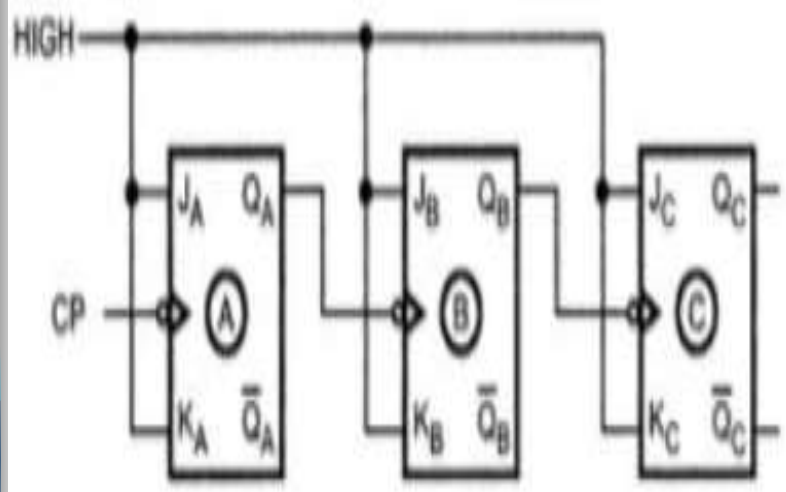
Asynchronous (Ripple) Counters

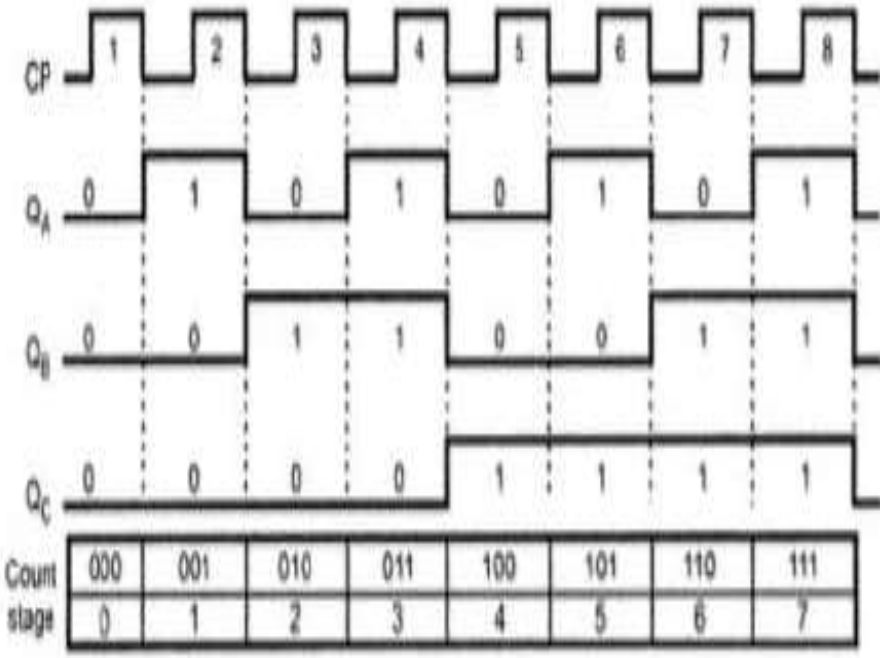
- Example: 2-bit ripple binary counter.
- Output of one flip-flop is connected to the clock input of the next more-significant flip-flop.



Asynchronous (Ripple) Counters

- Example: 3-bit ripple binary counter.

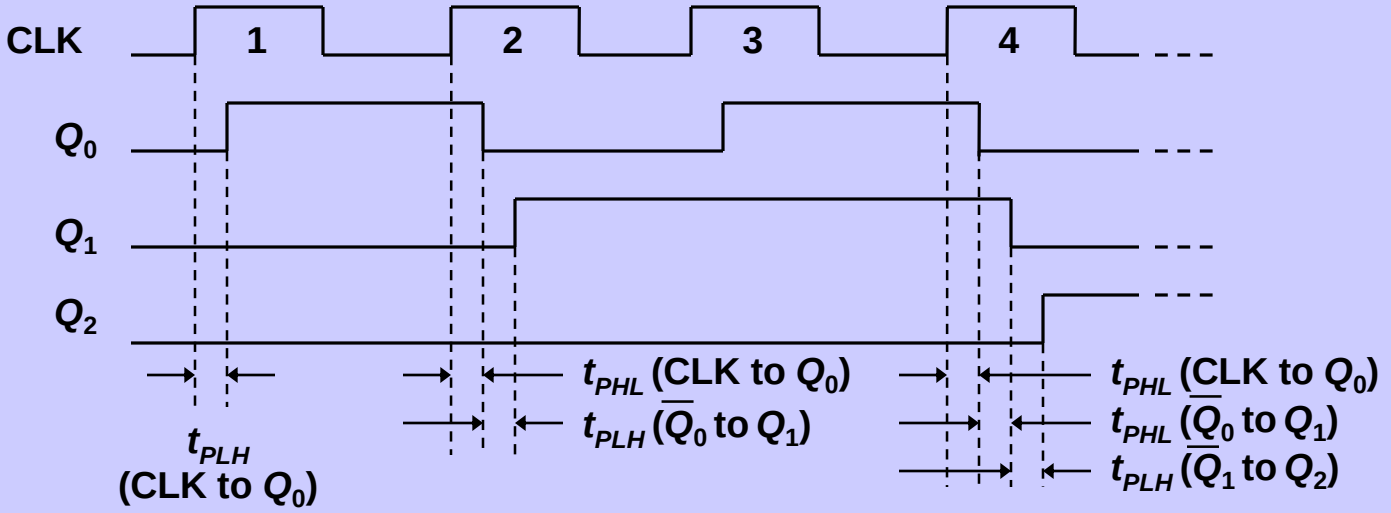




Count	000	001	010	011	100	101	110	111
stage	0	1	2	3	4	5	6	7

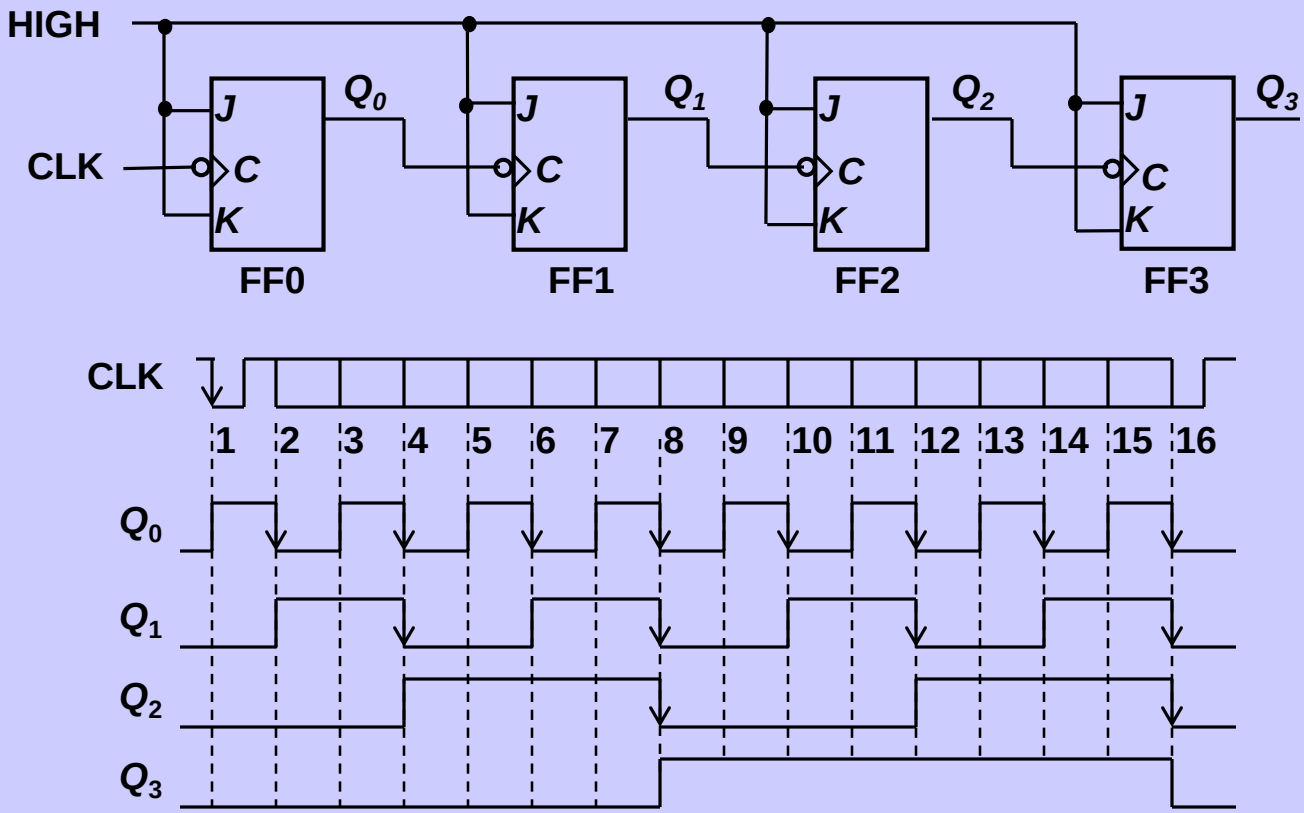
Asynchronous (Ripple) Counters

- Propagation delays in an asynchronous (ripple-clocked) binary counter.
- If the accumulated delay is greater than the clock pulse, some counter states may be misrepresented!

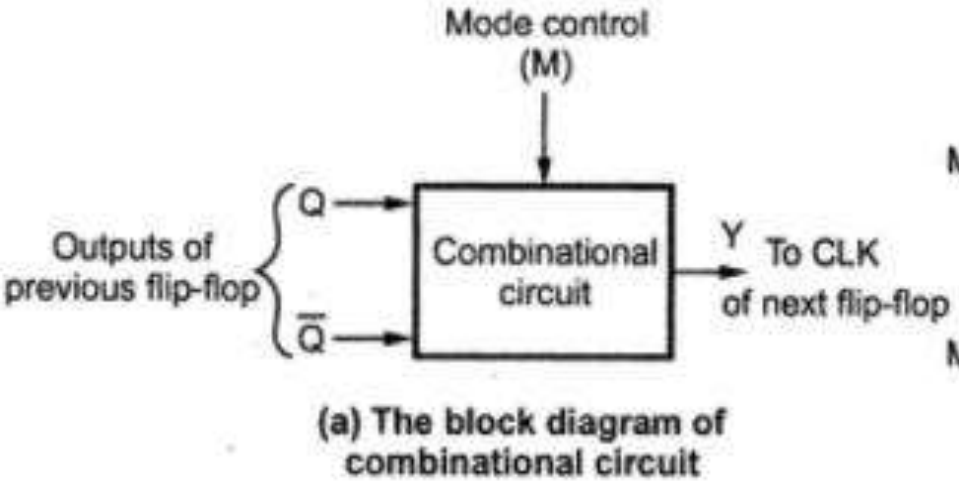


Asynchronous (Ripple) Counters

- Example: 4-bit ripple binary counter (negative-edge triggered).



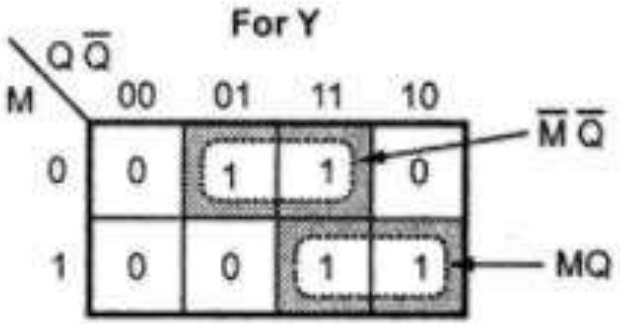
Asynchronous Up/Down Counters



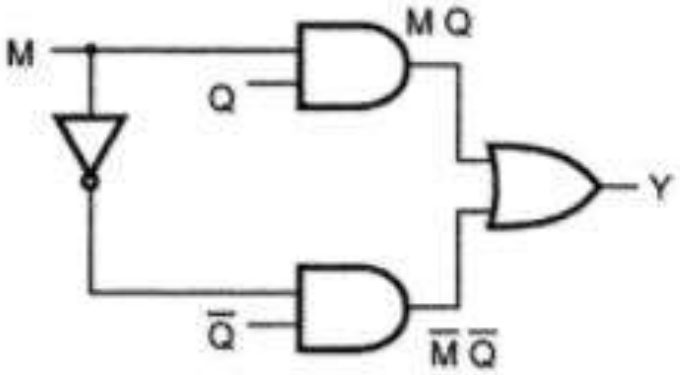
(a) The block diagram of combinational circuit

	Inputs M	Q	$\overline{Q}$	Output Y	
M = 0	0	0	0	0	$Y = \overline{Q}$ for down counting
	0	0	1	1	
	0	1	0	0	
	0	1	1	1	
M = 1	1	0	0	0	$Y = Q$ for up counting
	1	0	1	0	
	1	1	0	1	
	1	1	1	1	

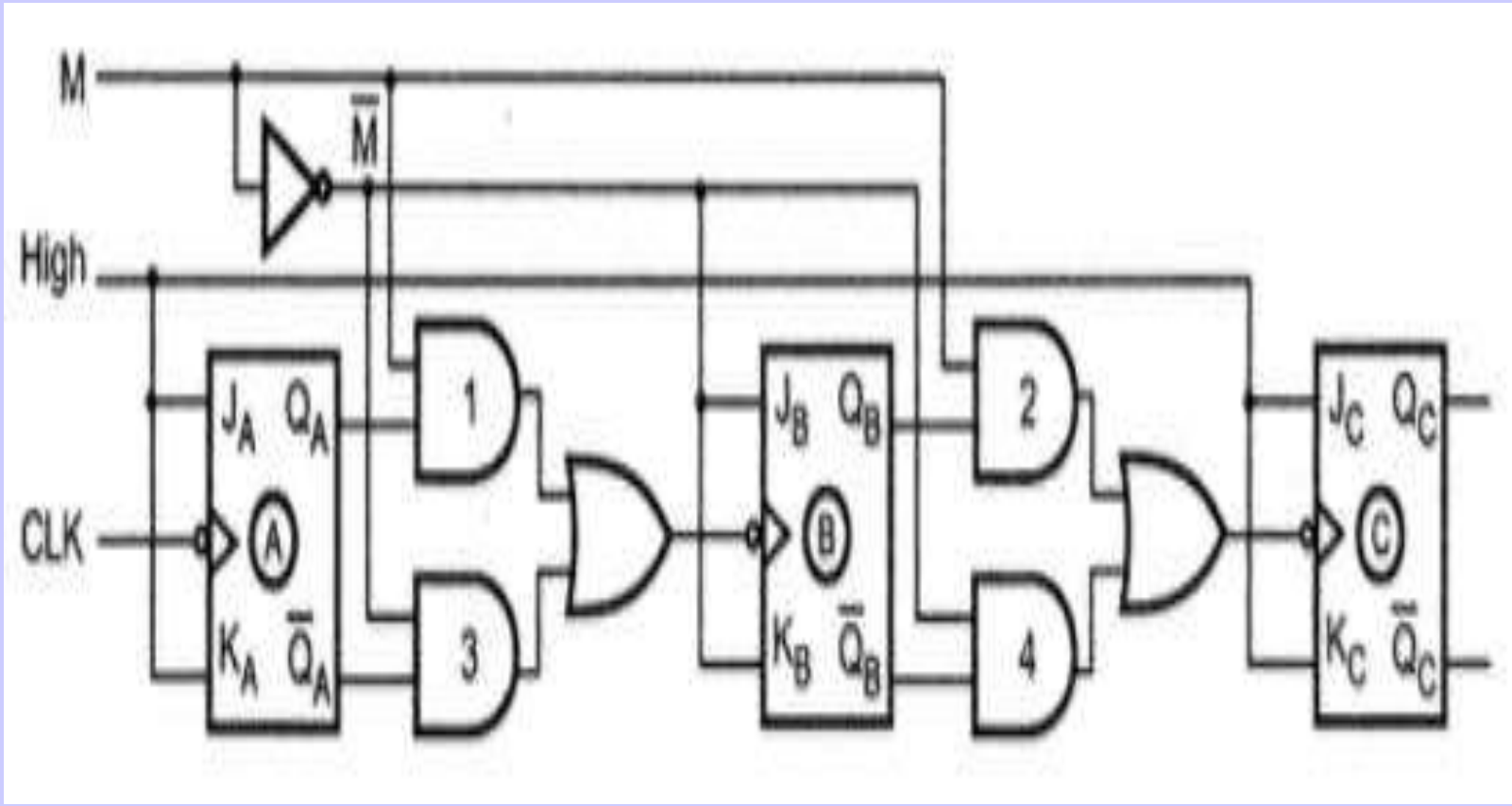
(b) Truth table



$\therefore Y = \overline{M}\,\overline{Q} + MQ$



A logic 1 on M enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs to drive the clock inputs of their respective next stages. So that counter will count up. When M is logic 0, AND gates 1 and 2 are disabled and AND gete 3 and 4 are enabled. This allows the $\overline{Q}_A$ and $\overline{Q}_B$ outputs to drive the clock inputs of their respective next stages so that counter will count down.



Quick Quiz

- How many natural states will there be in a 4-bit ripple counter?

  a) 4
  b) 8
  c) 16
  d) 32

Quick Quiz

- A ripple counter's speed is limited by the propagation delay of _____

  a) Each flip-flop
  b) All flip-flops and gates
  c) The flip-flops only with gates
  d) Only circuit gates

Quick Quiz

- Internal propagation delay of asynchronous counter is removed by _____

  a) Ripple counter
  b) Ring counter
  c) Modulus counter
  d) Synchronous counter