Lab Report 7

Computer Architecture Lab

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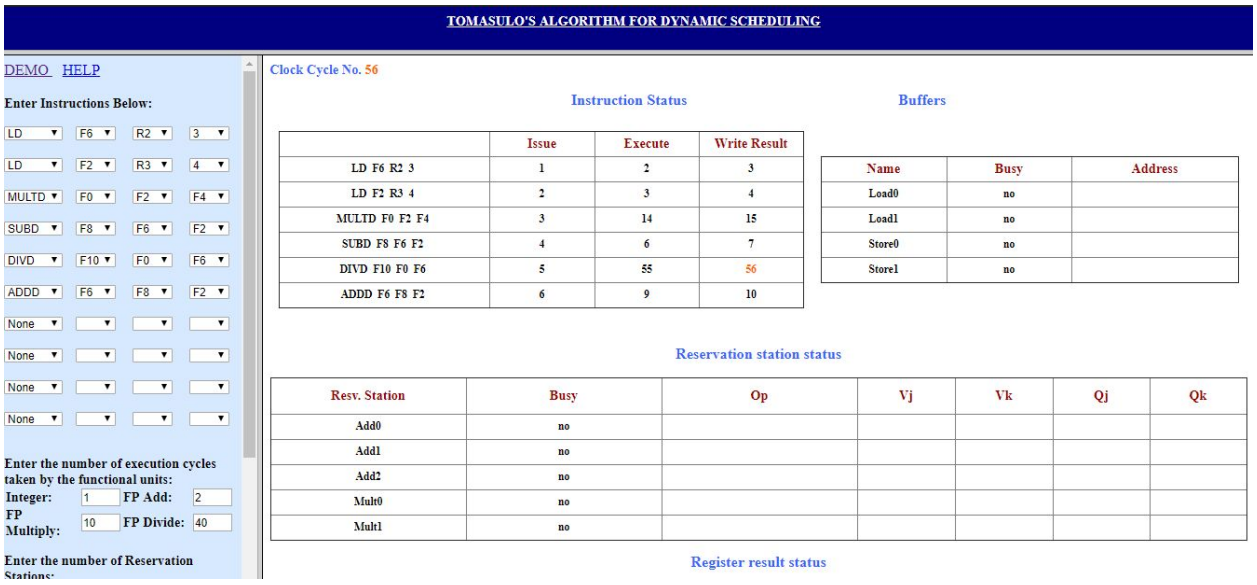
Aim

To apply Tomasulo's algorithm for instruction level parallelism and compare the performance with Scoreboarding.

Questions and Answers

Problem - 1

```
LD     F6    34+    R2
LD     F2    45+    R3
MULTD  F0    F2     F4
SUBD   F8    F6     F2
DIVD   F10   F0     F6
ADDD   F6    F8     F2
```



TOMASULO'S ALGORITHM FOR DYNAMIC SCHEDULING

DEMO HELP

Enter Instructions Below:

LD	F6	R2	3
LD	F2	R3	4
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2
None			
None			
None			
None			

Enter the number of execution cycles taken by the functional units:

Integer: 1 FP Add: 2

FP Multiply: 10 FP Divide: 40

Enter the number of Reservation Stations:

Clock Cycle No. 56

Instruction Status

	Issue	Execute	Write Result
LD F6 R2 3	1	2	3
LD F2 R3 4	2	3	4
MULTD F0 F2 F4	3	14	15
SUBD F8 F6 F2	4	6	7
DIVD F10 F0 F6	5	55	56
ADDD F6 F8 F2	6	9	10

Buffers

Name	Busy	Address
Load0	no	
Load1	no	
Store0	no	
Store1	no	

Reservation station status

Resv. Station	Busy	Op	Vj	Vk	Qj	Qk
Add0	no					
Add1	no					
Add2	no					
Mult0	no					
Mult1	no					

Register result status

Answer the following questions:-

1. After how many clock cycles can this program branch back to the beginning?

56 (62 in case of scoreboarding)

2. Does re-ordering influence the execution time of this program and how?

No.

3. Is there a Write-after-Read hazard present and how is it solved?

Yes, there is write-after-read hazard in last two instructions which are resolved by Tomasulo Algo.

Problem - 2

```
LD F0, 0(R1)
ADDD F4, F0, F2
SD F4, 0, R1
LD F0, -8(R1)
ADDD F4, F0, F2
SD F4, -8(R1)
```

Answer the following questions:-

1. After how many clock cycles can this program branch back to the beginning?

9 (24 in case of scoreboarding)

2. Does re-ordering influence the execution time of this program and how?

No

3. Is there a Write-after-Read hazard present and how is it solved?

No, there isn't any Write-after-Read Hazard.

Problem - 3

```
LD F0, 0(R1)
LD F4, 4(R1)
MULTD F8, F0, F2
LD F4, 6(R1)
LD F6, 5(R1)
MULTD F10, F4, F6
ADDD F10, F6, F10
LD F8, 3(R1)
ADDD F10, F10, F8
```

Answer the following questions:-

1. After how many clock cycles can this program branch back to the beginning?

32 (65 in case of scoreboarding)

2. Does re-ordering influence the execution time of this program and how?

No

3. Is there a Write-after-Read hazard present and how is it solved?

Yes, in second last and third last instruction there is write-after-read hazard which is resolved by register renaming.