Lab Report 6

Computer Architecture Lab

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Aim

Record for each instruction in which clock-cycle it is in each of the traversed pipeline stages.

Questions and Answers

Problem - 1

ld F6, 34(R2)

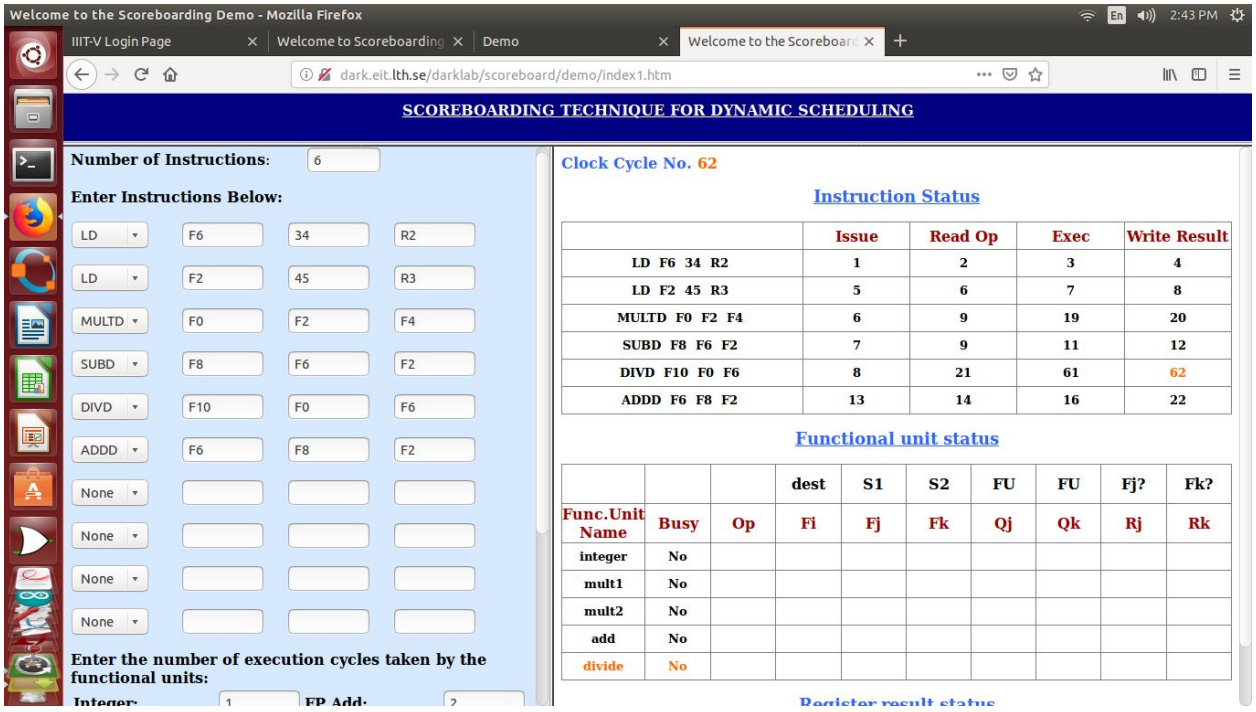
ld F2, 45(R3)

multd F0, F2, F4

subd F8, F6, F2

divd F10, F0, F6

addd F6, F8, F2



Answer the following questions:-

1. After how many clock cycles can this program branch back to the beginning?

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2. Does re-ordering influence the execution time of this program and how?

Yes, we can save two clock cycles by swapping the first two instructions. Previously, the third instruction completed at 20th clock cycle but if we swap it, the same instruction would be completed on the 18th clock cycle.

3. Is there a Write-after-Read hazard present and how is it solved?

Write-after-Read hazard is present between the last two instructions. Write-after-read is a hazard but it is causing no stalls, so there is no need to solve it.

Problem - 2

ld F0, 0(R1)

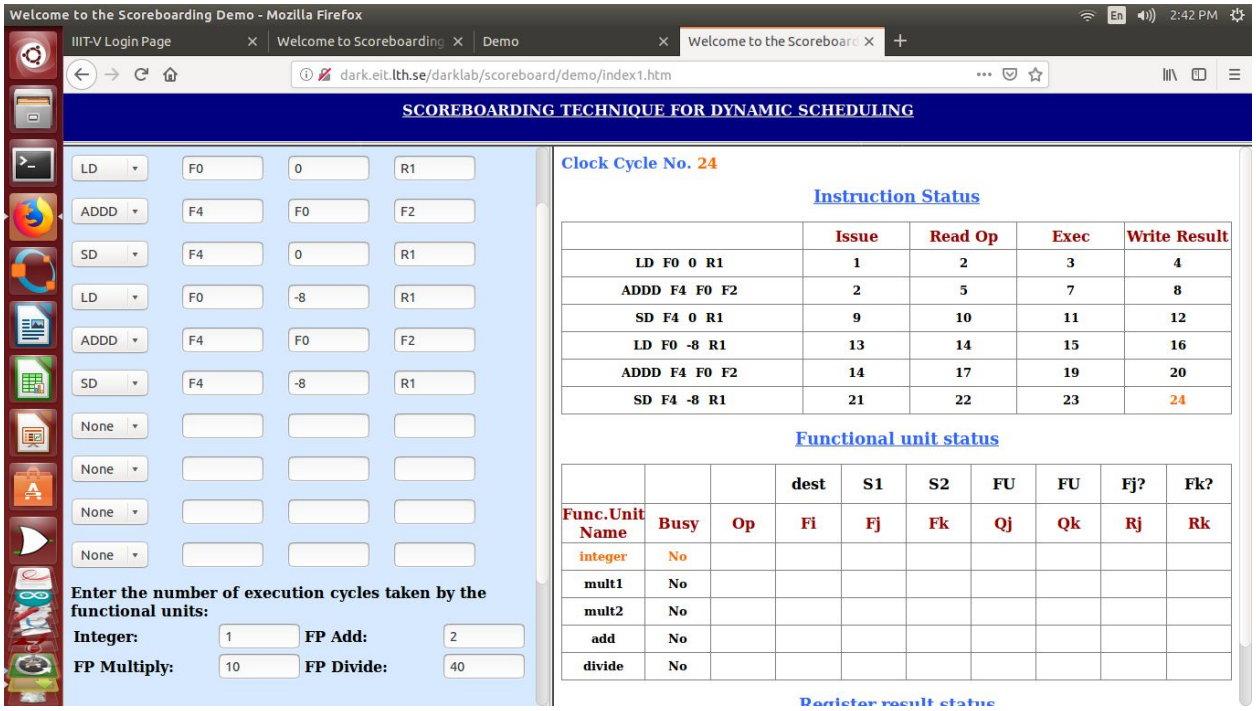
addd F4, F0, F2

sd F4, 0(R1)

ld F0, -8(R1)

addd F4, F0, F2

sd F4, -8(R1)



Answer the following questions:-

1. After how many clock cycles can this program branch back to the beginning?

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2. Does re-ordering influence the execution time of this program and how?

Yes, we can save two clock cycles by swapping the third and fourth instructions. Previously, the third instruction completed at 12th clock cycle but if we swap it, the same instruction would be completed on the 10th clock cycle.

3. Is there a Write-after-Read hazard present and how is it solved?

No, there isn't any Write-after-Read Hazard.